PMC-SIERRA

Passave

Framing and Integration for Stream-based FEC

Jeff Mandin

802.3av Knoxville

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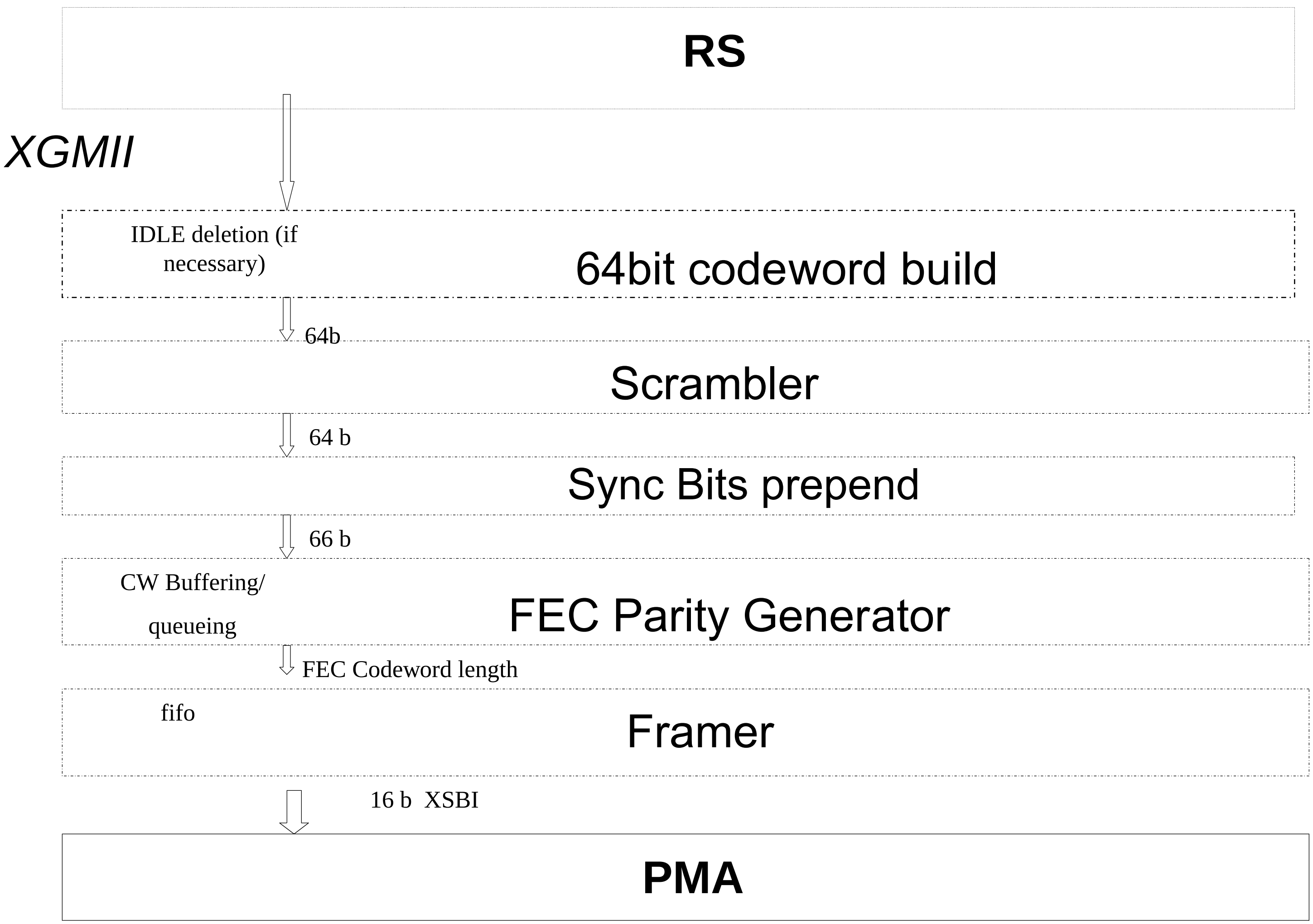
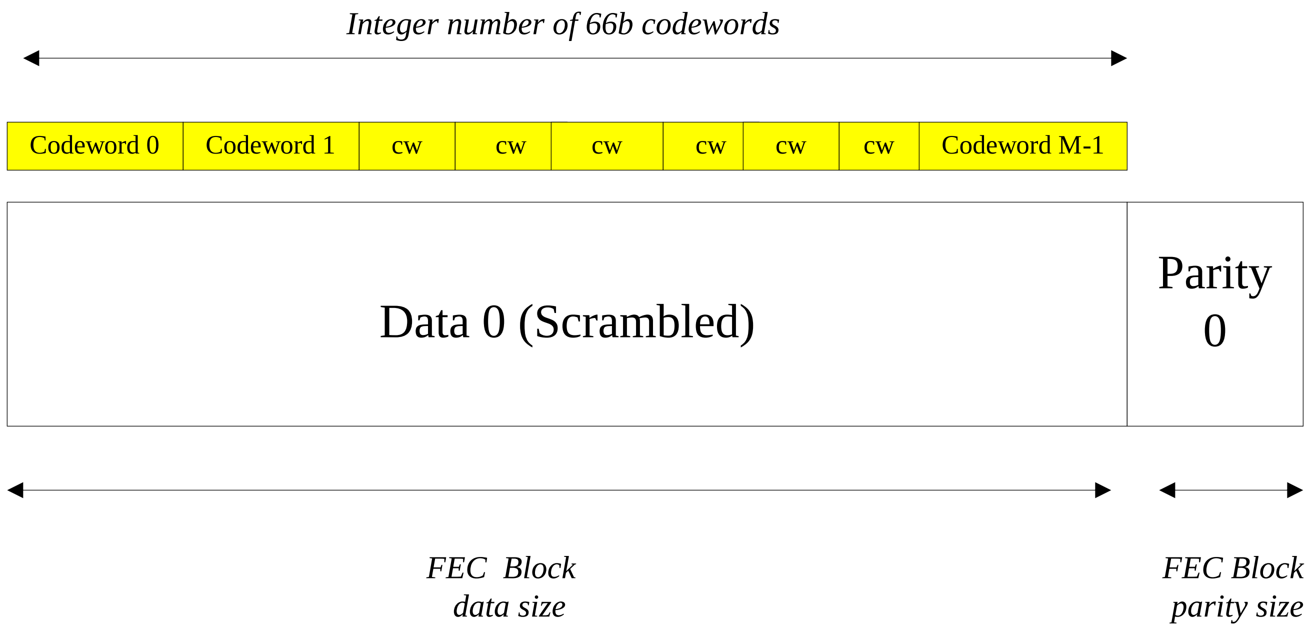
Agenda

1. High-level view of PCS processing sequence
2. Downstream Framing
   - Receiver synchronization
3. Upstream Framing
   - Shortened Final FEC block on upstream
   - Receiver synchronization
4. Time Quantum issues

10G EPON PCS processing sequence (10GBASE-R)



Format of Downstream PCS <-> PMA Frame



Format of Downlink PCS <-> PMA Frame

- No synchronization header necessary
- FEC code should be designed to accommodate an integer number of 66b codewords
  - Codeword sync is implicitly accomplished with FEC block sync

Receiver Synchronization on Downstream

- ONU synchronizes on the downstream using a *serial locking* algorithm:

  1. Select a bit position as potential beginning of a FEC block
  2. Run the FEC parity check/correction function
  3. If parity check fails ("uncorrectable block"), then slip to the next bit position

- If parity check passes for 4 consecutive blocks then we declare that FEC block sync has been established
- Codeword sync has also been established implicitly

- **Benefits:** no byte overhead; no seek delay; no dependency on bit error resistance; no special lock logic in ONU

Shortened Final FEC block (upstream)

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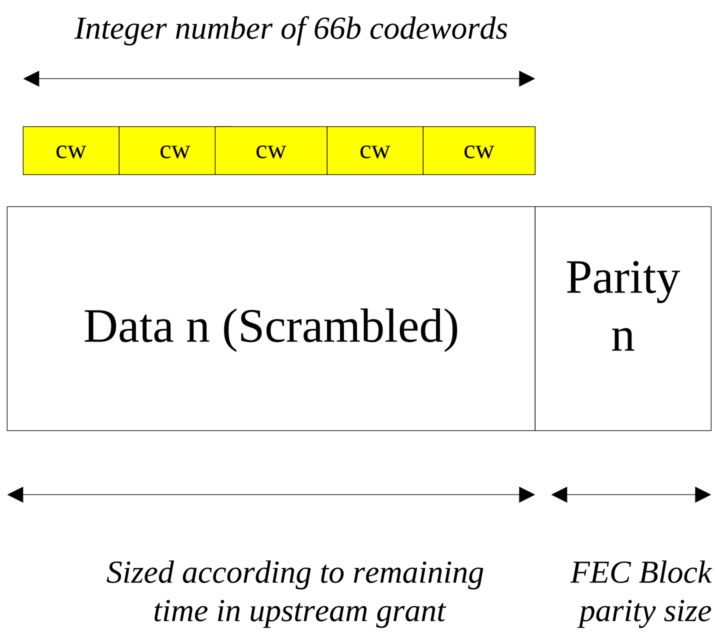
- Appears to be required because of MPCP
  - Idle ONUs periodically generate 64 byte REPORT messages
- Avoiding additional framing overhead for the shortened block:
  - ONU sends shortened final FEC block in the upstream only when its allocated transmission time in the GATE is insufficient for a full FEC block
  - ONU must not turn off its laser before the end of its grant
  - OLT maintains info on the grant - so it is able to determine where shortened data portion terminates and parity starts

Shortened Final FEC block (upstream only)

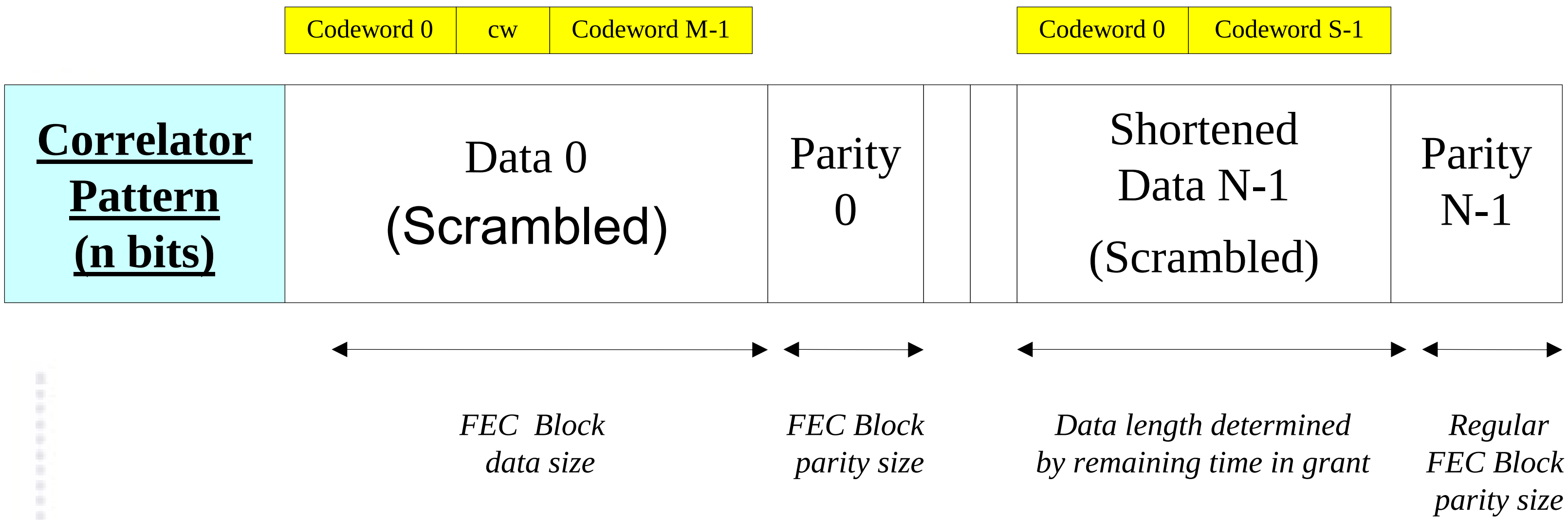


Fast Receiver Synchronization on upstream (burst mode)

- Upstream burst begins with a <n> bit delimiter (similar to S_FEC in GEPON) not contained in 66b codeword or FEC block

- After PMD layer bit sync, OLT seeks start-of-burst correlation sequence:
  1. Received datastream is fed into Linear Feedback Shift Register
  2. Taps measure the Hamming Distance from fixed correlation sequence
  3. If computed Hamming Distance is less than the threshold, then lock is declared

Format of Uplink PCS <-> PMA Frame (w/ shortened final code word)



Value of Time Quantum for 10G upstream

- For a 10Gbps PCS, clock will generally run at 156 Mhz – in which case:
  - Time Quantum of 6.4 ns is most natural
  - TQ of 16ns is not an integral number of clock cycles
- Moreover: 6.4 ns TQ yields grant granularity of 8 bytes
  - More flexibility to create good structure definitions
    - Better efficiency ultimately
- We've already said we would modify Fec_Overhead() definition in the MPCP clause
  - Adjusting TQ due to link speed up should be no more problematic

Thank you

Downstream Receiver Synchronization – An Implementation

- Downstream lock time does not have to be particularly fast in an EPON
  - Less than 1ms is fine
  - REGISTER is necessary before there can be data traffic
- One implementation approach is to make a decoding attempt once per "possible FEC block" ie.
  - the receiver accumulates a FEC block's worth of data (ie. up to bit <n>)
  - then the receiver decodes/correct the block
  - while correcting the block, the receiver accumulates the next block (ie. from bit <n+1> on)
  - If the decode fails, the receiver tries to decode the next candidate FEC block beginning at bit <n+2>
- The time to receive a block w/ RS (239, 255) is 197.81 ns. Maximum number of blocks received to lock is 2040.
- So maximum lock time is 197.81*2040 = 403549 ns = about .4ms
- If necessary, the receiver can decode/correct more than one FEC block at once in a pipeline implementation
  - Maximum number of concurrent blocks would be equal to the FEC processing latency time (measured in blocks)