
# 10Gbps Burst Mode Clock and Data Recovery

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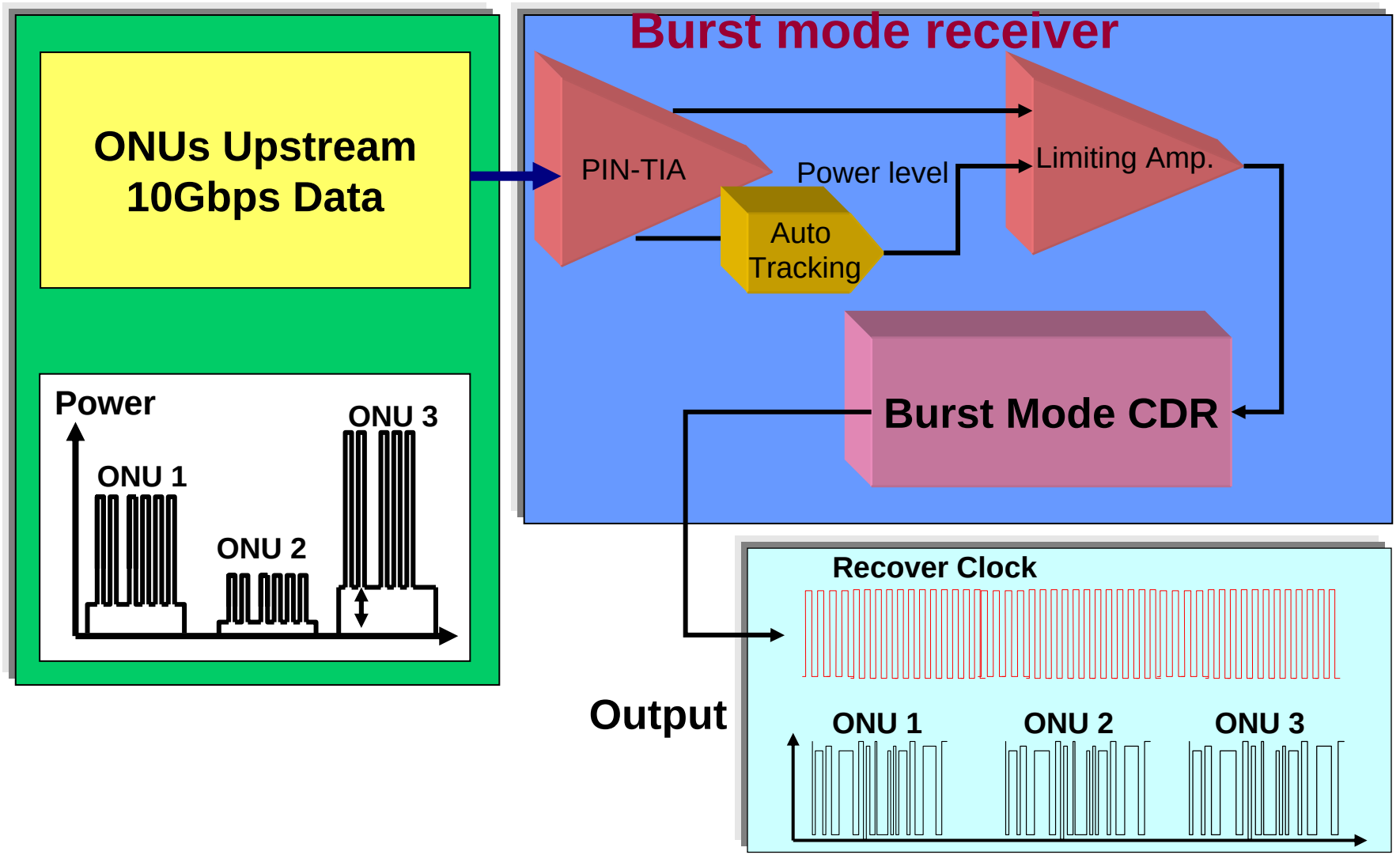
# Motivation

- Both asymmetric and symmetric operation of 10GEPON need to be studied
  - Two options for 10Gb/s EPON PHY : asymmetric (10Gb/s downstream/ 1Gb/s upstream) mode and symmetric (10Gb/s downstream/ 10Gb/s upstream) mode.
  - No discussion on symmetric operation in the previous meetings.
- Many applications require higher upstream data rate
  - Such as Enterprise Networking, Video Conference, P2P, Personal Multimedia Publishing
- Two major challenges in OLT PHY when symmetric operation are considered
  - Automatic gain control: (need power level adjustment mechanism)
  - 10Gb/s Burst Mode Data retiming
  - ➢ We focus on 10Gbps Burst Mode clock and data recovery

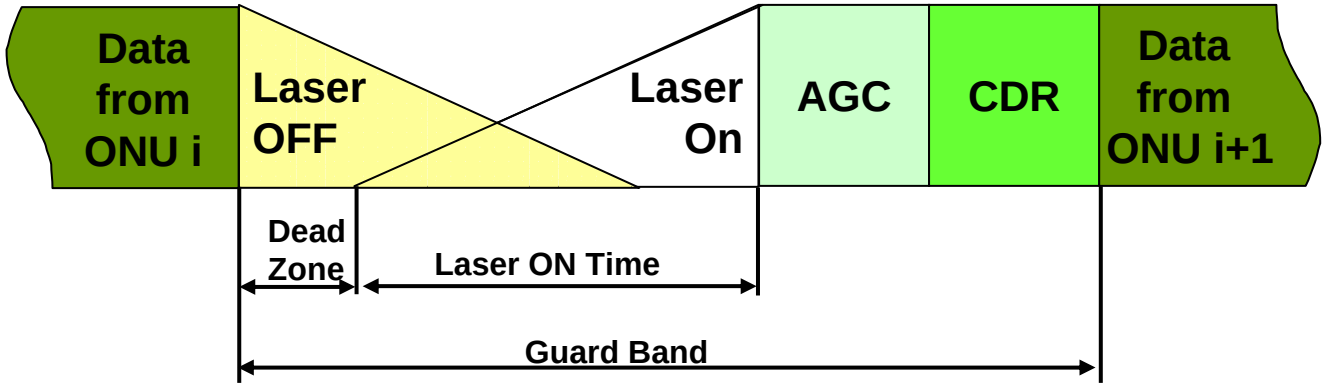
# Burst Mode Receiver in PON networks



# Burst Mode Receiver Requirement

- **Goal: Keep the PHY overhead not worse than than 1GEPON**

| Data Rate | Dead Zone | Laser On | AGC | CDR | Guard Band Overhead Efficiency |
|---|---|---|---|---|---|
| 1Gbps | ≤ 128 ns | ≤ 512 ns | ≤ 400 ns | ≤ 400 ns | 6.14% |
| 10Gbps | TBD | TBD | TBD | Goal:≤ 40ns (400bits) | Goal: <6.14% |




Reference: Glen Kramer
The 5th International Conference on Optical Internet (COIN 2006)
Hyatt Regency Jeju, Korea / July 9 - 13, 2006

$$guard\_overhead = \frac{(laser\_ON + dead\_zone + AGC + CDR) \times N_{ONU}}{cycle\_time}$$

# Burst Mode CDR Methods

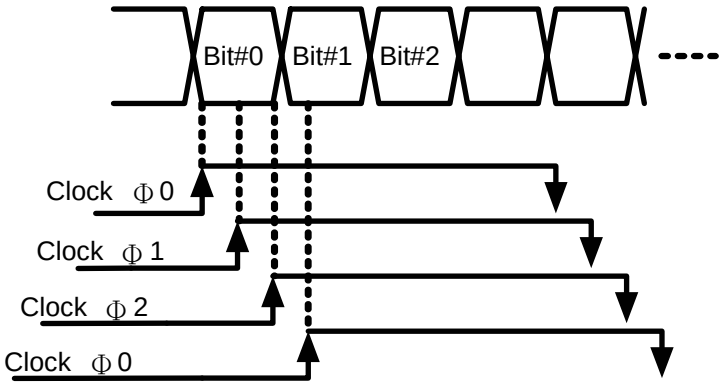
1. Using multi-phase clocks to over-sample the data
   - **Multiple samples on one bit and choose a proper sample**
   - **Feed-forward mechanism: Very high loop bandwidth**
2. Feed-back based clock recovery scheme
   - **GPLL,DLL, G-VCO**
   - **Require many transitions=> long acquisition time and waste bandwidth**

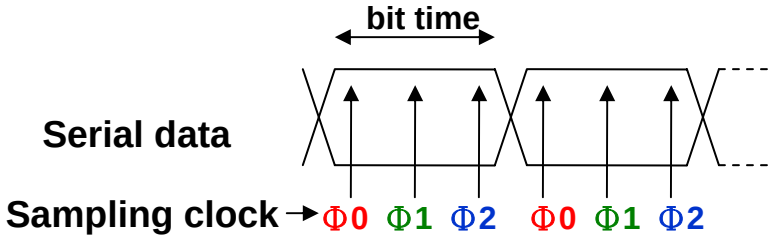
**This presentation provides a preliminary discussion of over-sampling method**

# Phase Picking Over-Sampling CDR

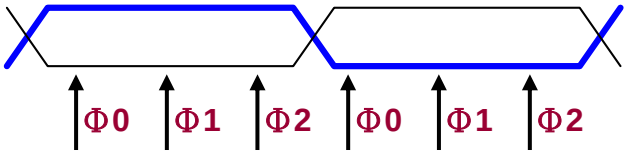
## Over-Sampling

- 3 times OverSampling
- Generate 3 different phase clocks



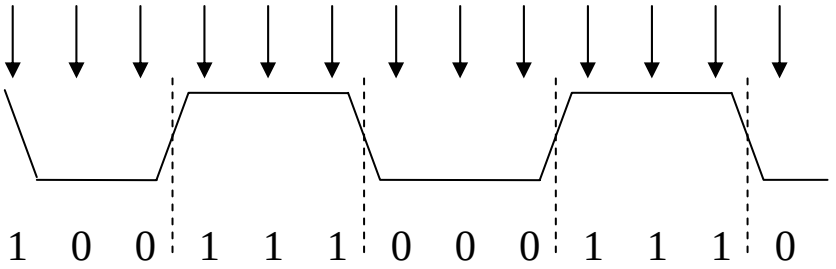




## Phase Picking




Sampled data 1 1 1 0 0 0

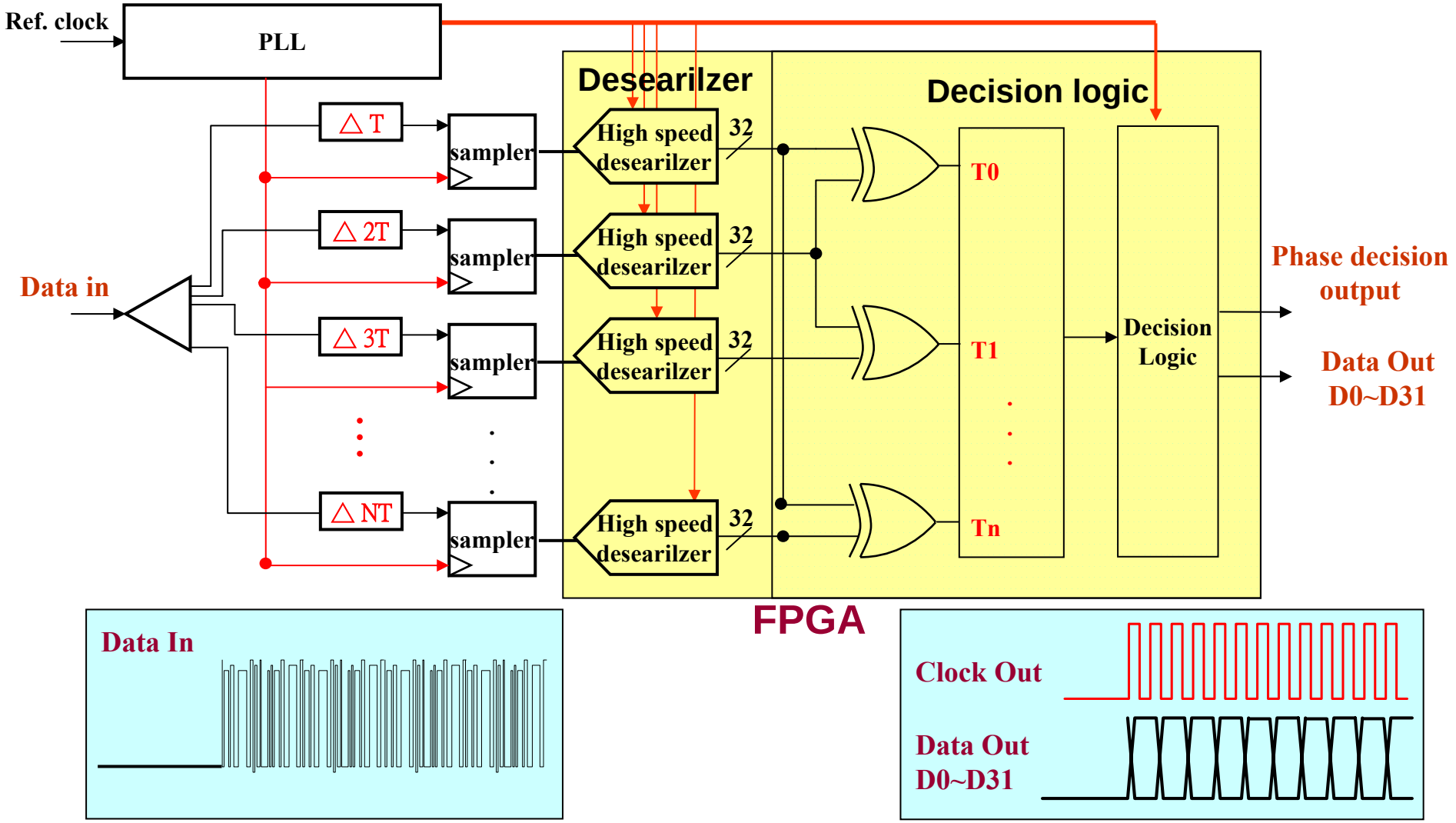
EX_OR transition 0 0 1 0 0



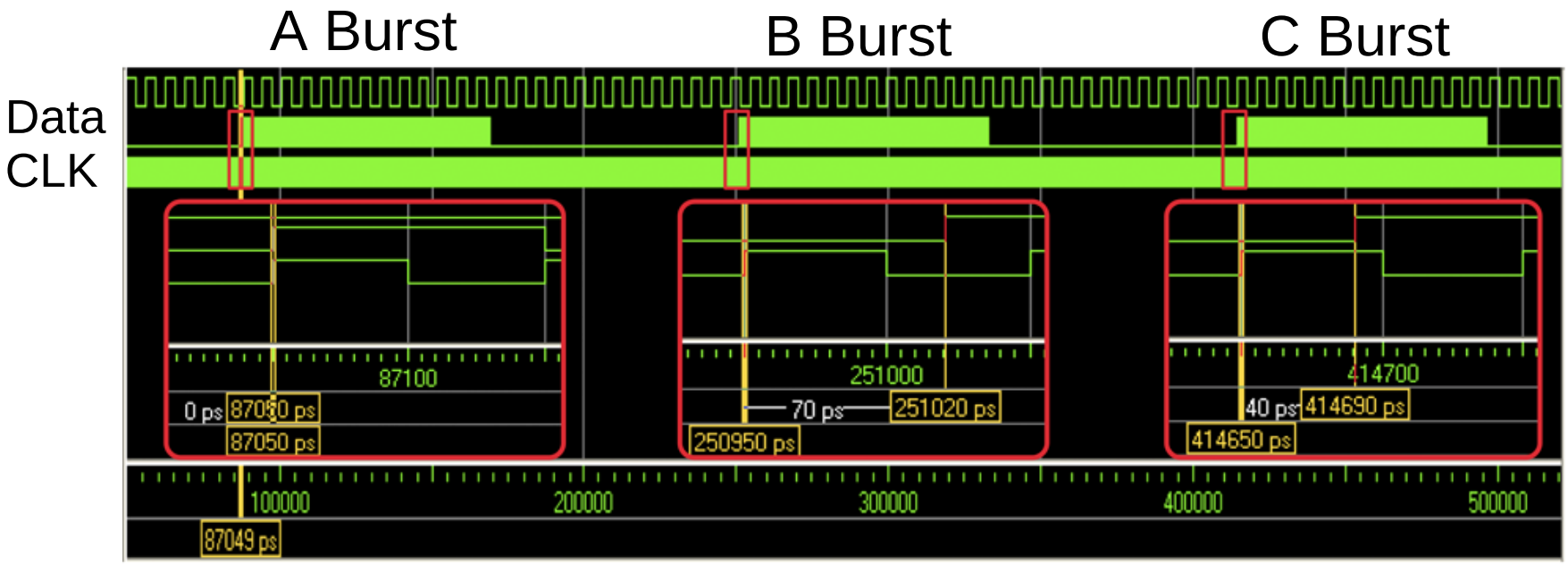

Transition mark 1 0 1 0 0 1 0 0 1 0 0 1

Transition count 1 0 4

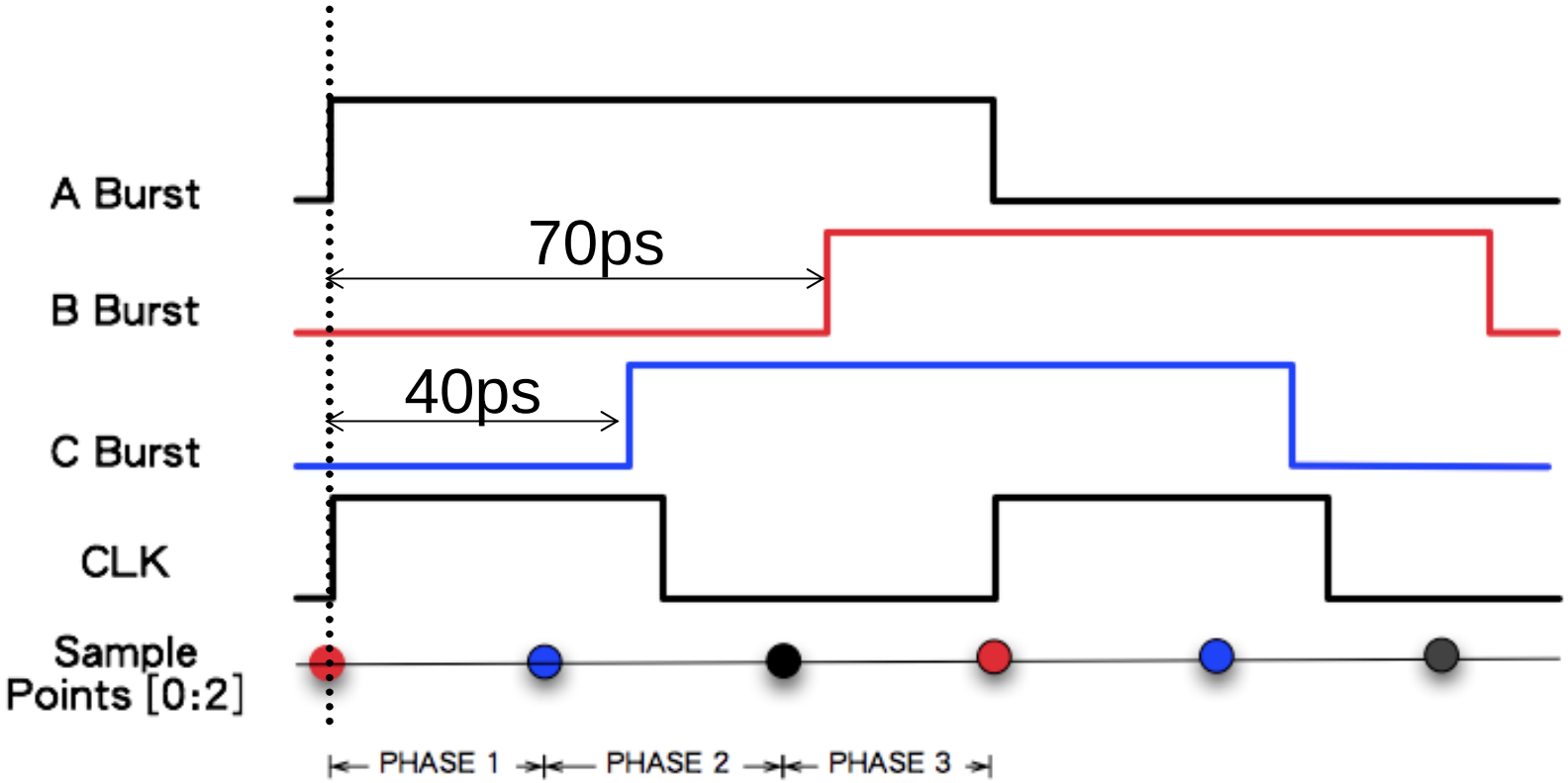
# Phase-Picking Over-Sampling CDR Architecture



# Test Bursts with different incoming phases



# Phase relationship of three bursts



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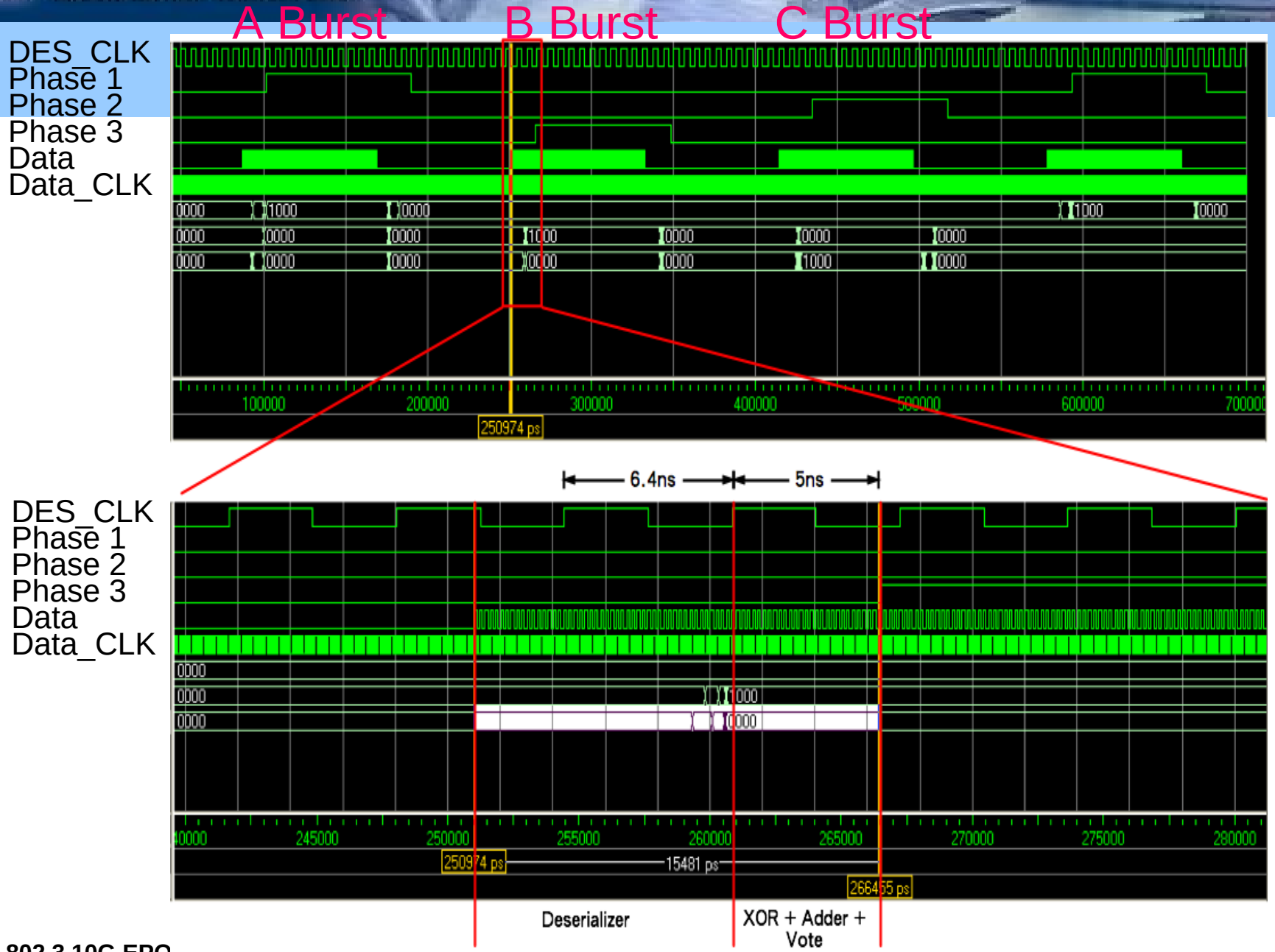
# Post-simulation results



# Conclusions

- **Over-sampling architecture can be applied in the 10G burst mode PON environment.**
- **32*3 =96 bits, which is less than the goal, 400 bits, preamble are required for burst mode phase picking.**
- **With an integrated sampler and a commercially available FPGA, clock data recovery problem for 10Gb/s upstream can be solved.**