Interleaved FEC for 10G EPON

Dongsoo Lee, <d-soolee@etri.re.kr>
Hoon Lee, <hlee@etri.re.kr>
Bin Yeong Yoon, <byyun@etri.re.kr>

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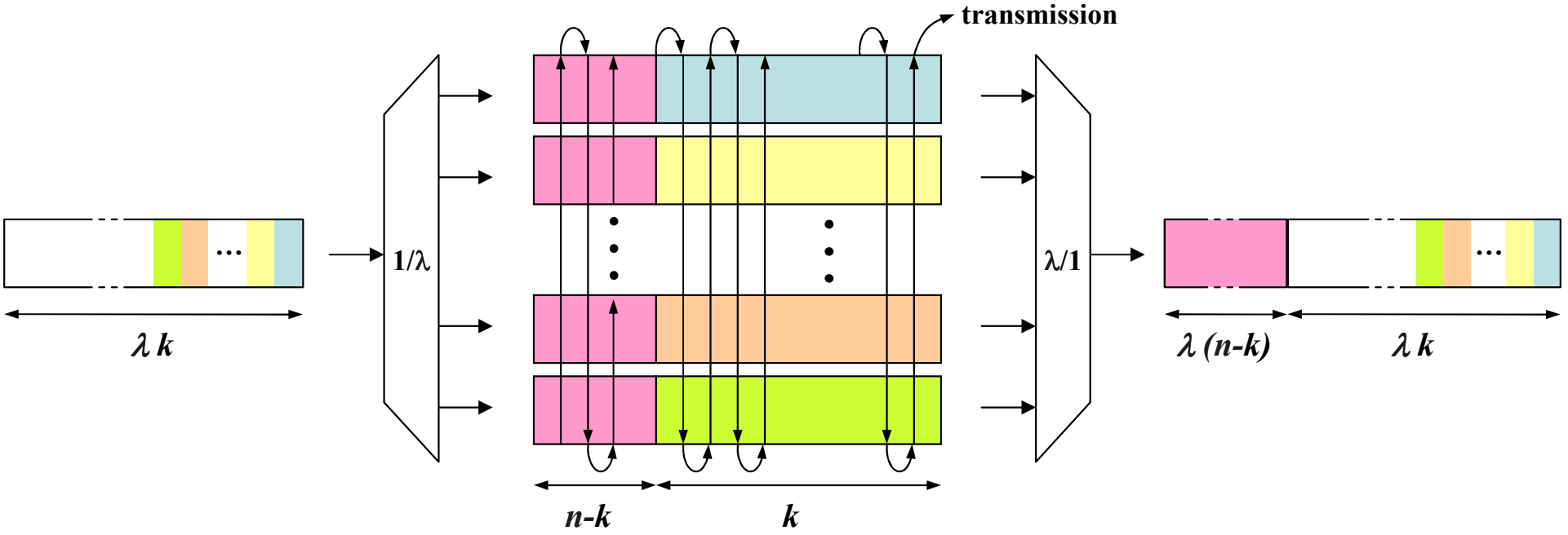
Introduction

- This presentation
  - Proposes use of interleaved FEC for practical implementation at 10G bit rate
  - Does not propose a specific FEC algorithm
  - Does not specify a FEC rating
- Backgrounds
  - For 1G EPON,
    - FEC is processed at 1G bit rate with 8 bit datapath width
    - Clock speed for implementation with FPGA or ASIC is 125MHz, which is available target
  - For 10G EPON
    - Required clock speed will be 1.29GHz if FEC is processed with 8 bit datapath width, which is impractical at both commercial FPGA and ASIC technology
  - At 10G data rate
    - FEC should be parallel-processed for practical implementation when narrow datapath width is maintained for 10G EPON FEC

Parallel Process - Interleaved FEC

Interleaved FEC [1]

- Given an (n, k) cyclic code, it is possible to construct a (λn, λk) cyclic code by *interleaving*
- Simply processed by arranging λ code vectors in the original code into λ rows of a rectangular array and then transmitting them column by column
- The parameter λ is referred to as the *interleaving degree*



[1] Source: S. Lin and D. Costello, *Error Control Coding : Fundamentals and Applications*, Prentice Hall, Englewood Cliffs, New Jersey 1983

Clock Speed with Interleaved FEC

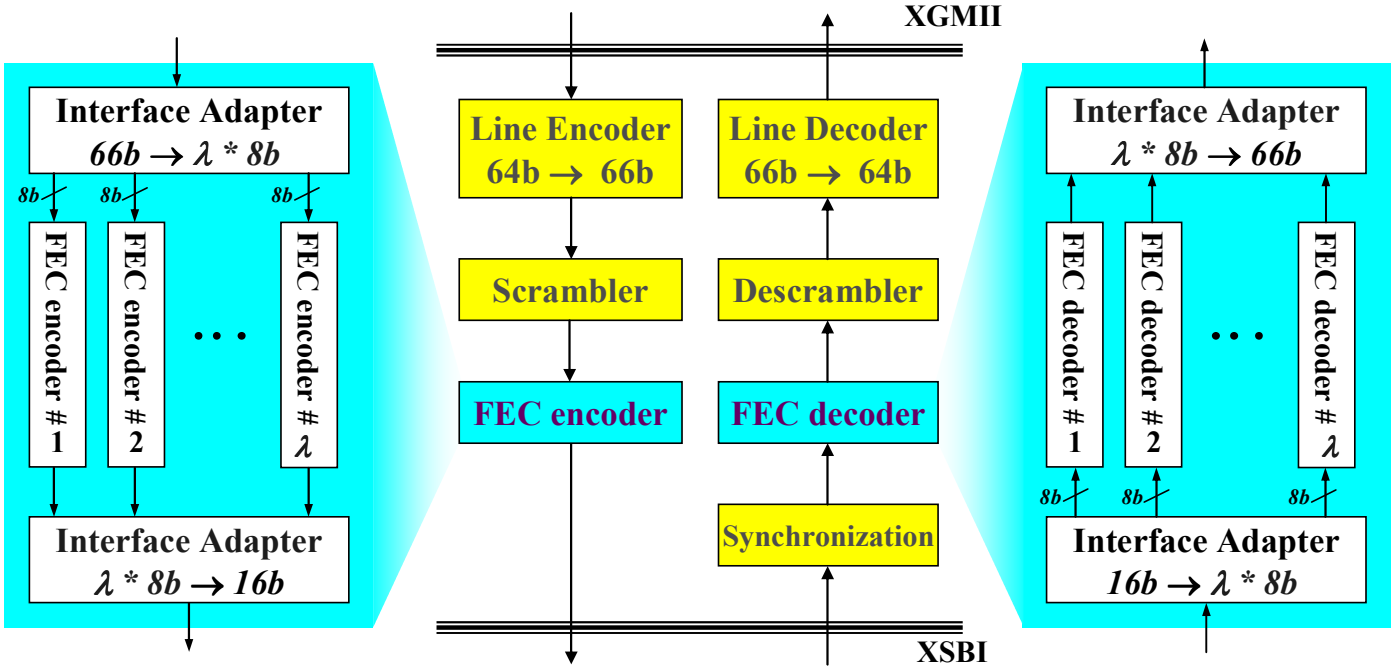
- Required clock speed at previous applications

Application	Bit Rate	Datapath width (λ)	FEC algorithm	Required Clock Speed	Referred Standard
EPON	1Gb/s	1 byte (1)	RS(255,239)	125 MHz	IEEE 802.3ah
Submarine systems	2.48832 Gb/s	1 byte (1)	RS(255,239)	332MHz	ITU-T G.975
	9.95328 Gb/s	4 byte (4)	RS(255,239)	332MHz	
OTU1	2.48832 Gb/s	16 byte (16)	RS(255,239)	21MHz	ITU-T G.709
OTU2	9.95328 Gb/s		RS(255,239)	84MHz	
OTU3	39.81312 Gb/s		RS(255,239)	333MHz	
Backplane Ethernet	10.3125 Gb/s	33 bit (-)	Shortened cyclic code (2112,2080)	312.5MHz [2]	IEEE802.3ap

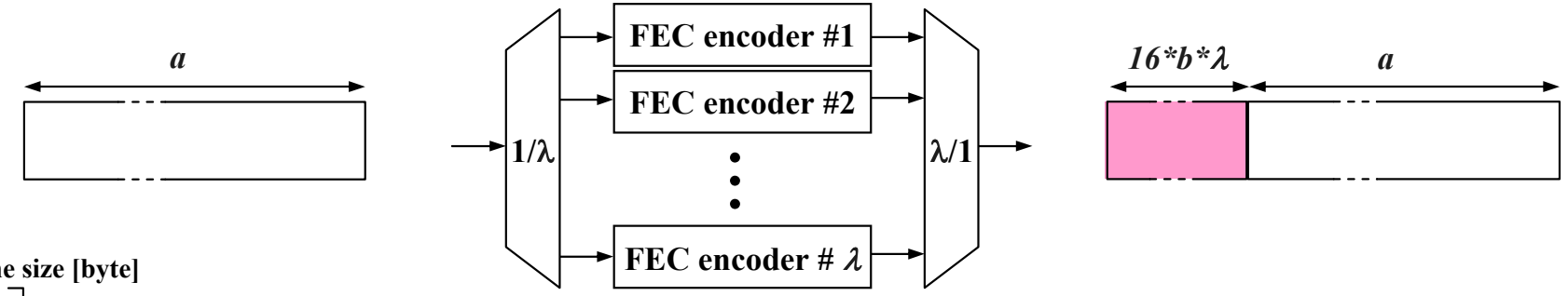
[2] Source: John D'Ambrosia, Adam Healey, "The state of IEEE 802.3ap Backplane Ethernet", DesignCon 2006.

Interleaved FEC for 10G EPON

- For explanation, use of RS (255, 239, 8) code is assumed
- FEC functional block



- FEC frames



* a is a frame size [byte]

* $b = \left\lceil \frac{\lceil a / \lambda \rceil}{239} \right\rceil$, the number of parity blocks for each FEC encoder

Summary

- For 10G EPON FEC, parallel processing is required for practical implementation when we maintain narrow datapath width

- For parallel process at 10G bit rate, interleaved FEC is;
  - *Practical* because it reduces the required clock speed from 1.29GHz to 322MHz when interleaving degree is 4
  - *Matured* because it is widely used in 10G applications

- For interleaved FEC, we need to consider;
  - *interleaving degree, λ* for efficient implementation
  - *FEC codeword* with better bandwidth efficiency