High Speed Jitter Test Points

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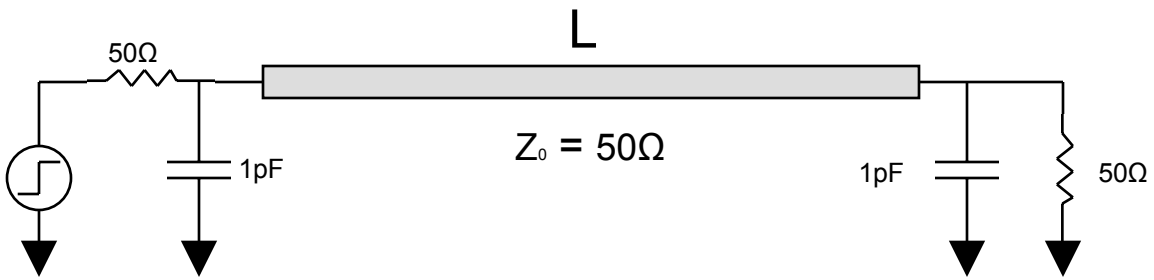
High Speed Link

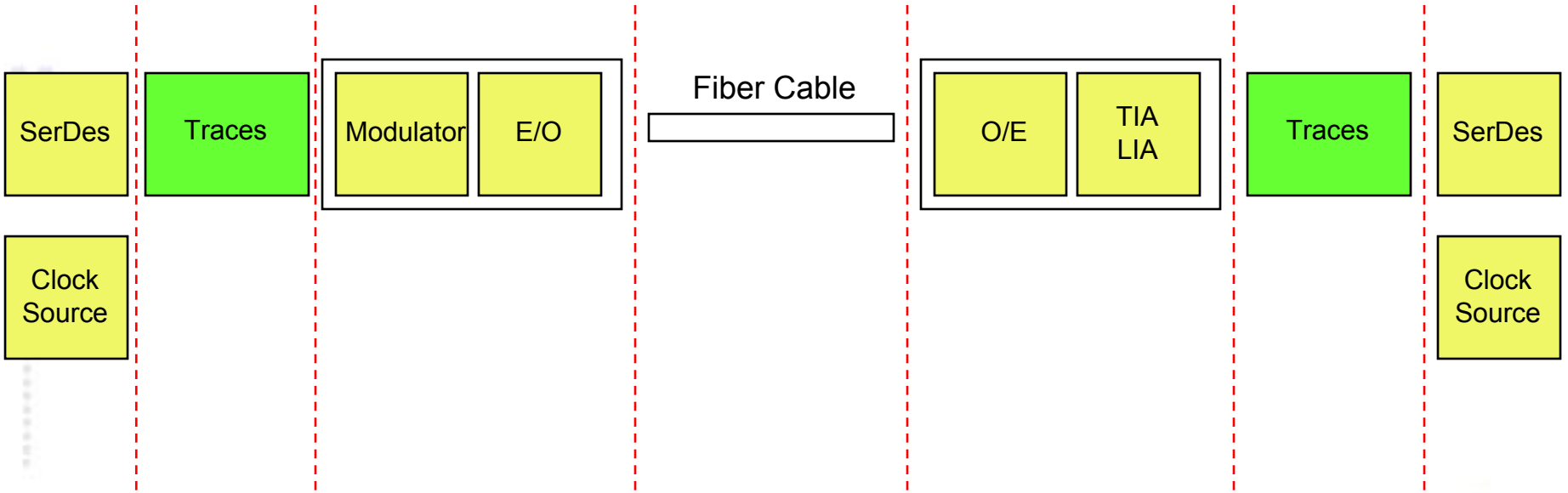
- The “Side Effect” of the interface between the SerDes and Optical Transceiver
  - Inter-Symbol Interference (ISI)
  - Reflection
  - Cross Talk
- To compensate this effect, the channel needs
  - Equalizer
  - Pre-Emphasis

Transmission Line

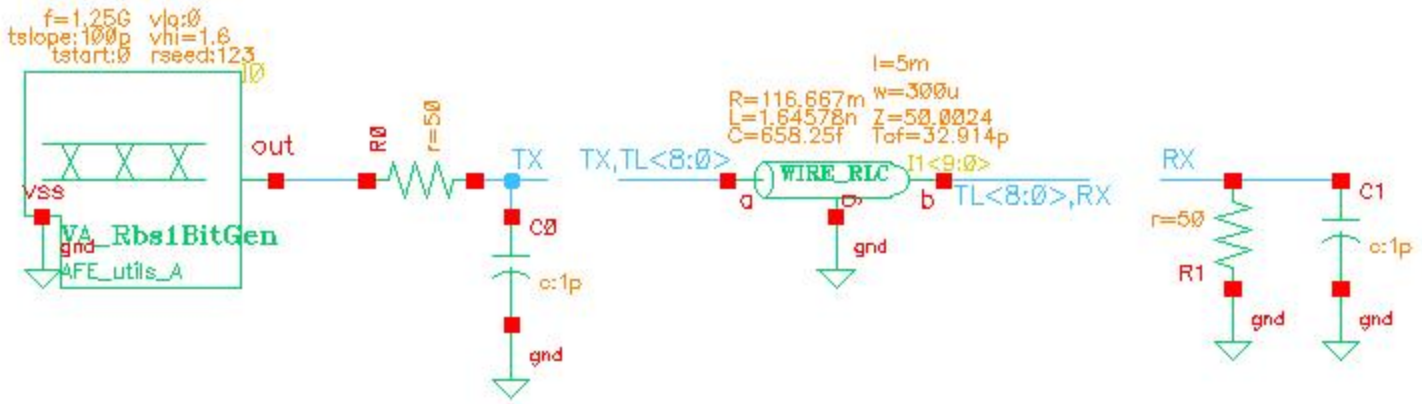
- Characteristics
  - Impedance Z_0
  - Length L



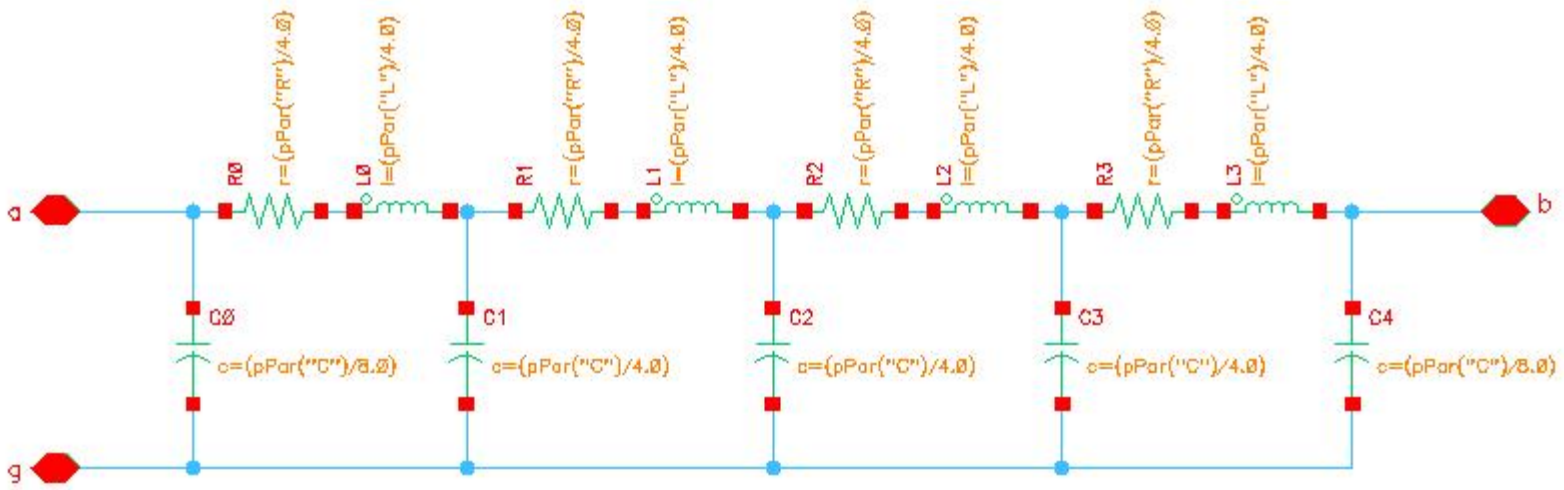
High Speed Optical Interface



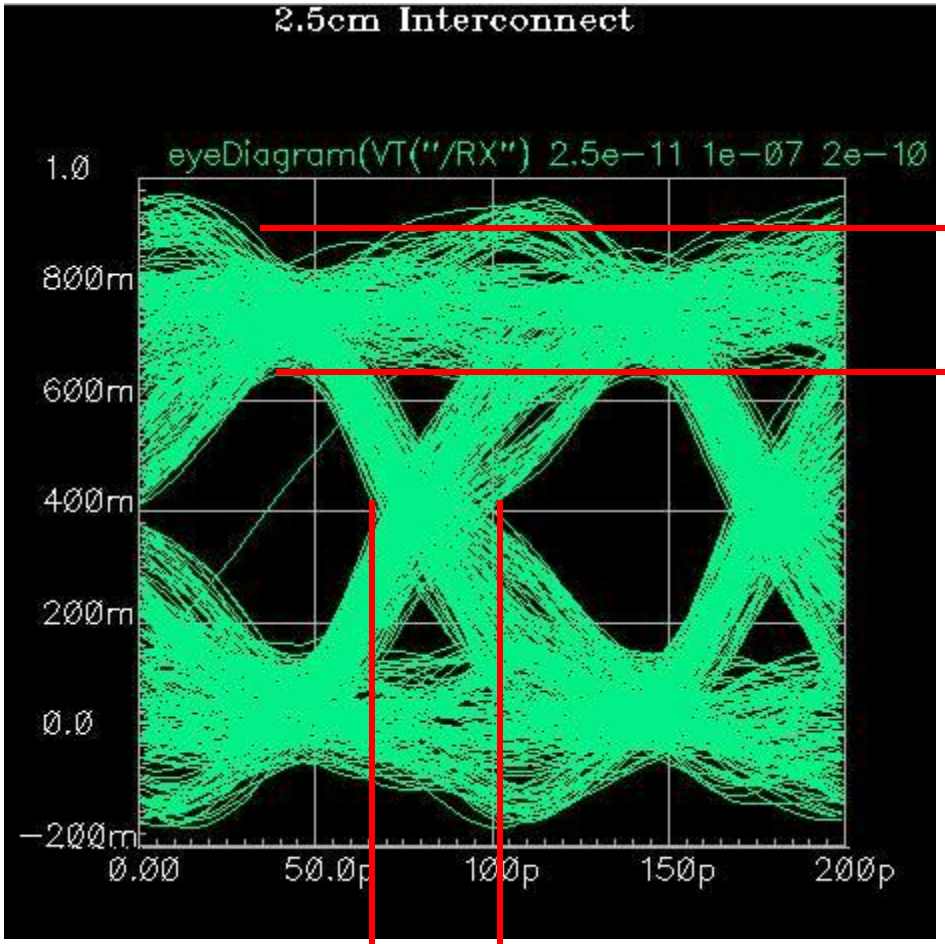
Simulation – Setup



Simulation – One Segment



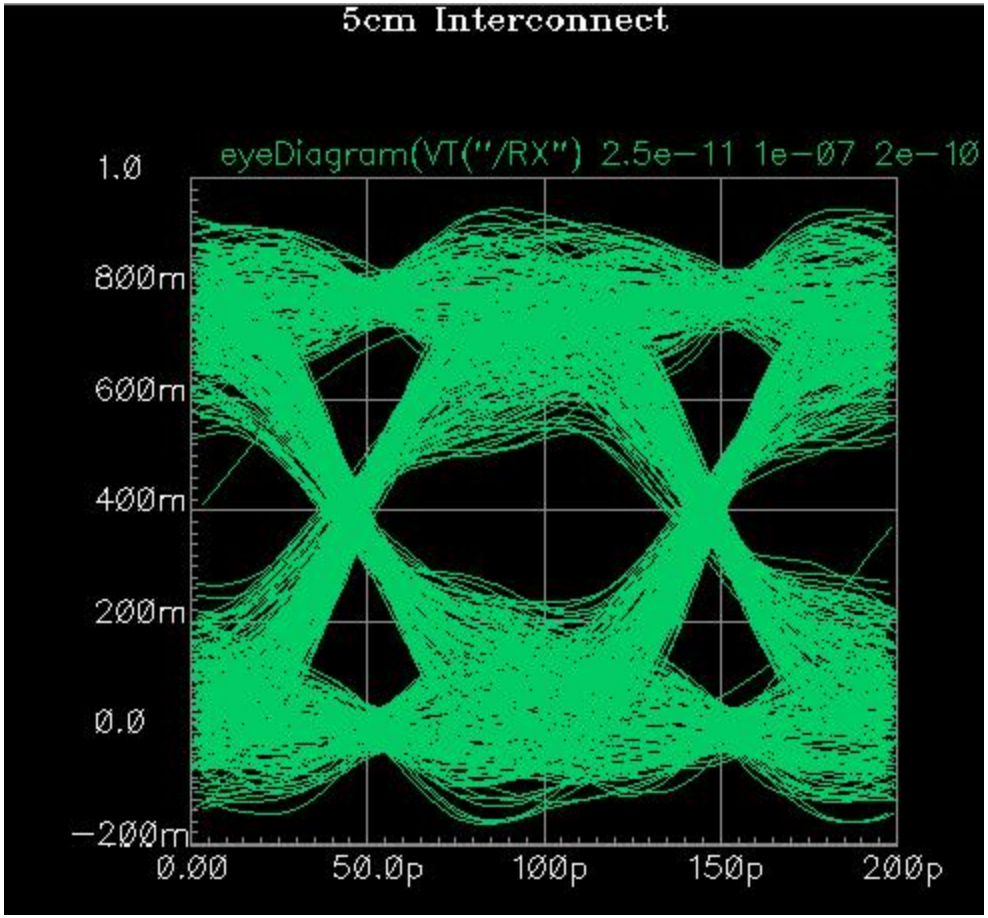
Simulation – 1” Length @10Gbps



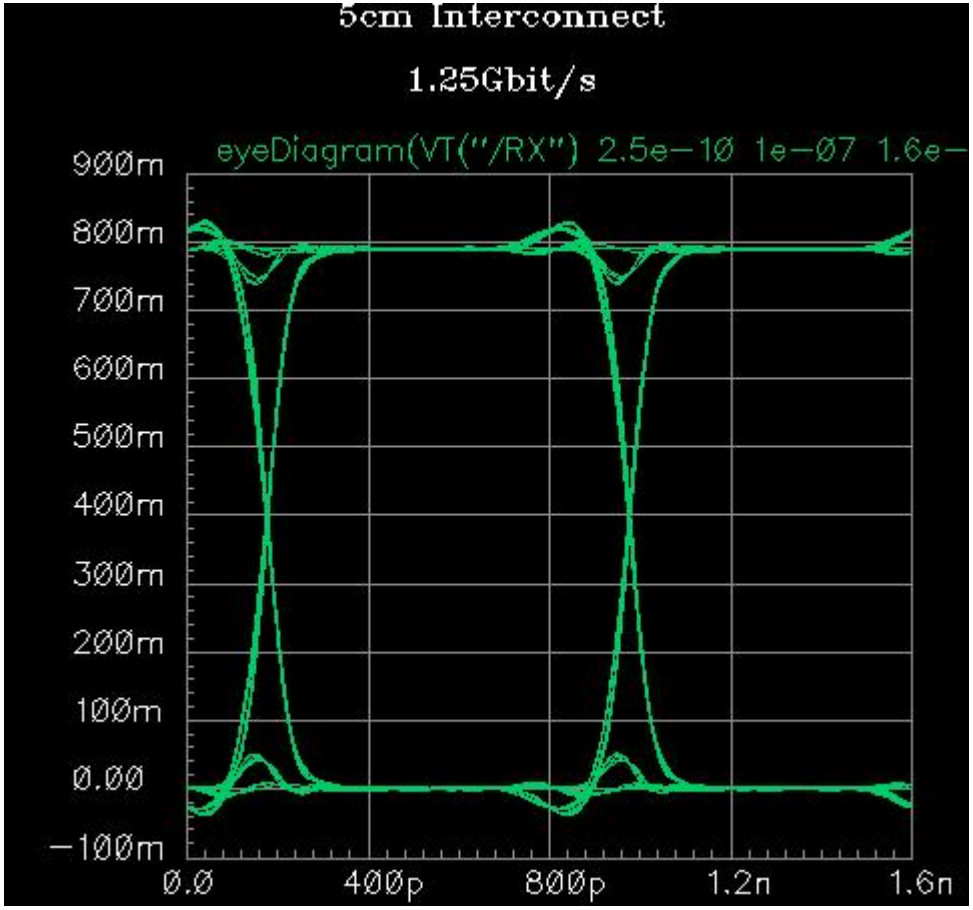
Amplitude Loss

Pattern Dependent Jitter

Simulation – 2” Length @10Gbps



Simulation – 2” Length @1Gbps



Transmission Line – ISI Calculation

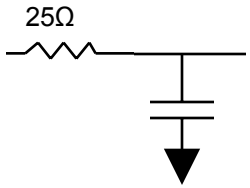
An Assumption:

Transmission line behaves as a low pass filter

For a first order model, we model only capacitance and termination resistance:

R_{eq} = 25Ω

C = 2pF



$$RC = \frac{1}{2\pi * BW}$$

$$BW = \frac{1}{RC * 2\pi}$$

$$BW = \frac{1}{25 * 2E-12 * 6.28} = 3.1GHz$$

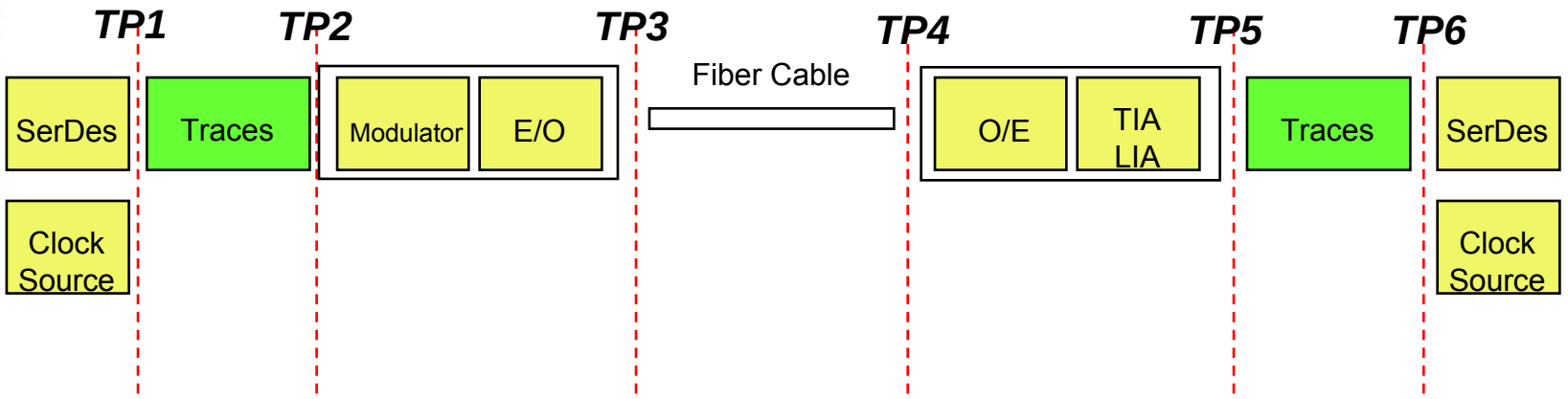
$$ISI[UI] = \frac{-\ln(1 - e^{-2\pi \cdot BWR})}{2\pi \cdot BWR} \quad = 0.087UI$$

Where:

$$BWR = \frac{\text{Bandwidth}}{\text{Baud rate}}$$

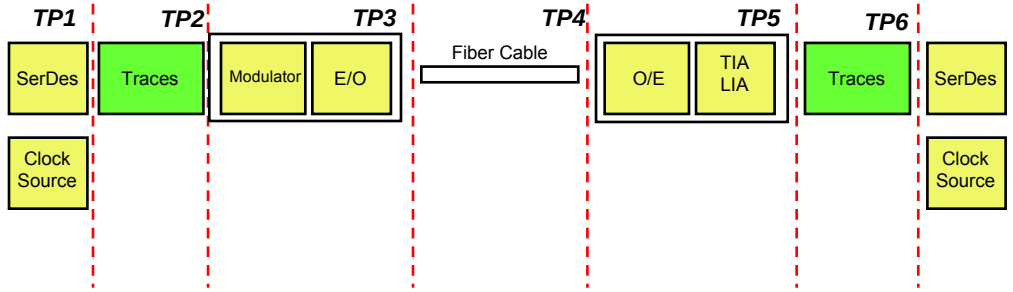
Conclusion

- We should add another 2 Jitter Test Points at the output and input of the SerDes
- Trace line is not dominated @1G, therefore, 802.3ah didn't specify dedicated test points at the I/O SerDes



Conclusion – Jitter Budget

	DS		US	
	[UI]	[PS]	[UI]	[PS]
TP1	0.10	9.7	0.20	19.4
TP2	0.25	24.2	0.35	33.9
TP3	0.43	41.7	0.45	43.6
TP4	0.80	77.6	0.55	53.5
TP5	0.90	87.3	0.75	72.7
TP6	1.05	101.8	0.90	87.3
TP6_eq	0.94	91.2	0.85	82.4



Back Up

Straw Poll #1

802.3av 10GEPON should include 6 Jitter Test Points for each direction (DS and US) as presented 3av_0803_benamram_2.pdf on slide 11.

Y: 5

N: 32

A: 23