On burst mode sync patterns and CDR performance

Frank Effenberger
Huawei Technologies Co. Ltd

The supposed issues

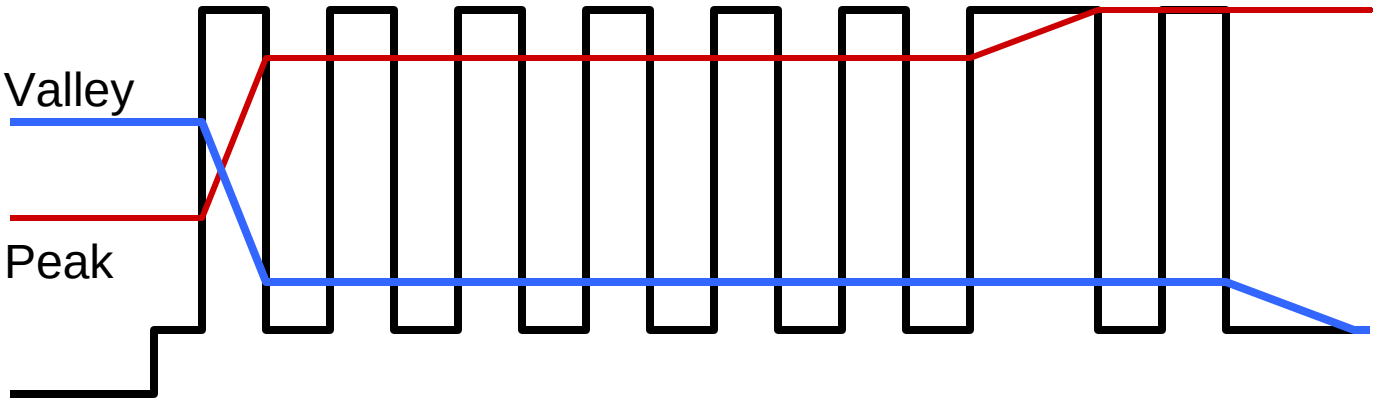
- The current sync pattern of 1010… is claimed to have some issues
  - Peak detector circuits have hard time responding to the fast pulses
  - Clock recovery circuits have a timing offset compared to random data
- We do not agree with this assessment

Fast level recovery

- There are several methods to do “fast” level recovery
  - Peak (and valley) detector
  - Gated averaging
  - Differential detection
- Only peak detection has a potential issue
  - It is clearly an issue of implementation
  - In other words, if you want to do instantaneous peak detection, then get a faster peak detector!

Peak (and valley) detection

- It should be noted that such circuits measure not only the peak, but also the valley voltage level
  - The decision threshold is then the average of the two
- Note that if the peaks are under-estimated, then the valleys will be equally over-estimated
  - The error cancels out in large part!

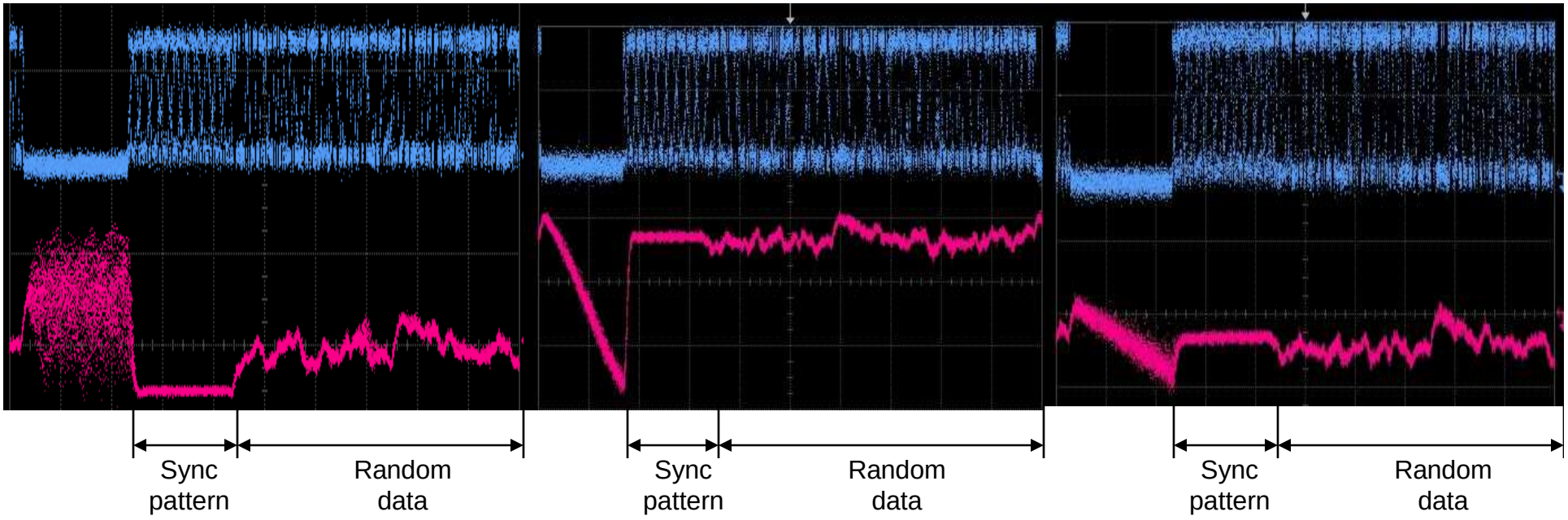


Better methods

- With a 1010 pattern, the simplest method to recover the signal level is gated averaging
  - When new burst has begun, you average 2N consecutive bits, and this gives you a very good estimate of the optimum decision threshold
- This is essentially the same as gated AC-coupling
  - When new burst has begun, you clamp the output of the AC-coupling capacitor to the decision voltage of the following comparator
- What could be simpler?
  - Why do we care about some other topologies that maybe have some implementation issues, that likely could be fixed?

Clock recovery phase offsets

- It has been pointed out that a PLL reports a different phase depending on if its input is 1010 or ‘random data’
- This is true, as the following figures show



Consider the following

- The magnitude of this phase shift is small
  - If it isn't small, then sequences of 1010 in the data will produce very bad pattern dependent clock jitter, so the system won't work
- The source of the shift is the fact that the PLL is a first order control loop (for phase)
  - The PLL phase error is proportional to the VCO frequency offset divided by the number of transitions provided by the data
  - 1010 has more transitions than random data
  - There is more negative feedback to the PLL
  - This reduces the phase error
- Given the choice, we should use the 1010 phase, since it has less error than the random data phase
  - In fact, one might be tempted to lock the phase during the burst!

Conclusions

- Very simple: There are no problems with the current sync pattern of 1010…
- This pattern enables very simple and easy level recovery
- This pattern produces the best quality clock signal

Thank you !