92.3 Extensions to PMA for 10GBASE-PR and 10/1GBASE-PRX

The 10GBASE-PR PMA is derived from the 10GBASE-R PMA defined in Clause 51. This clause specifies 10GBASE-R extensions necessary to support P2MP operation. The 10/1GBASE-PRX PMA conceptually consists of a combination of transmit and receive functions specified for 10GBASE-PR and 1000BASE-PX, as shown in Table 92-5.

Table 92-5 – Derivation of PMA transmit and receive functions for 10GBASE-PR and 10/1GBASE-PRX

PMA	Transmit Function	Receive Function
10GBASE-PR-U	As specified in Clause 51 with extensions defined in @@92.3.1@@ below.	
10/1GBASE-PRX-U	Identical to 1000BASE-PX-U. See @@65.3.1@@.	As specified in Clause 51 with extensions defined in @@92.3.1@@ below.
10GBASE-PR-D	As specified in Clause 51 with extensions defined in @@92.3.2@@ below.	
10/1GBASE-PRX-D	Identical to 10GBASE-PR-D.	Identical to 1000BASE-PX-D. See @@65.3.2@@.

92.3.1 Extensions for 10GBASE-PR-U and 10/1GBASE-PRX-U

92.3.1.1 Physical Medium Attachment (PMA) sublayer interfaces

In addition to the primitives of Clause 51, the following primitive is defined:

PMD_SIGNAL.request(tx_enable)

This primitive controls PMD emission of light. It is generated by the PCS's data detector (see 92.2.2.8.4) and the effect of its receipt is defined in 91.3.1.4. This primitive is received from the PCS and passed in timely fashion and without modification to the PMD. It takes the following parameter:

tx_enable

The tx_enable parameter can take one of two values, ON or OFF.

92.3.1.2 Loop-timing specifications for ONUs

ONUs shall operate at the same time basis as the OLT, i.e., the ONU TX clock tracks the ONU RX clock and in turn locks to OLT TX clock. Jitter transfer masks are defined in Subcause@@91.8@@.

For the 10/1GBASE-PRX-U devices, the received clock PMA_RX_CLK is 644.53125 MHz (10.3125 GBd/16), however, the transmit clock PMA_TX_CLK is 125 MHz (1.25GBd/10). The loop timing is achieved by multiplying the PMA_RX_CLK by 32 and dividing by 165.

92.3.2 Extensions for 10GBASE-PR-D

92.3.2.1 Upstream CDR lock timing measurement

CDR lock time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase and frequency lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when electrical signal after the PMD at TP4, as illustrated in Figures 91-3 and 91-4, reaches the conditions specified in @@TBD: section needs to be added to C91@@ for receiver settling time to the moment when the phase and frequency are recovered and jitter is maintained for a network with BER of no more than 10^{-3}.

A PMA instantiated in an OLT becomes synchronized at the bit level within 400 ns (T_{CDR}) and code-group level within an additional @@TBD@@ ns ($T_{code\_group\_alignment}$) with the appearance of a valid synchronization pattern (0x55…) at TP4. The combined value of measured T_{CDR} and $T_{code\_group\_alignment}$ shall not exceed @@400+TBD@@ ns.

92.3.2.1.2 Test specification

Figures 92-23 and 92-24 illustrate the tests setup for the OLT PMA receiver (upstream) T_{CDR} time. The test assumes that there is an optical PMD transmitter at the ONU with well known parameters, having a fixed known T_{ON} time as defined in @@TBD: section needs to be added to C91@@, and an optical PMD receiver at the OLT with well-known parameters, having a fixed known $T_{receiver\_settling}$ time as defined in 60.7.13.2. After T_{ON} + $T_{receiver\_settling}$ time , the parameters at TP4 reach within 15% of their steady state values.

Measure T_{CDR} as the time from the TX_ENABLE assertion, minus the known T_{ON} + $T_{receiver\_settling}$ time, to the time the electrical signal at the output of the PMA reaches up to the phase difference from the input signal of the transmitting PMA assuring BER of 10^{-3}, and maintaining its jitter specifications. The signal throughout this test is the synchronization pattern, as illustrated in Figure 92-15.

A non-rigorous way to describe this test setup would be (using a transmitter PMD at the ONU, with a known T_{ON} time and a receiver PMD at the OLT, with a known $T_{receiver\_settling}$ time):

For a tested PMA receiver with a declared T_{CDR} time, measure the phase and jitter of the recovered PMA receiver signal after T_{CDR} time from the TX_ENABLE trigger minus the reference T_{ON} + $T_{receiver\_settling}$ time, reassuring synchronization to the ONU PMA input signal and conformance to the specified steady state phase, frequency, and jitter values for BER of 10^{-3}.

Figure 92-23

Figure 92-24

92.3.3 Delay variation requirements

The MPCP relies on strict timing based on the distribution of timestamps. The actual delay is implementation dependent but an implementation shall maintain a combined delay variation through RS, PCS, and PMA sublayers of no more than 16 ns in order to comply with this mechanism.