45.2.3.29 10GBASE-PR and 10/1GBASE-PRX BER Monitor Control register (Register 3.74)

The assignment of bits in the 10GBASE-R and 10/1GBASE-PRX BER Monitor Control Register is shown in table 45-77. This register is only required when 10GBASE-PR or 10/1GBASE-PRX ONU capability is supported. The 10G-EPON BER Monitor is described in 92.2.4.1.1.1.

Bit(s)	Name	Description	R/W
3.74.0:7	10G-EPON BER Monitor Timer	Duration (in units of 5 microseconds) of the timer used by the 10G-EPON BER Monitor function Default value is 25 (ie. 125 microseconds). A value of 0 indicates that the BER monitor function is disabled.	R/W
3.74.8:15	10G-EPON BER Monitor Threshold	Number of Sync Header errors within a timer interval that triggers a high BER condition for the 10G-EPON BER Monitor function. Default value is 16. A value of 0 indicates that the BER monitor function is disabled.	R/W