Considerations for Idle Insertion

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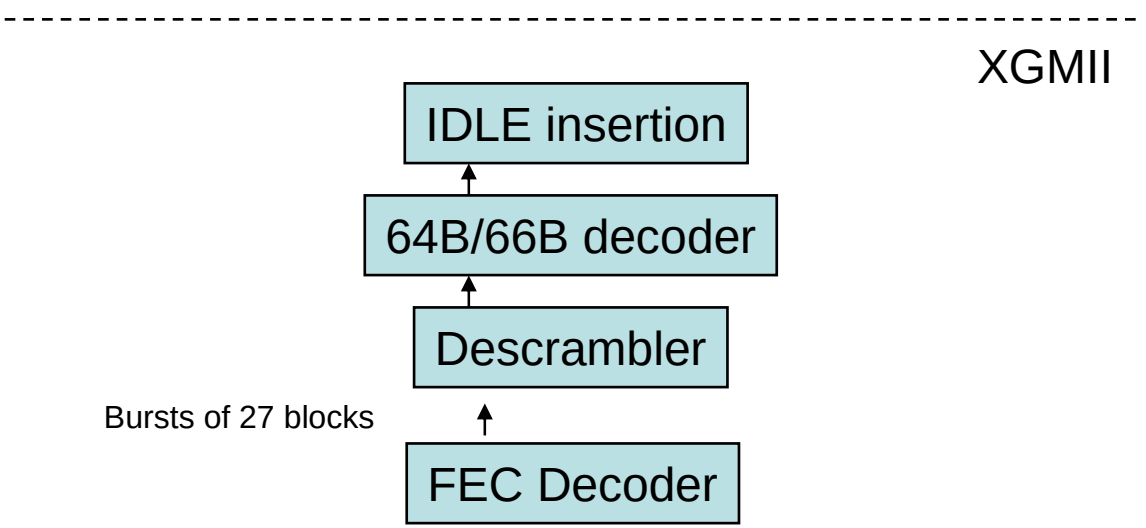
IDLE Insertion in Rx Path

1. In the current IDLE Insertion mechanism, packet latency is variable
   - Longer packets are delayed longer than shorter packets

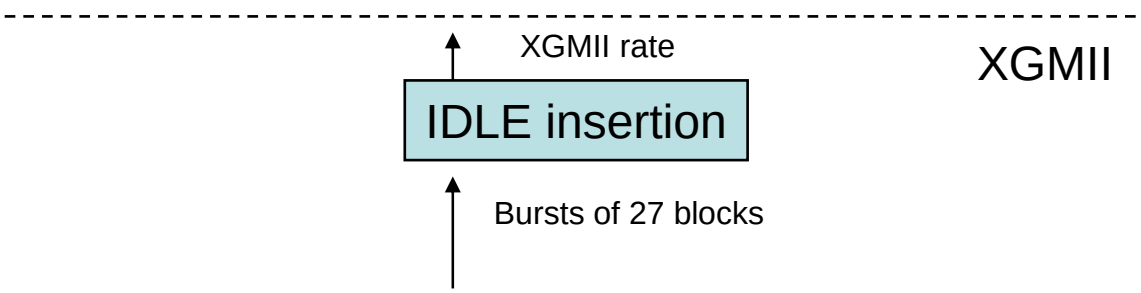
2. The remedy is to make the IDLE insertion FIFO have constant delay

Rx Data Path is Bursty



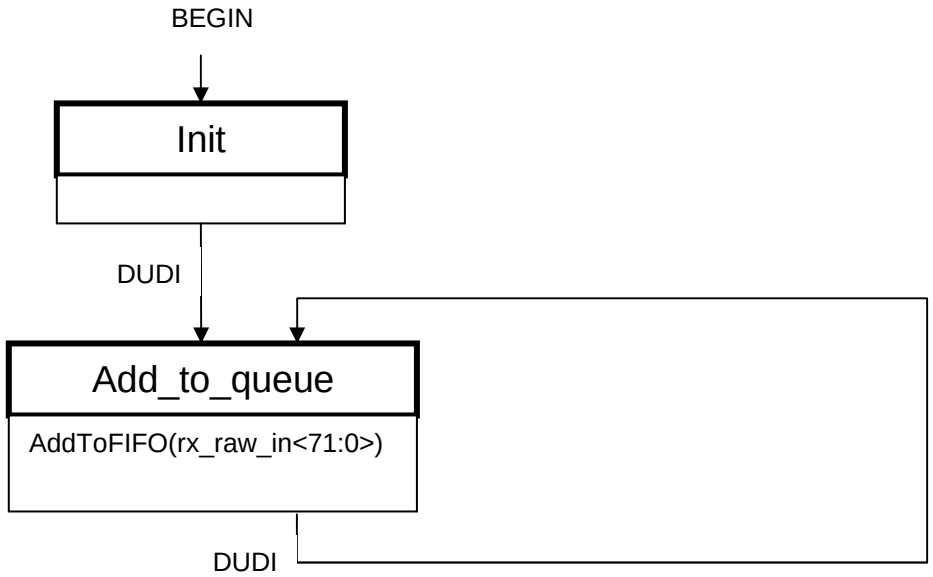
- Receive path between FEC decoder and IDLE insertion is bursty
  - FEC decoder accumulates a codeword, then sends up 27 66b blocks all at once

IDLE Insertion has bursty input and constant output



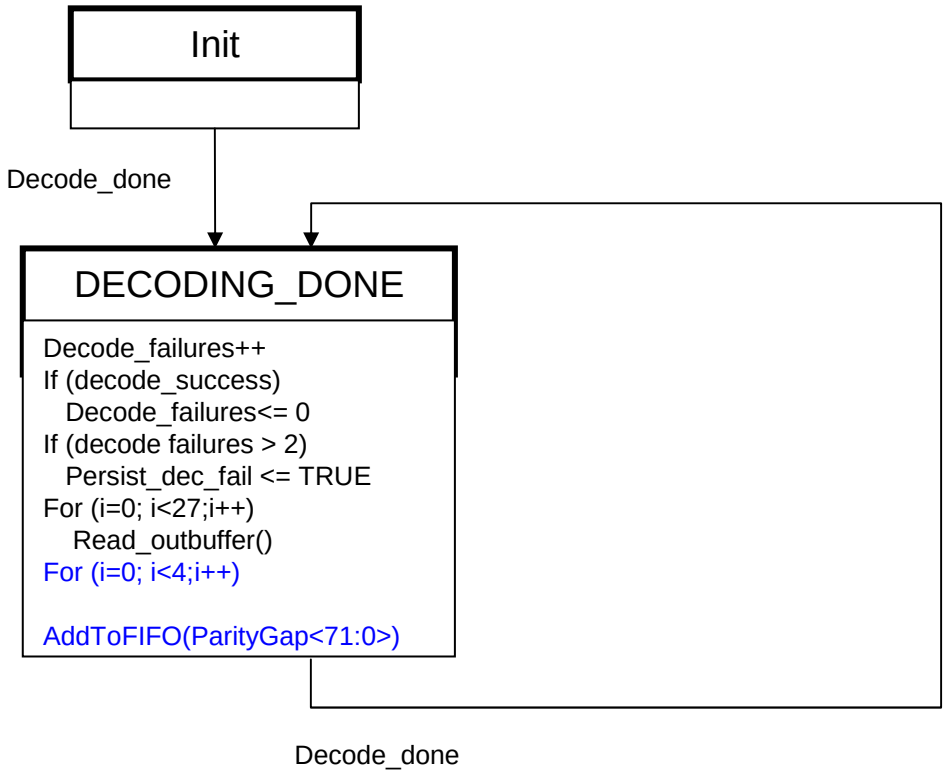
- But the 72bit XGMII vectors flow at a constant rate
- So: there must one process to write the blocks into the Idle Insertion FIFO (in bursts) and a separate process for generating the 72bit XGMII vectors when they are needed

Input Process to Idle Insertion FIFO (1)



- "DUDI" = data indication from 66b Decoder
- These occur in groups of 27 each time a FEC block is corrected

Input Process to Idle Insertion FIFO (2)



Output Process to XGMII

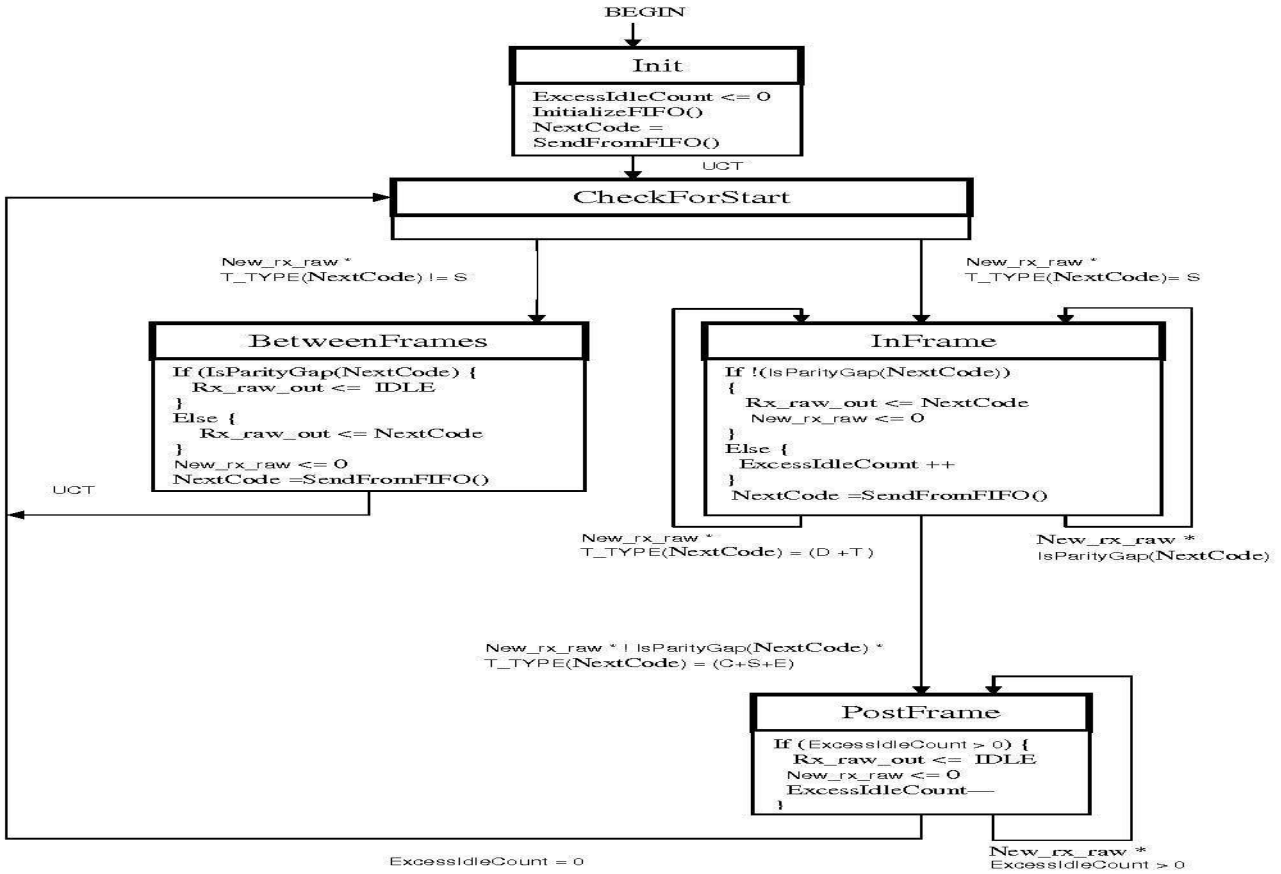


Figure 92–27 — PCS Idle Insertion, output process state diagram

Summary

1. IDLE Insertion element must perform 2 functions:
   - the actual insertion of IDLE in a manner that maintains constant packet delay
   - modifying bursty input traffic to constant rate output
     - Must have distinct input and output processes
2. A solution that performs both these functions was presented