Supplement for proposal on data-like Sync Pattern/Delimiter at May meeting

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Back Ground

Additional input is requested at May meeting.

1) What maximum run length is desired in sync pattern?
2) What is the estimated level of impairment of the current sync pattern?
3) Is there any significant reason to choose one implementation vs another?
4) If a different Sync Pattern and Delimiter is chosen with a different Hamming distance (at all shift positions) what would be the impact to FEC synchronization?
5) What is the impact on ISI equalization

1. Desired Maximum Run Length in Sync Pattern

- Peak detector circuit is widely used for TIA-AGC and LIM in a burst-mode receiver.
- Droop and bandwidth of a peak detector is in trade-off.
  - Open-loop peak detector with Bipolar Technology
    - >5GHz bandwidth
    - CID of <<64bit (several bits)
  - Closed-loop voltage peak detector
    - Almost zero-leak is available using BiCMOS.
    - A 1GHz bandwidth is now available for G-PON receiver with reasonable power dissipation.
    - A 2-2.5 GHz bandwidth is a reasonable challenging target within standardization schedule.
- Considering CID, close-loop peak detector is necessary.
- A 2-2.5 GHz bandwidth target corresponds 5-6 bits run length at 10 Gbps.

2. Estimated Level of Impairment with 1010 Sync Pattern

- We have experienced around 1dB burst power penalty due to insufficient response for 1010 preamble in early stage of G-PON burst receiver from plural vendors.
- Estimation of power penalty
  - Assumption
    - Bandwidth of peak detector : 2.5GHz
    - peak & bottom detector design for TIA-AGC and LIM
  - Gain for 1010 (5GHz)sync pattern:

    -3dB(0.7) <3dB/oct slope>
  - Power penalty: 10*log(1-(1-0.7/2)) = 1.5dB
- 1.5dB power penalty is a large impact for power budget and jitter budget.
- For CDR phase error, larger loop-gain design will tolerate the issue.

3. Implementation Method to tolerate 1010 Sync Pattern

- Using AC coupling or average detector makes burst mode receiver to tolerate 1010sync pattern.
- Maximum allowable value of $t_{RECEIVER\_SETLING}$ is 800ns and 400ns for 10 Gbps and 1.25 Gbps, respectively. But there are demands on technologies to obtain for tighter timing.
  - Tighter timing is preferable for cooperation with FSAN/ITU-T.
  - TIA-AGC with <<400ns response is necessary for 10G/1.25G Dual rate operation
- If AC coupling or average detector is used, the shorter burst-mode overhead cannot be obtained.
- The sync pattern should be allow to use a peak detector with a couple of year technology in order to make tight timing design easy.

4. Impacts on Hamming Distance(1)

- Minimum Hamming distance versus Sync Pattern/Delimiter

	Sync Pattern	Delimiter	Minimum Humming Distance
(1)	1010	D1.3	32
(2)	3av_nagahori_0805_1.pdf		30
(3)	3av_effenberger_0807_1.pdf		30

Impacts on FEC synchronization is calculated in the next slide.

4. Impacts on Hamming Distance(2)

Probability of Lost Burst $< {}_{66}C_{t+1}\ p^{t+1}$

Probability of False Lock $< N\ {}_{66}C_{d-t}\ p^{d-t}$

Input BER : p,
Sync Pattern Length : $N(< 10^4$ (up to a micro second))
Minimum Hamming distance: d,
Number of tolerant errors in correlation search: t $(< d/2)$

p	d=32, t=13		d=30, t=12	
	Upper Bounds of Prob. Lost Burst	Prob. False Lock	Upper Bounds of Prob. Lost Burst	Prob. False Lock
0.001	7.7e-29	1.7e-37	2.0e-26	6.8e-35
0.005	4.7e-19	3.3e-24	2.4e-17	2.6e-22
0.01	7.7e-15	1.7e-18	2.0e-13	6.8e-17

By reducing the minimum Hamming distance from 32 to 30, probability of Lost Burst and False Lock enlarges slightly. But the enlargement can be an allowable level in practical use.

5. Impact on ISI

- Using an equalizer to equalize ISI is expected to improve jitter/loss budget with a tight spec.
- An ISI equalizer requires flat-spectrum pattern in order to train-on.
- 1010 sync pattern cannot be used to train-on.
- A 22bit data-like sync pattern improves the drawback of 1010 sync pattern.
- A 66bit data-like sync pattern is more likely than 22bit data-like pattern in flatness of spectrum.

6. Impact on Burst CDR Lock Time

- By using data-like sync pattern, number of edge in t_{CDR} reduce by a factor of approximately 0.5. This enlarges the CDR lock time by a factor of approximately 2.
- Even if data-like sync pattern is applied, there are still 7 times larger number of edges in t_{CDR} compared with 802.3ah system. Therefore the impact to CDR lock-time is not severe in implementation of 802.3av system.

Sync Pattern	# of rise/fall edge in 400ns
1010	4000
3av_nagahori_0805_1.pdf	2200
3av_effenberger_0807_1.pdf	2100
802.3ah	300

Summary

- Using a data-like sync pattern with maxim run length of several bit is preferable in implementation of a burst-mode receiver.
- 66bit interval pattern is superior in maximum run-length and flatness of spectrum.

22bit pattern
Binary 1 0011111010 1100000101 0
Hex 4 BE 06 95 AF 41 E5 6B 50

66bit pattern
Binary 10 1111 1101 0000 0010 0001 1000 1010 0111
1010 0011 1001 0010 1101 1101 1001 1010
Hex 4 BF 40 18 E5 C5 49 BB 59