45.2.3.30 10GBASE-PR and 10/1GBASE-PRX BER Monitor Status (Register 3.75)

The assignments of bits in the 10GBASE-PR and 10/1GBASE-PRX BER Status Register is shown in Table 45-76. This register is only required when 10GBASE-PR or 10/1GBASE-PRX ONU capability is supported.

Table 45-76 – PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W
3.75.7:2	Reserved	Value always zero, writes ignored	RO
3.75.1	Latched high	1 = 10GBASE-PR or 10GBASE PRX <u>10/1GBASE-PRX</u> PCS reported a	RO/NR
	BER	high BER.	
		<u>1-0</u> = 10GBASE-PR or <u>10GBASE-PRX</u> 10/1GBASE-PRX PCS did not	
		report a high BER.	
3.75.0	High BER	1 = 10GBASE-PR or 10GBASE PRX <u>10/1GBASE-PRX</u> PCS reporting a	RO
		high BER.	
		$0 = 10$ GBASE-PR or $\frac{10$ GBASE PRX $\frac{10}{1}$ GBASE-PRX $\frac{10}{1}$ PCS not	
		reporting a high BER.	

45.2.3.30.1 10GBASE-PR and 10GBASE-PRX10/1GBASE-PRX PCS high BER (3.75.0)

For In 10GBASE-PR and 10/1GBASE-PRX PCS, when read as a one, bit 3.*75.*0 indicates that the receiver is detecting a BER greater than the configurable threshold. of When read as a zero, bit 3.*75.*0 indicates that the receiver is detecting a BER of lower than the configurable threshold. This bit mirrors is a direct reflection of the state of the hi_ber variable, in the state diagram that is defined in 76.2.3.4.

45.2.3.30.2 10GBASE-PR and 10GBASE-PRX10/1GBASE-PRX PCS latched high BER (3.75.1)

In 10GBASE-PR and 10/1GBASE-PRX PCS, When when read as a one, bit 3.*75.*1 indicates that the receiver detected that the 10GBASE PR or the 10GBASE PRX PCS has detected a high BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.*75.*1 indicates that the receiver detected BER lower than the configurable threshold (low BER state). 10GBASE R or the 10GBASE T PCS has not detected a high BER.

The latched high BER shall be implemented with latching high behavior.

This bit is a latching high version of the 10GBASE-PR and 10/1GBASE-PRX high BER status bit (3.75.0).

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