[Add new entries to table 45-82:]

3.75 10GBASE-PR and 10/1GBASE-PRX FEC ability register
3.76 10GBASE-PR and 10/1GBASE-PRX FEC control register
3.77, 3.78 10/1GBASE-PRX and 10GBASE-PR corrected FEC blocks counter
3.79 3.80 10/1GBASE-PRX and 10GBASE-PR uncorrected FEC blocks counter
3.81 thgough 3.32 767 Reserved

45.2.3.30 10GBASE-PR and 10/1GBASE-PRX FEC ability register (Register 3.75)

The assignment of bits in the 10GBASE-PR and 10/1GBASE-PRX FEC ability register is shown in Table 45–110.

Table 45-110 10GBASE-PR and 10/1GBASE-PRX FEC ability register bit definitions

Bit(s)	Name	Description	R/W*
3.75.15:2	Reserved	Value always zero, Writes ignored	R/0
3.75.1	FEC error indication ability	A read of 1 in this bit indicates whether the 10Gb/s FEC decoder component of the 10/1GBASE-PRX or 10GBASE-PR PCS is able to indicate decoding errors to higher layers. In a 10/1GBASE-PRX OLT, this bit is undefined.	R/0
3.75.0	10 Gb/s FEC ability	This bit always reads as one, to indicate that the 10/1GBASE-PRX or 10GBASE-PR PCS supports 10 Gb/s FEC	R/0

*RO readonly

45.2.3.30.1 10Gb/s FEC ability (3.75.0)

This bit indicates that the 10GBASE-PR PCS or the downstream transmitter/receiver component of the 10/1GBASE-PRX supports 10Gb/s forward error correction. The bit always reads as one.

The register describing ability to perform forward error correction in the 10/1GBASE-PRX upstream is specified in subclause 45.2.7.2.

45.2.3.30.2 FEC error indication ability (3.75.1),

When read as a one, this bit indicates that the 10 Gb/s FEC decoder is able to indicate decoding errors to the higher layers (see Subclause 76.2.2.3). When read as a zero, the FEC decoder is not able to indicate decoding errors to the higher layers. FEC error indication is controlled by a bit in the 10GBASE-PR and 10/1GBASE-PRX FEC control register (see subclause 45.2.3.31.2).

45.2.3.31 10GBASE-PR and 10/1GBASE-PRX FEC control register (Register 3.76)

The assignment of bits in the 10GBASE-PR FEC control register is shown in Table 45–111.

Table 45-111 10GBASE-PR and 10/1GBASE-PRX FEC control register bit definitions

Bit(s)	Name	Description	R/W*
3.76.15:2	Reserved	Value always zero, Writes ignored	R/0
3.76.1	enable FEC error indication	A write of 1 to this bit configures the 10 Gb/s FEC decoder to indicate uncorrectable codeword errors to the higher layer. In a 10/1GBASE-PRX OLT, this bit is undefined.	R/W
3.76.0	10 Gb/s FEC enable	Always reads as 1 since 10 Gb/s FEC is always enabled	R/0

*RO readonly

45.2.3.31.1 FEC enable error indication (3.76.1)

This bit instructs the 10Gb/s FEC decoder component of the 10GBASE-PR and 10/1GBASE-PRX PCS indicate decoding errors to the upper layers (see subclause 45.2.3.30 and subclause 76.2.3.3).

When written as a one, the receiving PCS replaces 66B blocks received in uncorrectable FEC codewords with /E/ (ie. error codes). As a consequence, the receiving MAC discards any packet which includes data that was received in an uncorrectable FEC codeword (even though the packet itself might or might not contain errors).

When written as a zero, the receiving PCS does not modify 66B blocks received in uncorrectable FEC codewords. As a consequence, the receiving MAC performs regular processing on a packet that includes data that was received in an uncorrectable FEC codeword (though the packet itself may contain errors which might or might not be detected by the MAC FCS)

45.2.3.31.2 10 Gb/s FEC Enable (3.76.0)

This bit indicates whether 10 Gb/s FEC is enabled in the 10GBASE-PR and 10/1GBASE-PRX PCS and always reads as one.

The register describing ability to enable forward error correction in the 10/1GBASE-PRX upstream is specified in subclause 45.2.7.3.

45.2.3.32 10/1GBASE-PRX and 10GBASE-PR corrected FEC blocks counter (Register 3.77, 3.78)

The assignment of bits in the 10/1GBASE-PRX and 10GBASE-PR FEC corrected blocks counter register is shown in Table 45–112. See subclause 76.2.3.3.2 for a definition of this counter. These bits shall be reset to all zeroes when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–112—10GBASE-PR FEC corrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W*
3.77.15:0	FEC corrected blocks lower	FEC_corrected_blocks_counter[15:0]	RO, MW
3.78.15:0	FEC corrected blocks upper	FEC_corrected_blocks_counter[31:16]	RO, MW

*RO = Read only, MW = Multi-Word

45.2.3.33 10GBASE-PR FEC and 10/1GBASE-PRX uncorrected FEC blocks counter (Register 3.79, 3.80)

The assignment of bits in the 10/1GBASE-PRX and 10GBASE-PR FEC uncorrected blocks counter register is shown in Table 45–113. See subclause 76.2.3.3.2 for a definition of this counter. These bits shall be reset to all zeroes when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–113—10GBASE-PR FEC uncorrected blocks counter register bit definitions

Bit(s)	Name	Description	R/W*
3.79.15:0	FEC uncorrected blocks lower	FEC_uncorrected_blocks_counter[15:0]	RO, MW
3.80.15:0	FEC uncorrected blocks upper	FEC_uncorrected_blocks_counter[31:16]	RO, MW

*RO = Read only, MW = Multi-Word