**Move BURST_DELIMITER & SP to varaibles as shown below.**

**76.2.2.5.2 Variables**

BURST_DELIMITER

TYPE: 66-bit unsigned

A 66-bit value used to find the beginning of the first FEC codeword in the upstream burst.

Default Value: 0x 8 6B F8 D8 12 D8 58 E4 AB (transmission bit sequence: 01 1101 0110 0001 1111 0001 1011 0100 1000 0001 1011 0001 1010 0010 0111 1101 0101)

SP

Type: 66-bit unsigned

A 66-bit value used to for the burst mode synchronization pattern.

Default Value: 0x 4 BF 40 18 E5 C5 49 BB 59 (transmission bit sequence 10 1111 1101 0000 0010 0001 1000 1010 0111 1010 0011 1001 0010 1101 1101 1001 1010)

**Modify Figure 77-31 in subclause 77.3.6.1 GATE description**

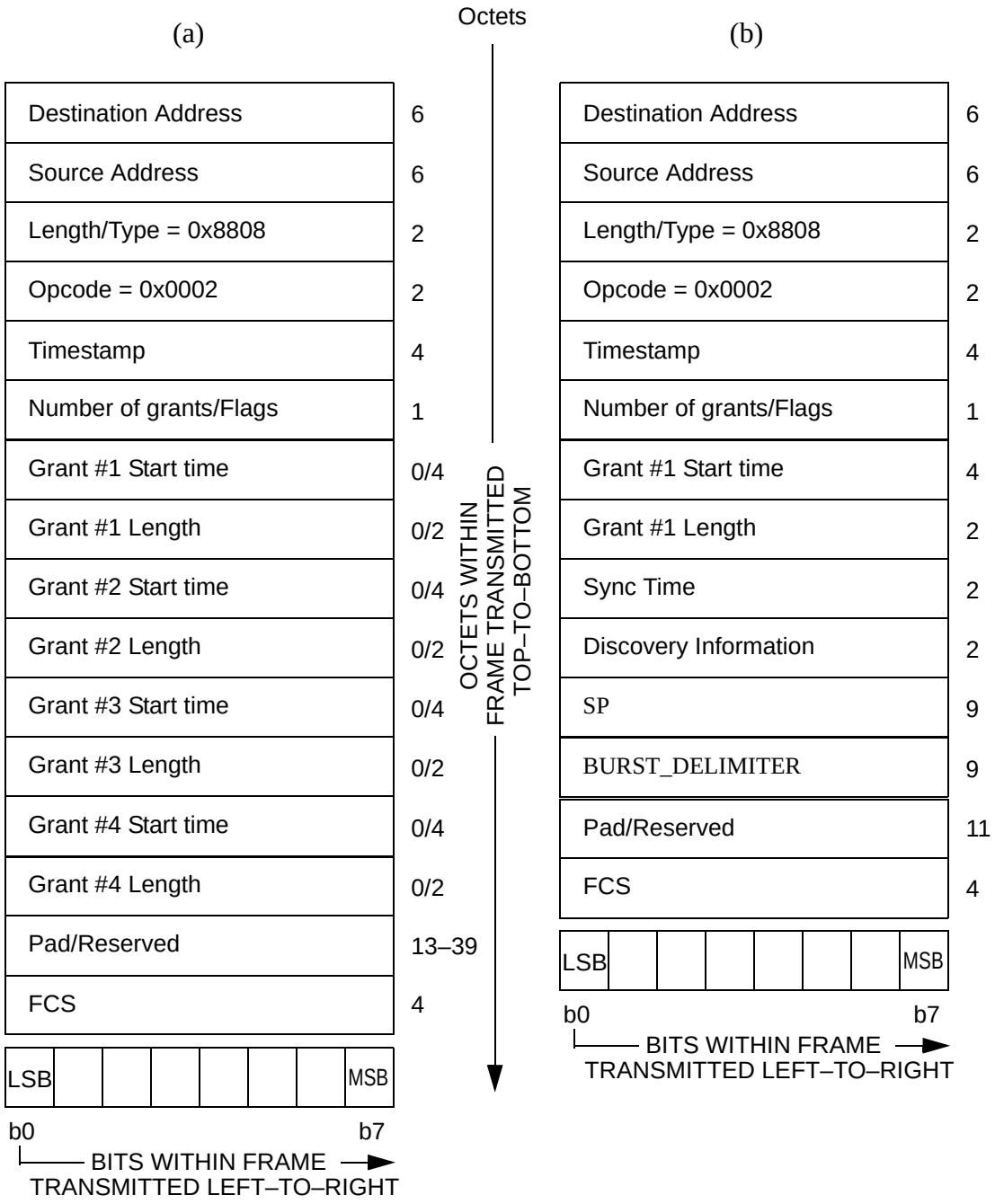


**Figure 77–31—GATE MPCPDU: (a) normal GATE MPCPDU, (b) discovery GATE MPCPDU**

**Add tables describing SP and BURST_DELIMITER to subclause 77.3.6.1 GATE description.**

**Table 77–xx—GATE MPCPDU SP Fields**

| Bit | Values |
|---|---|
| 0-65 | Sync pattern to be used in the upstream direction. |
| 66-71 | Ignored on reception. |

**Table 77–yy—GATE MPCPDU BURST_DELIMITER Fields**

| Bit | Values |
|---|---|
| 0-65 | BURST_DELIMTER to be used in the upstream direction. |
| 66-71 | Ignored on reception. |

**Add Management Register to Clause 45.**

***Change last rows of Table 45-82:***

| Register address | Register name |
|---|---|
| 3.74 | 10GBASE-PR and 10/1GBASE-PRX Clause 76 BER Monitor Control |
| 3.75 through 3.79 | 10GBASE-PR SP (Sync Pattern) |
| 3.80 through 3.84 | 10GBASE-PR BURST_DELIMITER |
| ~~3.74~~ 3.84 thgough 3.32 767 | Reserved |
| 3.32 768 through 3.65 535 | Vendor specific |

**Add after instructions to insert subclause 45.2.3.29**

### 45.2.3.30 10GBASE-PR SP register (Register 3.75 through 3.79)

The assignment of bits in the 10GBASE-PR SP Register is shown in @@ Table 45-78@@. This register is only required when 10GBASE-PR capability is supported. The 10G-EPON SP is described in @@Subclause 76.2.2.5@@

**Table 45–78—10GBASE-PR SP register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.79.15:2 | Reserved | Value always 0, writes ignored | R/W |
| 3.79.1:0 | SP word 4 | SP bits 65-66 | R/W |
| 3.78.15:0 | SP word 3 | SP bits 48-63 | R/W |
| 3.77.15:0 | SP word 2 | SP bits 32-47 | R/W |
| 3.76.15:0 | SP word 1 | SP bits 16-31 | R/W |
| 3.75.15:0 | SP word 0 | SP bits 0-15 | R/W |

a.R/W = Read/Write

### 45.2.3.31 10GBASE-PR BURST_DELIMITER register (Register 3.80 through 3.84)

The assignment of bits in the 10GBASE-PR BURST_DELIMITER Register is shown in @@ Table 45-79@@. This register is only required when 10GBASE-PR capability is supported. The 10G-EPON BURST_DELIMITER is described in @@Subclause 76.2.2.5@@

**Table 45–79—10GBASE-PR BURST_DELIMITER register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.84.15:2 | Reserved | Value always 0, writes ignored | R/W |
| 3.84.1:0 | BURST_DELIMITER word 4 | BURST_DELIMITER bits 65-66 | R/W |
| 3.83.15:0 | BURST_DELIMITER word 3 | BURST_DELIMITER bits 48-63 | R/W |
| 3.82.15:0 | BURST_DELIMITER word 2 | BURST_DELIMITER bits 32-47 | R/W |
| 3.81.15:0 | BURST_DELIMITER word 1 | BURST_DELIMITER bits 16-31 | R/W |
| 3.80.15:0 | BURST_DELIMITER word 0 | BURST_DELIMITER bits 0-15 | R/W |

a.R/W = Read/Write