75.5.16 Receiver settling timing measurement

75.5.16.1 Definitions

Denote $T_{receiver\_settling}$ as the time beginning from the time that the optical power in the receiver at TP3 reaches the conditions specified in 38.6.11, 58.7.11.2 and ending at the time that the electrical signal after the PMD at TP4, reaches within 15% of its steady state parameter, (average power, jitter), see Table 75-6 for 10GBASE-PR-D1, 10GBASE-PR-D2 and 10GBASE-PR-D3, and Table 75-7 for 10/1GBASE-PRX-D1, 10/1GBASE-PRX-D2 and 10/1GBASE-PRX-D3. $T_{receiver\_settling}$ is presented in Figure 75–9. The data transmitted may be any valid 64B/66B symbols (or a specific power synchronization sequence). The optical signal at TP3, at the beginning of the locking, may have any valid 64B/66B pattern, optical power level, jitter, or frequency shift matching the standard specifications.

75.5.16.2 Test specification

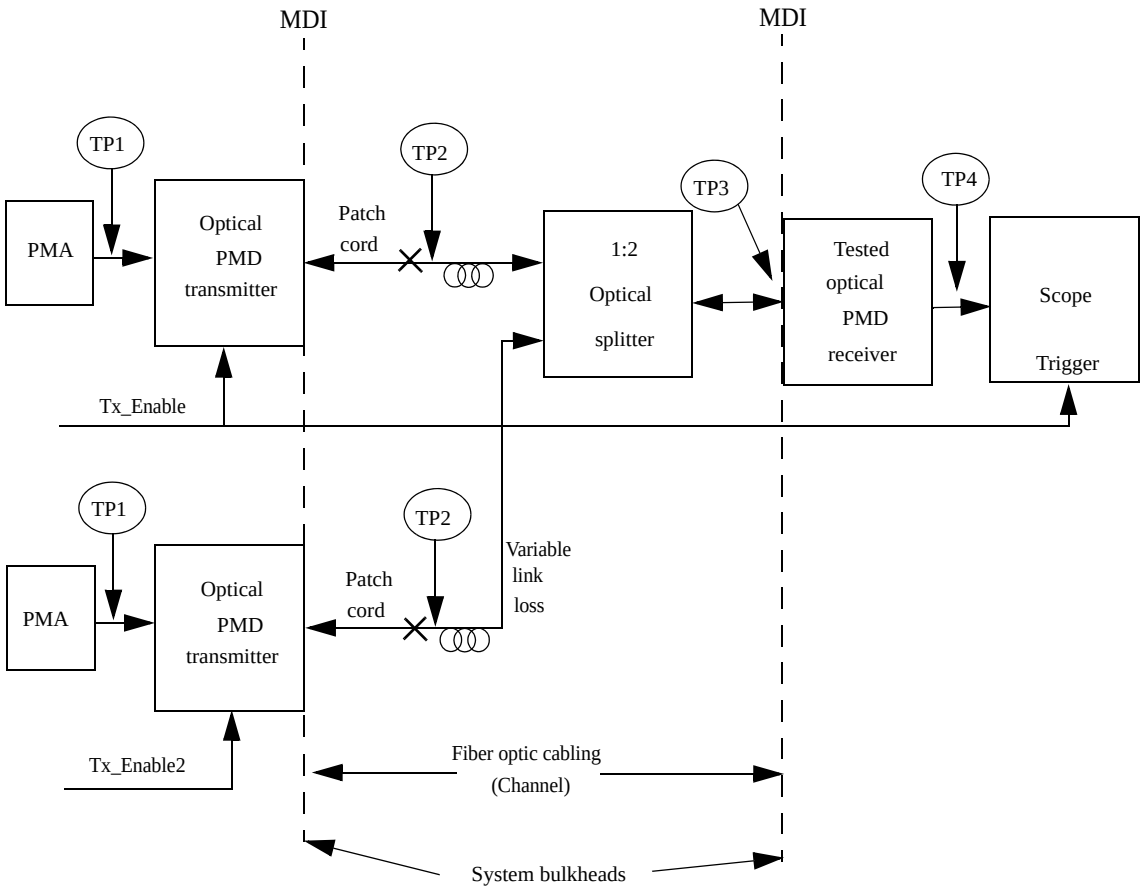

Figure 75–9—Receiver settling time measurement setup

Figure 75–9 illustrates the test setup for the OLT PMD receiver (upstream) $T_{receiver\_settling}$ time. The optical PMD transmitter has well-known parameters, with a fixed known T_{on} time. After T_{on} time the parameters of the reference transmitter, at TP2 and therefore at TP3, reach within 15% of its steady state values as specified in Table 75-8 for 10GBASE-PR-U1 and 10GBASE-PR-U3 and Table 75-9 for 10/1GBASE-PRX-U1, 10/1GBASE-PRX-U2 and 10/1GBASE-PRX-U3.

Define $T_{receiver\_settling}$ time as the time from the Tx_Enable assertion, minus the known T_{on} time, to the time the electrical signal at TP4 reaches within 15% of its steady state conditions.