45.2.3 PCS registers

Change last rows of Table 45-82:

Register address	Register name
3.74	~~10GBASE-PR and 10~~10 Gb/~~1GBASE-PRX~~ s FEC ability register
3.75	~~10GBASE-PR and 10~~10 Gb/~~1GBASE-PRX~~ s FEC control register
3.76, 3.77	~~10~~Corrected 10 Gb/~~1GBASE-PRX and 10GBASE-PR corrected~~ s FEC codewords counter
3.78, 3.79	~~10~~Uncorrected 10 Gb/~~1GBASE-PRX and 10GBASE-PR uncorrected~~ s FEC codewords counter
3.80	~~10GBASE-PR and 10/1GBASE-PRX BER Monitor Control~~ BER monitor control
3.81	~~10GBASE-PR and 10/1GBASE-PRX BER Monitor Status~~ BER monitor status
~~3.74~~ 3.82 through 3.32 767	Reserved
3.32 768 through 3.65 535	Vendor specific

Change row 8 (not including header) of Table 45-83 as follows:

3.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved x x 1 ~~x~~1 = Reserved 0 0 1 0 = 10/1 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W

Insert after subclause 45.2.3.28 10P/2B PAF lost ends of fragments register (Register 3.73):

45.2.3.29 ~~10GBASE-PR and 10~~10 Gb/~~1GBASE-PRX~~ s FEC ability register (Register 3.74)

The assignment of bits in the ~~10GBASE-PR and 10~~10 Gb/~~1GBASE-PRX~~ s FEC ability register is shown in Table 45–107.

Table 45–107—~~10GBASE-PR and 10~~10 Gb/~~1GBASE-PRX~~ s FEC ability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.74.15:2	Reserved	Value always zero, writes ignored	RO
3.74.1	10 Gb/s FEC error indication ability	A read of 1 in this bit indicates that the 10 Gb/s FEC decoder component of the ~~10/1GBASE-PRX or 10GBASE-PR~~ PCS is able to indicate decoding errors to higher layers~~. In a 10/1GBASE-PRX OLT, this bit is undefined~~.	RO
3.74.0	10 Gb/s FEC ability	~~This~~ A read of 1 in this bit indicates that the PCS supports the ~~10/1GBASE-PRX or 10GBASE-PR~~ 10 Gb/s FEC ~~(mandatory~~ defined in 76.3. This bit always reads as 1 for 10/1GBASE-PRX or 10GBASE-PR~~)~~.	RO

[a]RO = Read only

45.2.3.29.1 10 Gb/s FEC error indication ability (3.74.1)

When read as a one, this bit indicates that the 10 Gb/s FEC decoder component of the ~~10GBASE-PR or 10/1GBASE-PRX~~ PCS is able to indicate decoding errors to the higher layers (see 76.3.3.3). When read as a zero, the FEC decoder is not able to indicate decoding errors to the higher layers. FEC error indication is controlled by a bit in the ~~10GBASE-PR and 10~~10 Gb/~~1GBASE-PRX~~ s FEC control register (see 45.2.3.31.2).

45.2.3.29.2 10 Gb/s FEC ability (3.74.0)

This bit indicates that the ~~10GBASE-PR PCS or the downstream~~ transmitter/receiver component of the ~~10/1GBASE-PRX~~ PCS supports 10 Gb/s forward error correction. The bit always reads as one for ~~10~~a PCS in which 10 Gb/~~1GBASE-PRX or 10GBASE-PR~~s FEC is mandatory. The register describing the ability to perform forward error correction in the ~~10/1GBASE-PRX upstream~~ receive direction is specified in 45.2.~~7~~8.2.

45.2.3.30 ~~10GBASE-PR and 10~~10 Gb/~~1GBASE-PRX~~ s FEC control register (Register 3.75)

The assignment of bits in the ~~10GBASE-PR~~ 10 Gb/s FEC control register is shown in Table 45–108.

Table 45–108—~~10GBASE-PR and 10~~10 Gb/~~1GBASE-PRX~~ s FEC control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.75.15:2	Reserved	Value always zero, Writes ignored	RO
3.75.1	enable 10 Gb/s FEC error indication	A write of 1 to this bit configures the 10 Gb/s FEC decoder to indicate uncorrectable codeword errors to the higher layer. In a ~~10~~PCS which does not support 10 Gb/~~1GBASE-PRX OLT~~s FEC, this bit is undefined.	R/W
3.75.0	10 Gb/s FEC enable	Always reads as 1 for ~~10/1GBASE-PRX or 10GBASE-PR since~~ a PCS in which 10 Gb/s FEC is ~~always enabled~~mandatory	RO

[a]RO read only, R/W read write

45.2.3.30.1 10 Gb/s FEC enable error indication (3.75.1)

This bit instructs the 10 Gb/s FEC decoder component of the ~~10GBASE-PR and 10/1GBASE-PRX~~ PCS to indicate decoding errors to the upper layers (see 45.2.3.30 and 76.3.3.3).

When written as a one, the receiving PCS invalidates 66-bit blocks received in uncorrectable FEC codewords. As a consequence, the receiving MAC discards any packet which includes data that was received in an uncorrectable FEC codeword (even though the packet itself might or might not contain errors).

When written as a zero, the receiving PCS does not modify 66-bit blocks received in uncorrectable FEC codewords. As a consequence, the receiving MAC performs regular processing on a packet that includes

data that was received in an uncorrectable FEC codeword (though the packet itself may contain errors which ~~might~~ may or ~~might~~ may not be detected by the MAC FCS).

If 10 Gb/s FEC error indication ability in 3.47.1 reads 0, then a read of this bit will return 0 and writes are ignored.

45.2.3.30.2 10 Gb/s FEC Enable (3.75.0)

~~This bit indicates whether 10 Gb/s FEC is enabled in the 10GBASE-PR and 10/1GBASE-PRX PCS and always reads as one.~~

This bit indicates whether 10 Gb/s FEC is enabled in the PCS and always reads as one for a 10 Gb/s PCS in which FEC support is mandatory.

The register ~~describing ability to enable~~ for enabling and disabling forward error correction in the 10/1GBASE-PRX upstream is specified in 45.2.~~7~~8.3.

45.2.3.31 ~~10GBASE-PR and 10~~Corrected 10 Gb/~~1GBASE-PRX corrected~~ s FEC codewords counter (Register 3.76, 3.77)

The assignment of bits in the ~~10~~Corrected 10 Gb/~~1GBASE-PRX and 10GBASE-PR corrected~~ s FEC codewords counter register is shown in Table 45–109. See ~~76.3.3.1.2~~ 76.3.3.3.2 for a definition of this counter. These bits shall be reset to all zeroes when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–109—~~10GBASE-PR corrected~~ Corrected 10 Gb/s FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.76.15:0	corrected 10 Gb/s FEC codewords lower	~~corrected_FEC_codewords_counter~~corrected_10_Gb/s_FEC_codewords_counter[15:0]	RO, MW, NR
3.77.15:0	corrected 10 Gb/s FEC codewords upper	~~corrected_FEC_codewords_counter~~corrected_10_Gb/s_FEC_codewords_counter[31:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.32 ~~10GBASE-PR FEC and 10~~Uncorrected 10 Gb/~~1GBASE-PRX uncorrected~~ s FEC codewords counter (Register 3.78, 3.79)

The assignment of bits in the ~~10~~Uncorrected 10 Gb/~~1GBASE-PRX and 10GBASE-PR~~ s FEC ~~uncorrected~~ codewords counter register is shown in Table 45–110. See ~~76.3.3.1.2~~ 76.3.3.3.2 for a definition of this

counter. These bits shall be reset to all zeroes when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

Table 45–110—~~10GBASE-PR uncorrected~~ Uncorrected 10 Gb/s FEC codewords counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.78.15:0	uncorrected 10 Gb/s FEC code-words lower	~~uncorrected_FEC_codewords_counter~~uncorrected_10_Gb/s_FEC_codewords_counter[15:0]	RO, MW, NR
3.79.15:0	uncorrected 10 Gb/s FEC code-words lower	~~uncorrected_FEC_codewords_counter~~uncorrected_10_Gb/s_FEC_codewords_counter[32:16]	RO, MW, NR

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

45.2.3.33 10GBASE-PR and 10/1GBASE-PRX BER ~~Monitor Control~~ monitor control register (Register 3.80)

The assignment of bits in the 10GBASE-PR and 10/1GBASE-PRX BER ~~Monitor Control Register~~ monitor control register is shown in Table 45–111. This register is only required when 10GBASE-PR or 10/1GBASE-PRX ONU capability is supported. The 10G-EPON BER ~~Monitor~~ monitor is described in 76.3.3.4.

Table 45–111—10GBASE-PR and 10/1GBASE-PRX BER ~~Monitor Control~~ monitor control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.80.~~0~~8:~~7~~15	10G-EPON BER Monitor ~~Timer~~Threshold	~~Duration (in units~~ Number of ~~5 microseconds) of the~~ Sync Header errors within a timer ~~used by~~ interval that triggers a high BER condition for the 10G-EPON BER ~~Monitor function~~ monitor function. Default value is ~~25 (ie~~16. ~~125 microseconds).~~ A value of 0 indicates that the BER monitor function is disabled.	R/W
3.80.~~8~~0:~~1~~57	10G-EPON BER Monitor ~~Threshold~~ Timer	~~Number~~ Duration (in units of 5 microseconds) of ~~Sync Header errors within a~~ the timer ~~interval that triggers a high BER condition for~~ used by the 10G-EPON BER ~~Monitor~~ monitor function. Default value is ~~16~~25 (ie. 125 microseconds). A value of 0 indicates that the BER monitor function is disabled~~.~~	R/W

[a]R/W = Read/Write

45.2.3.34 10GBASE-PR and 10/1GBASE-PRX BER ~~Monitor Status~~ monitor status (Register 3.81)

The assignments of bits in the 10GBASE-PR and 10/1GBASE-PRX BER ~~Status Register~~ status register is shown in Table 45–112. This register is only required when 10GBASE-PR or 10/1GBASE-PRX ONU capability is supported.

Table 45–112—10GBASE-PR and 10/1GBASE-PRX BER ~~Monitor Status~~ monitor status Register

Bit(s)	Name	Description	R/W[a]
3.81.7:2	Reserved	Value always zero, Writes ignored	RO
3.81.1	Latched high BER	1 = 10GBASE-PR or 10/1GBASE-PRX PCS reported a high BER. 0 = 10GBASE-PR or 10/1GBASE-PRX PCS did not report a high BER.	RO, LH
3.81.0	high BER	1 = 10GBASE-PR or 10/1GBASE-PRX PCS reporting a high BER. 0 = 10GBASE-PR or 10/1GBASE-PRX PCS not reportiong a high BER.	RO

[a]RO read only, LH = Latching high

45.2.3.34.1 10GBASE-PR and 10/1GBASE-PRX PCS high BER (3.81.0)

In the 10GBASE-PR and 10/1GBASE-PRX PCS, when read as a one, bit 3.81.0 indicates that the receiver is detecting a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.0 indicates that the receiver is detecting a BER lower than the configurable threshold (low BER state). This bit mirrors the state of the hi_ber variable, defined in 76.3.3.4.

45.2.3.34.2 10GBASE-PR and 10/1GBASE-PRX PCS latched high BER (3.81.1)

In the 10GBASE-PR and 10/1GBASE-PRX PCS, when read as a one, bit 3.81.1 indicates that the receiver detected a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.1 indicates that the receiver detected BER lower than the configurable threshold (low BER state).

The latched high BER ~~shall~~ should be implemented with latching high behavior.

This bit is a latching high version of the 10GBASE-PR and 10/1GBASE-PRX high BER status bit (3.81.0).

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface

Add to the end of table 45.5.3.3 PMA/PMD management functions:

Item	Feature	Subclause	Value/Comment	Status	Support
MM119	Writes to this register have no effect	45.2.1.11		PMA:M	Yes [ ] No [ ] N/A [ ]

Add to the end of table 45.5.3.6 PCS options:

Item	Feature	Subclause	Value/Comment	Status	Support
*CPR	Implementation of 10GBASE-PR or 10/1GBASE-PRX PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]

Add to the end of table 45.5.3.7 PCS management functions:

Item	Feature	Subclause	Value/Comment	Status	Support
RM79	corrected FEC codeword counter is reset when read or upon PHY reset.	45.2.3.31		CPR:M	Yes [ ] No [ ] N/A [ ]
RM80	corrected FEC codeword counter is held at all ones in the case of overflow	45.2.3.31		CPR:M	Yes [ ] No [ ] N/A [ ]
RM81	uncorrected FEC codeword counter is reset when read or upon PHY reset.	45.2.3.32		CPR:M	Yes [ ] No [ ] N/A [ ]
RM82	uncorrected FEC codeword counter is held at all ones in the case of overflow	45.2.3.32		CPR:M	Yes [ ] No [ ] N/A [ ]