45.2.3 PCS registers

Change last rows of Table 45-82:

Register address	Register name
3.74	10GBASE-PR and 10/1GBASE-PRX FEC ability register
3.75	10GBASE-PR and 10/1GBASE-PRX FEC control register
3.76, 3.77	10/1GBASE-PRX and 10GBASE-PR corrected FEC codewords counter
3.78, 3.79	10/1GBASE-PRX and 10GBASE-PR uncorrected FEC codewords counter
3.80	10GBASE-PR and 10/1GBASE-PRX BER monitor timer control
3.81	10GBASE-PR and 10/1GBASE-PRX BER monitor status
3.82	10GBASE-PR and 10/1GBASE-PRX BER monitor threshold control
~~3.74~~ 3.83 through 3.32 767	Reserved
3.32 768 through 3.65 535	Vendor specific

45.2.3.33 10GBASE-PR and 10/1GBASE-PRX BER monitor timer control register (Register 3.80)

The assignment of bits in the 10GBASE-PR and 10/1GBASE-PRX BER monitor timer control register is shown in Table 45–111. This register is defined only when 10GBASE-PR or 10/1GBASE-PRX ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4.

Table 45–111—10GBASE-PR and 10/1GBASE-PRX BER monitor timer control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.80.7:0	10G-EPON BER monitor timer	Duration (in units of 5 microseconds) of the timer used by the 10G-EPON BER monitor function. Default value is 25 (i.e. 125 microseconds). A value of 0 indicates that the BER monitor function is disabled.	R/W

[a]R/W = Read/Write

45.2.3.35 10GBASE-PR and 10/1GBASE-PRX BER monitor threshold control register (Register 3.82)

The assignment of bits in the 10GBASE-PR and 10/1GBASE-PRX BER monitor threshold control register is shown in Table 45–113. This register is defined only when 10GBASE-PR or 10/1GBASE-PRX ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4.

Table 45–113—10GBASE-PR and 10/1GBASE-PRX BER monitor threshold control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.82.15:0	10G-EPON BER monitor threshold	Number of sync header errors within a timer interval that triggers a high BER condition for the 10G-EPON BER monitor function. Default value is 1600. A value of 0 indicates that the BER monitor function is disabled.	R/W

[a]R/W = Read/Write

Change in section 76.3.3.4.1 Variables in definition of BER_Threshold variable

Indicates the threshold value of invalid sync headers associated with the BER monitor function. When BER_Threshold bad sync headers are encountered within the BER Monitor_Interval period, the BER monitor raises the hi_ber flag. When the number of bad sync headers encountered within the BER_Monitor_interval period less than the BER_Threshold, the hi_ber flag is turned off. This value is reflected in MDIO register 3.82.