40G/100G Implementations with 10G FPGA: Part 2

For IEEE 802.3ba

Contributors and Supporters

Mike Li, Altera

David Greenfield, Altera

Zhi Wong, Altera

Divya Vijayaraghavan, Altera

Ali Ghiasi, Broadcom (TBC)

Chris Cole, Finisar (TBC)

Aris Wong, Foundry (TBC)

Ryan Latchman, Gennum (TBC)

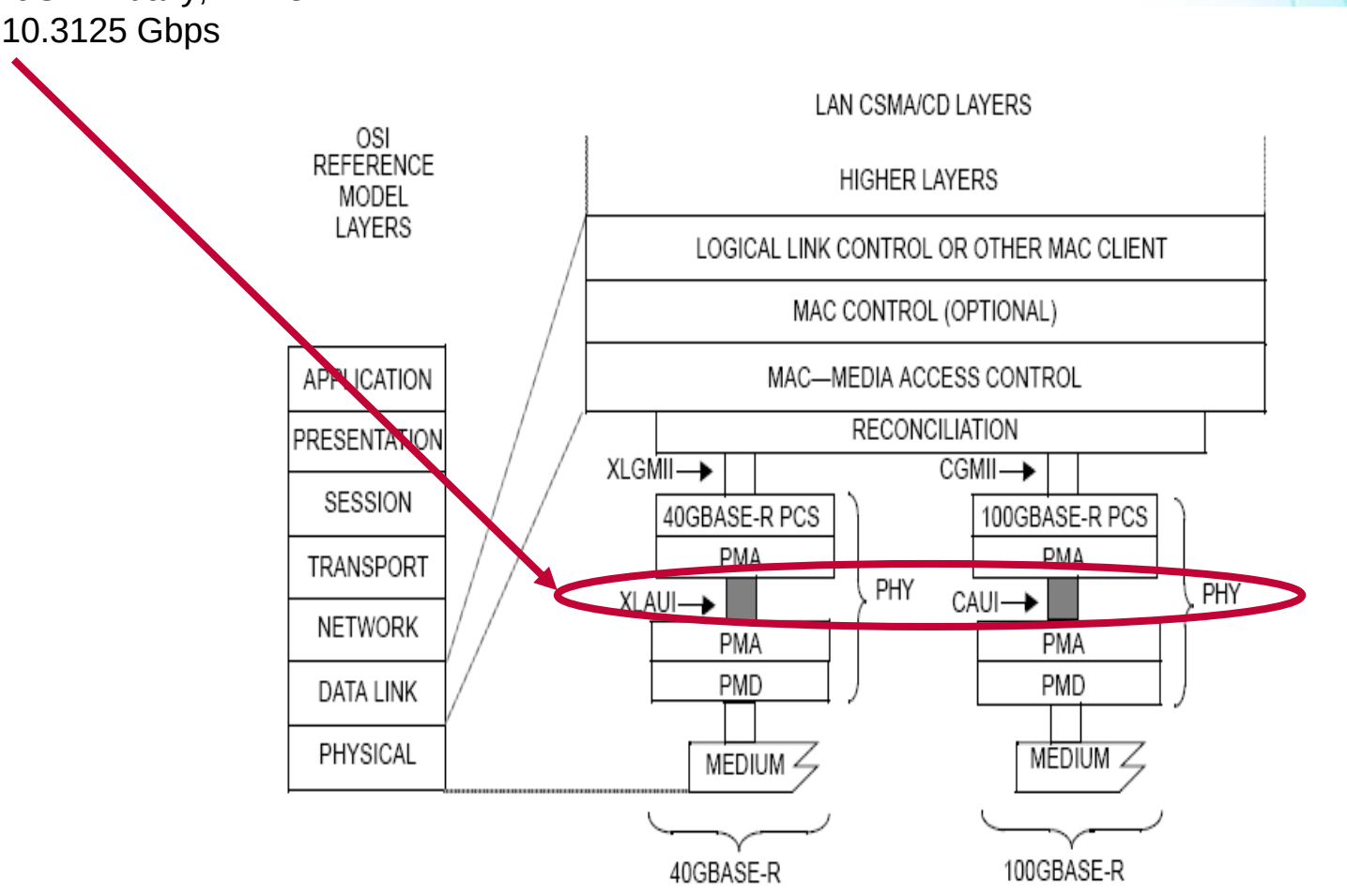
Andre Szczepanek , TI (TBC)

Franck Chang, Vitesse(TBC)

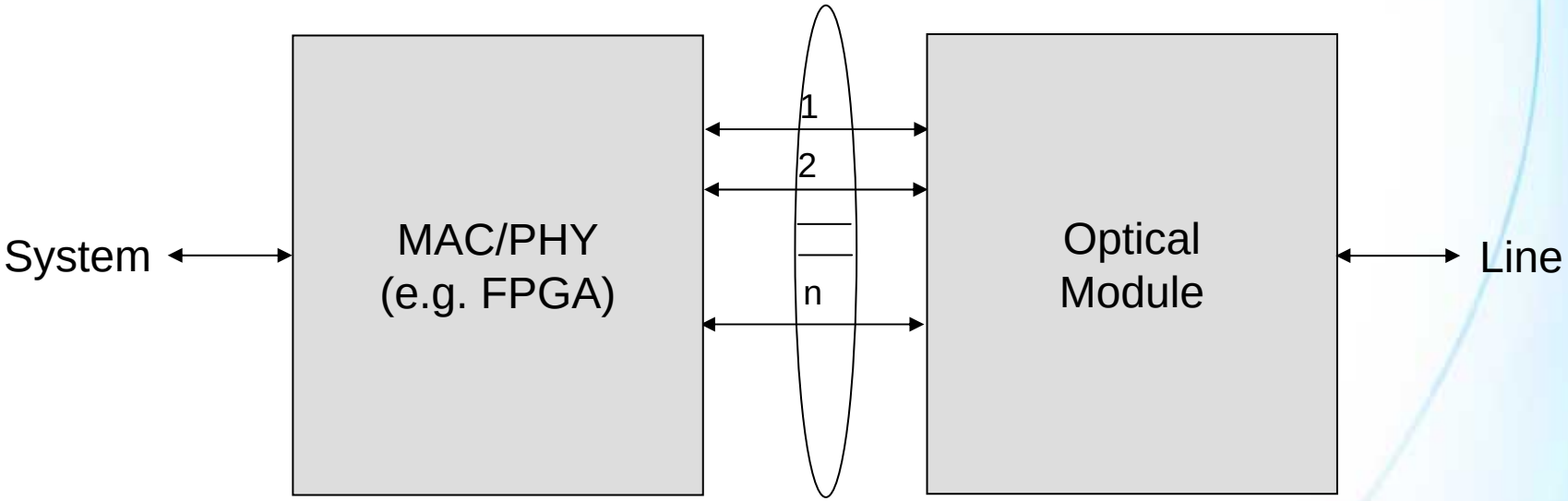
*TBC: To Be Confirmed

D0.9 Baseline Architecture 40G/100G Ethernet

"n" Lane PMA t<-> PMA, or PMA <-> PMD Electrical Interfaces
a) n= 10 Lanes for 100GE initially, CAUI
b) n= 4 Lanes for 40GE initially, XLAUI
Each lane runs at 10.3125 Gbps

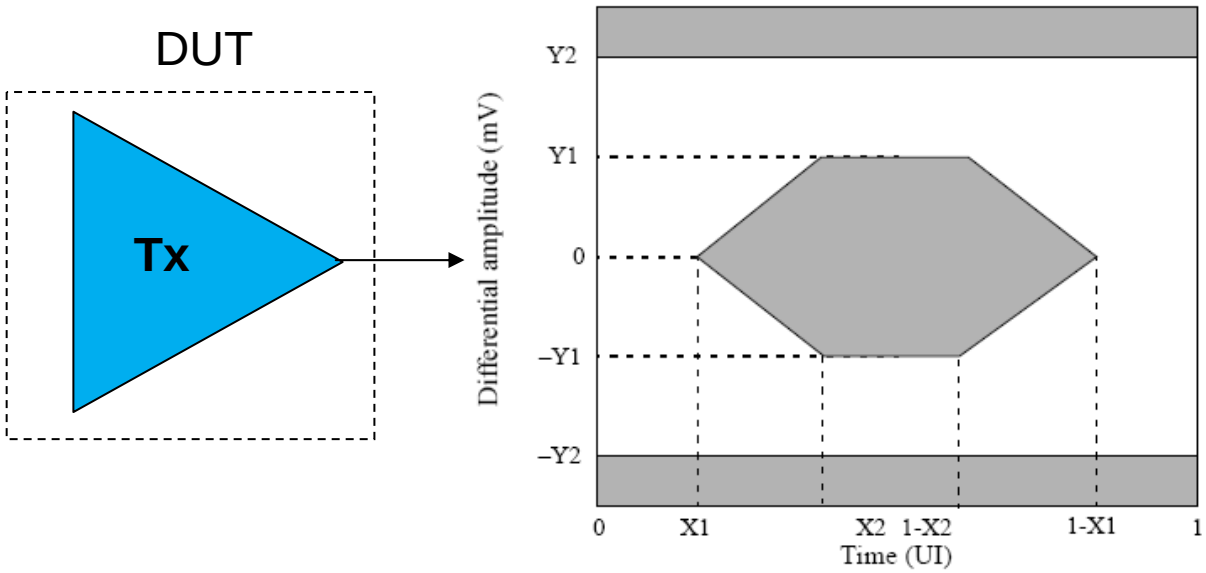


D0.9 Baseline Architecture Expected PMA ←→PMA or PMA ←→ PMD Interfaces



n = 4 for 40G and
n =10 for 100G ,
@10.3125 Gbps
for each lane

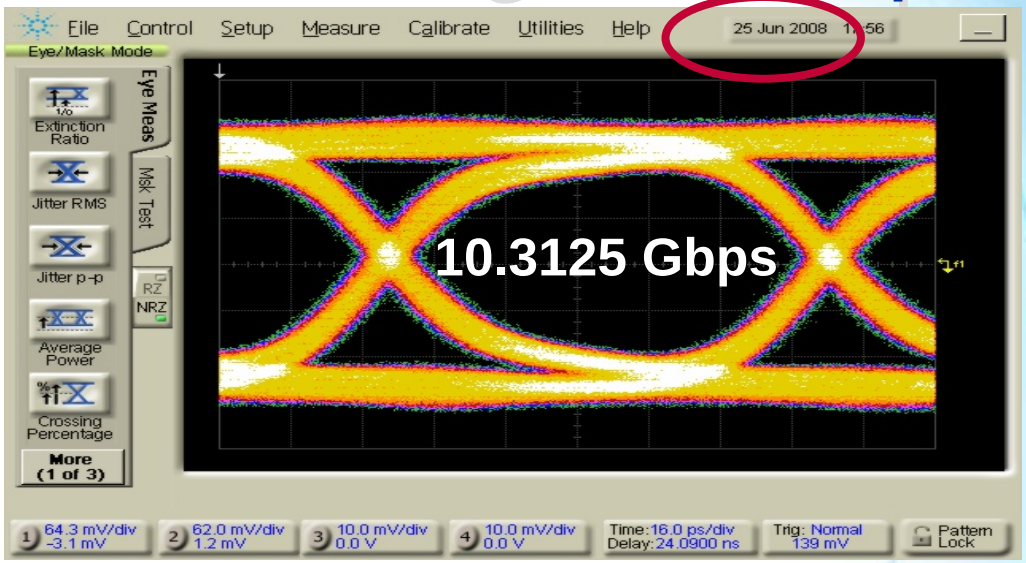
D0.9 XLAUI/CAUI Transmitter Signaling/Jitter Specification

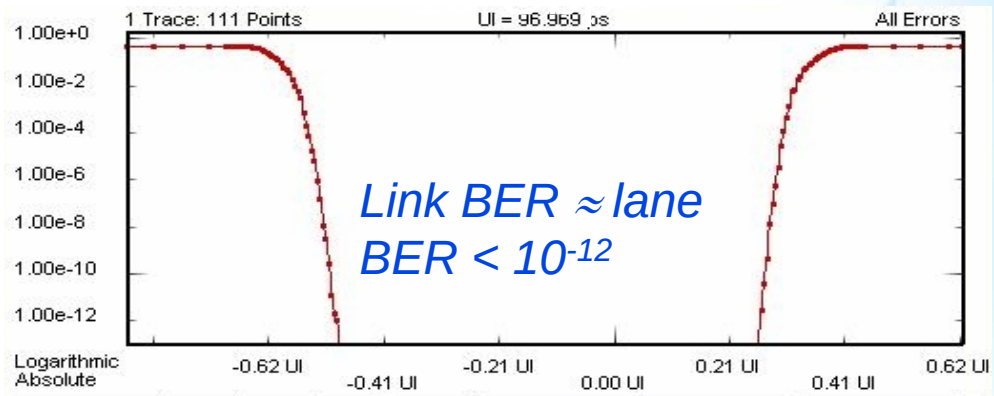


Maximum Total Jitter	0.32	UI
Maximum Deterministic Jitter	0.17	UI
Transmitter eye mask definition X1	0.16	UI
Transmitter eye mask definition X2	0.38	UI
Transmitter eye mask definition Y1	190	mV
Transmitter eye mask definition Y2	380	mV

40 nm FPGA SERDES Test Chip Transmitter Eye Diagram and BER Bathtub Curve @ 10.3125 Gbps

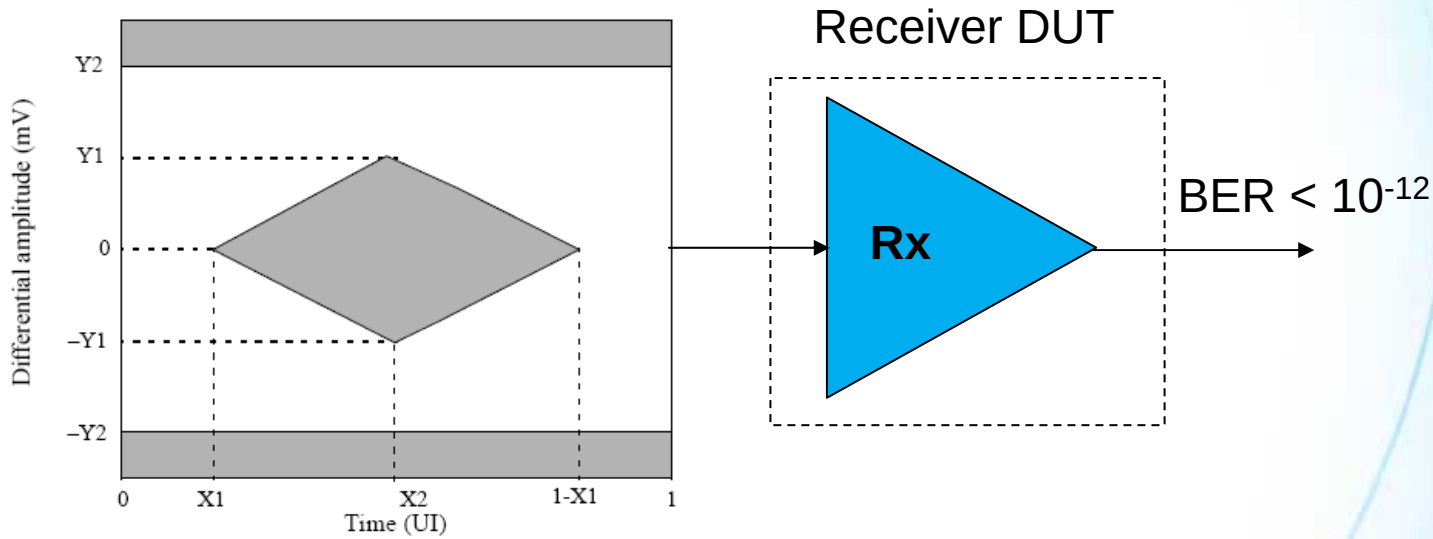
- Test Pattern
  - PRBS 2^{31}-1
- Vod
  - 600 mV
- DJ (δ-δ)
  - 5.08 ps, 0.0524 UI
  - Exceeds XLAUI/CAUI requirement (0.17 UI)
- RJ (rms)
  - 1.46 ps, 0.0151 UI
- TJ (@ BER = 10^{-12})
  - 25.6 ps, 0.264 UI
  - Exceeds XLAUI/CAUI requirement (0.32 UI)





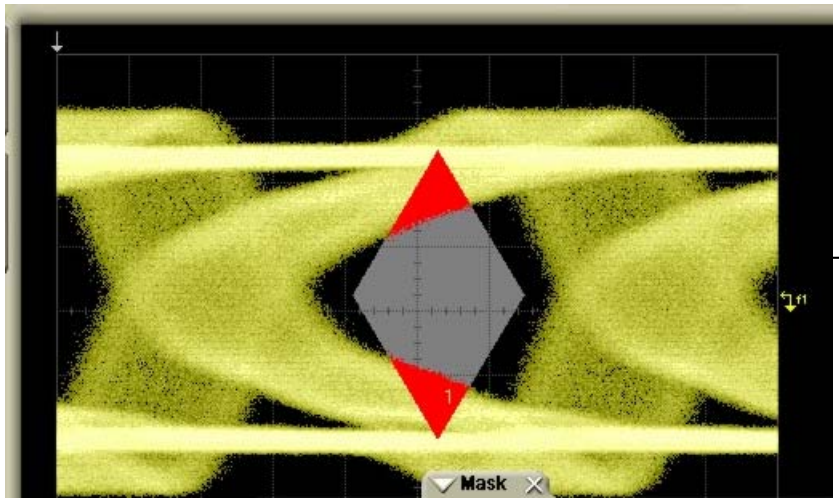
- *FPGAs that embed 10.3125G SERDES will be available in early 2009*
- *Test Chips are available since early 2008*
- *FPGA 10.3125G SERDES have pre/de-emphasis, FFE/CTLE equalization capabilities*

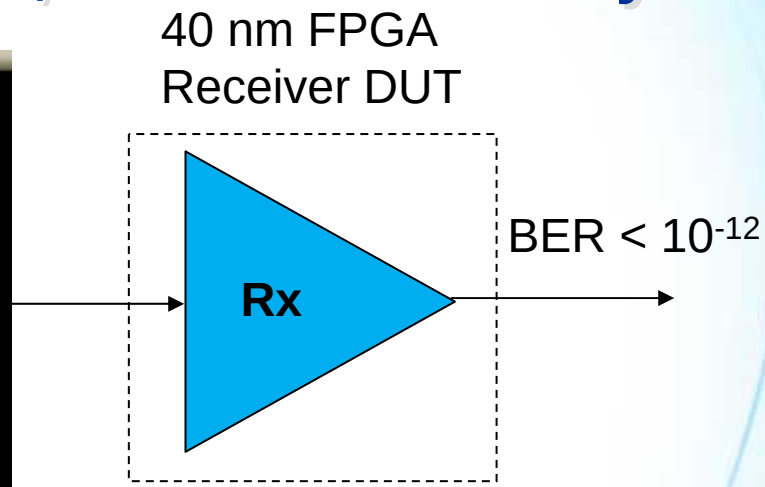
D0.9 XLAUI/CAUI Receiver Signaling/Jitter Specification, Part 1: Stressed Eye



Maximum Total Jitter	0.62	UI
Maximum non-EQ Jitter (TJ - ISI)	0.42	UI
Receiver eye mask definition X1	0.31	UI
Receiver eye mask definition X2	0.5	UI
Receiver eye mask definition Y1	45	mV
Receiver eye mask definition Y2	425	mV

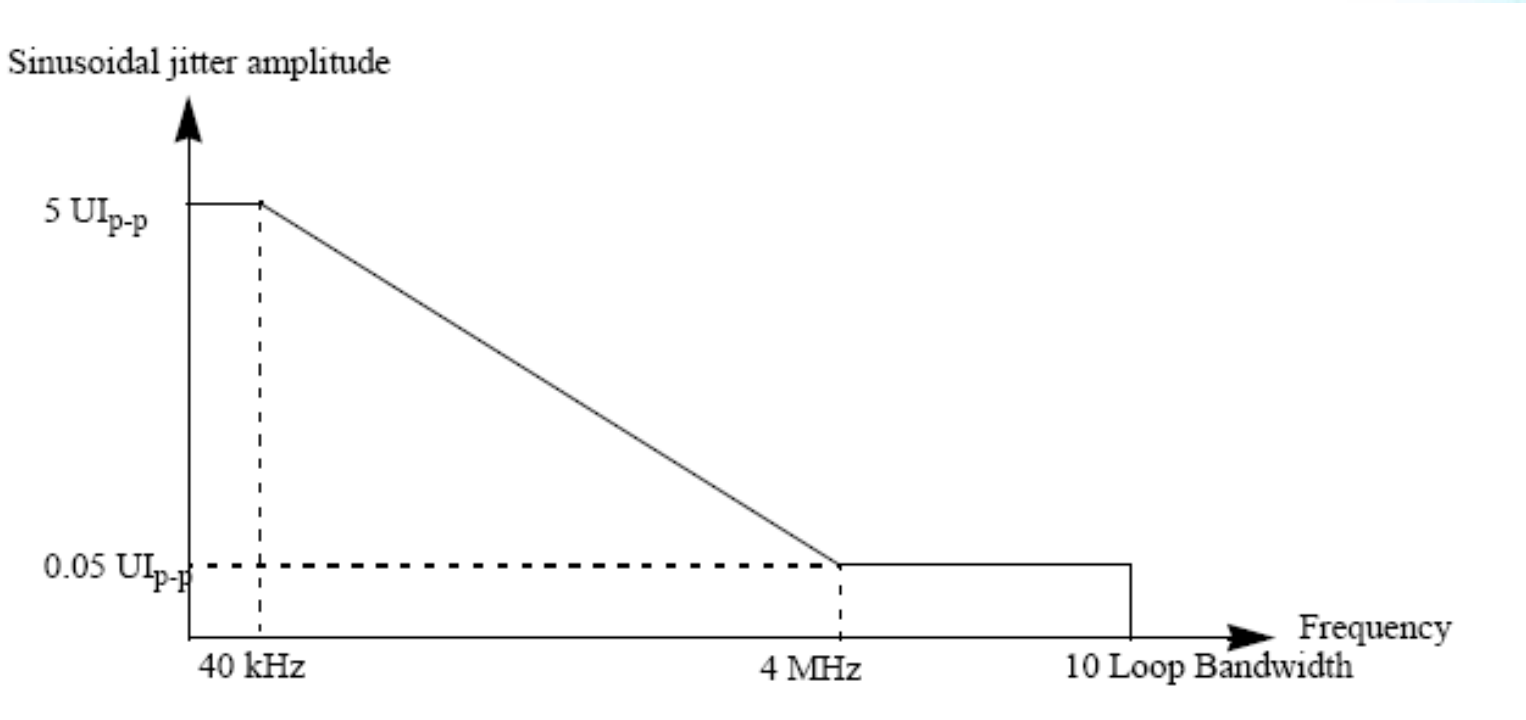
40 nm FPGA SERDES Test Chip Receiver Tolerance Test Results @ 10.3125 Gbps, Part 1: Stressed Eye



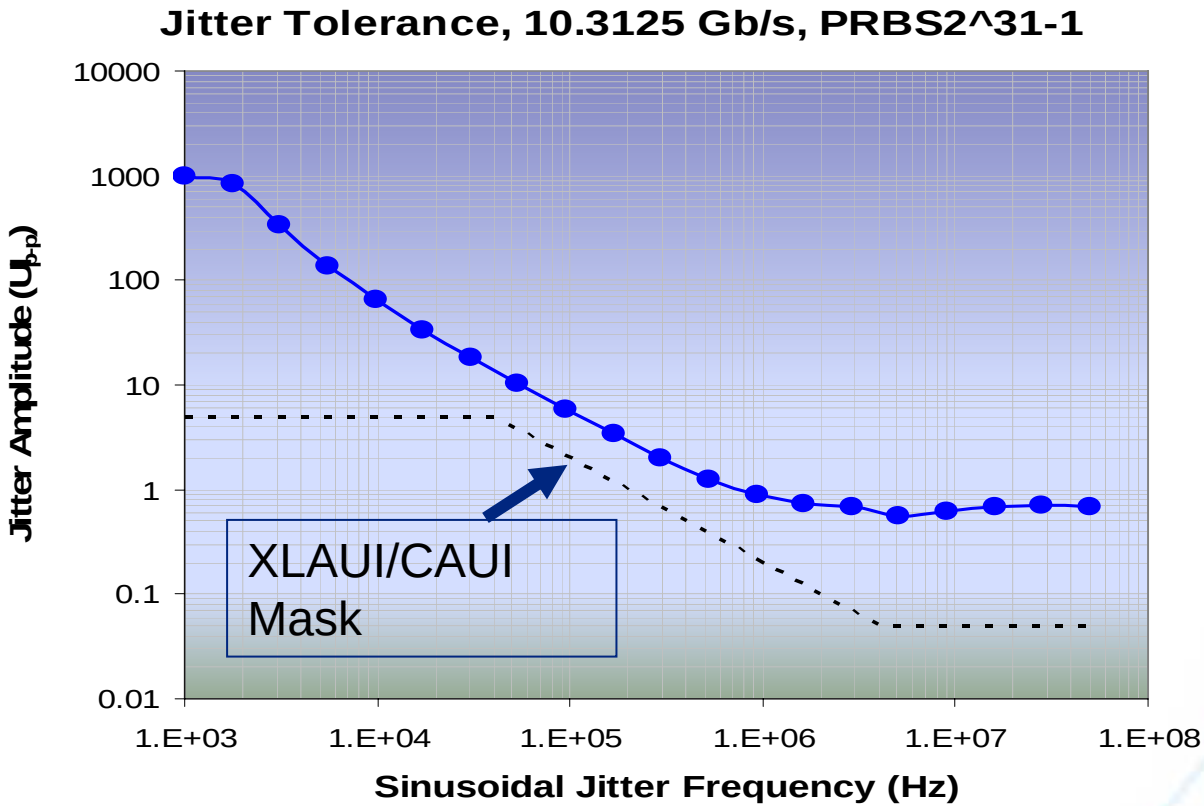


- Pattern
  - PRBS 2^{31}-1
- Eye-height (EH) < 90 mV
  - Exceeds XLAUI/CAUI requirement (90 mV)
- TJ (@ BER = 10^{-12})> 60.12 ps, or 0.62 UI
  - Exceeds XLAUI/CAUI requirement (0.62 UI)
- Non-EQ DJ (TJ-RJ-ISI) > 40.72 ps, or 0.42 UI
  - Exceeds XLAUI/CAUI requirement (0.42 UI)
- BER < 10^{-12}

D0.9 XLAUI/CAUI Receiver Signaling/Jitter Specification, Part 2: SJ Sweeping

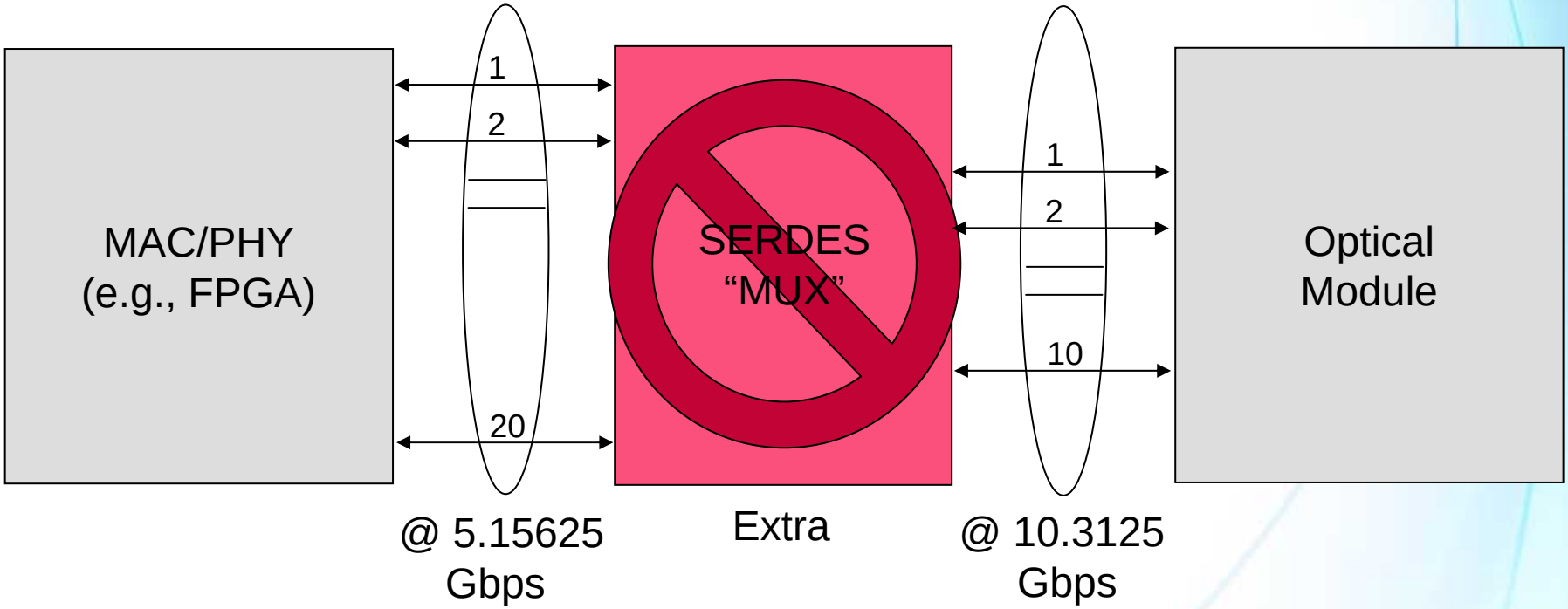


40 nm FPGA SERDES Test Chip Receiver Tolerance Test Results @ 10.3125 Gbps, Part 2: SJ Sweeping



- *FPGAs that embed 10.3125G SERDES will be available in early 2009*
- *Test Chips are available since early 2008*
- *FPGA 10.3125G SERDES have pre/de-emphasis, FFE/CTLE equalization capabilities*

10.3125 Gbps FPGA Transceiver Enables a Direct PMA←→PMA or PMA←→PMD Interfaces



Summary

- 10.3125 Gbps FPGA transceiver meets/exceeds the XLAUI/CAUI specification for both transmitter and receiver
  - Ultra low DJ, RJ and TJ for Transmitter
  - Superior receiver stressed eye and jitter tolerance for Receiver
- FPGAs with 10.3125 Gbps transceivers will be available in the near future
- 40G/100G implementation with 10.3125 Gbps FPGA transceivers do not need “SERDES muxes”
  - 10.3125 Gbps transceivers offer minimum transceiver count, lower power consumption & easier layout

Issues with the D1.0 XLAUI/CAUI Specification

- Is Tx equalization required? If so, spell out the Tx equalization details and factor them to the Tx verification
- Spell out the jitter transfer function (JTF) for Tx jitter and eye verification
- Is pulse width jitter (PWJ) required? If so, give the definition and number
- Is Rx equalization required? If so, spell out the Rx equalization details factor them to the Rx verification
- For Rx jitter tolerance test, jitter type and spectrum need to be spelled out
- Need to settle the BER if it is not 10^{-12}.

Thank you