

# Changes to XLAUI/CAUI Electrical Specifications

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# Where does the spec. apply?

153A.3.3 Transmitter characteristics, applies at TP0 and TP4 (eqv. to XFI A,C resp.).

153A.3.4 Receiver characteristics, applies at TP1 and TP5 (eqv. To XFI B,D resp.).

TP1,TP4 (XFI B,C) are at or near module connector pins.  
TP0,TP5 (XFI A,D) are at or near host ASIC pins.

This is not clear from Figure 153A-2.

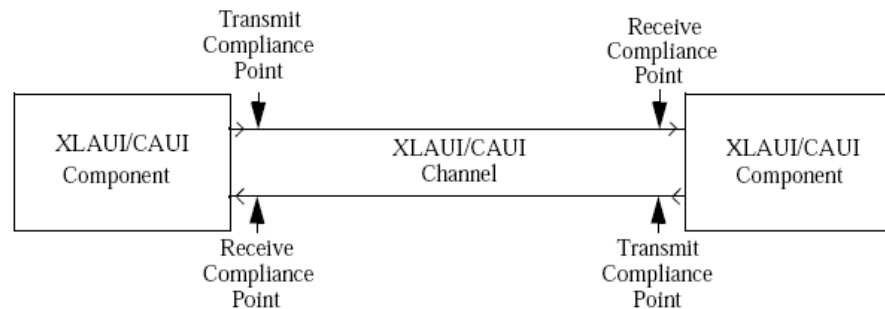


Figure 153A-2—Definition of transmit and receive test points

# Pre-Emphasis

To achieve the 25 cm. reach objective, the TX spec. should also include a minimum level of pre-emphasis that needs to be supported.

To test pre-emphasis, propose same approach as OIF-CEI-02.0 Clause 2.2.3.  
([http://www.oiforum.com/public/documents/OIF\\_CEI\\_02.0.pdf](http://www.oiforum.com/public/documents/OIF_CEI_02.0.pdf))

Testing pre-emphasis using a far-end eye mask like XAUI can result in understress because the far-end eye mask also includes effects such as reflections and crosstalk that will not be part of the test.

# Non-EQJ

Since the receiver has no equalization, can the RX non-EQJ spec. be removed? This will make the interconnect design more flexible.

If a non-EQJ spec. is retained to allow some linear equalization in the RX, an interference tolerance spec. would be needed to ensure proper stress test of the RX.

# BER

Tighten TX Jitter Generation and RX Jitter Tolerance spec. to cover BER of  $1e-15$  instead of  $1e-12$ .

Testing could still be limited to  $1e-12$  with data extrapolated to demonstrate compliance at  $1e-15$ .

# Interconnect Spec.

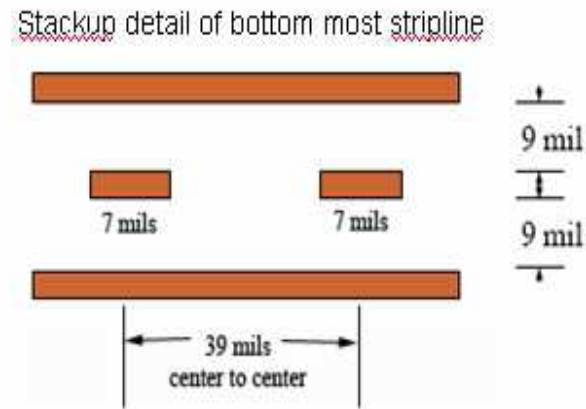
Draft 1.0 only includes S21 magnitude limit.

Phase response and crosstalk effects are not covered.

Propose an interconnect spec. similar to OIF-CEI-02.0 Clause 6.3.7 using StatEye.

# Test Point (TP0,TP5) Definition

Since ASIC/serdes pin/balls are associated with complex EM fields (non-TEM), it may be better to define TP0 and TP5 on a test board as the cross-section of two uncoupled stripline traces, 1" away from the component.



Alternately, TP0 and TP5 can be defined to be at the test board connector, with the test board defined to have a loss of 0.5 +/- 0.1dB at  $F_{\text{baud}}/2$  (Ali Ghiasi's suggestion).