40/100G Architecture & Interfaces proposal

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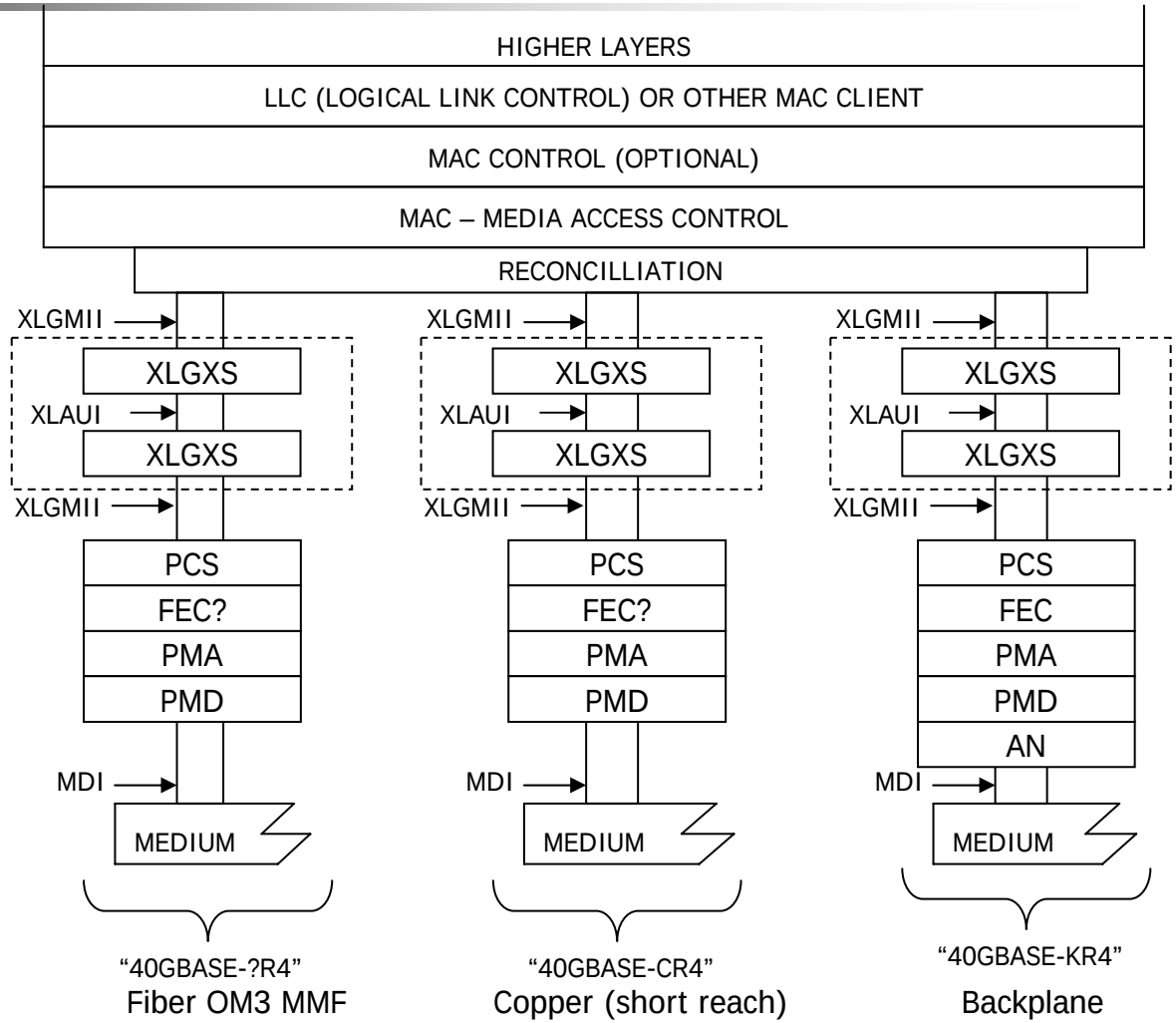
Agenda

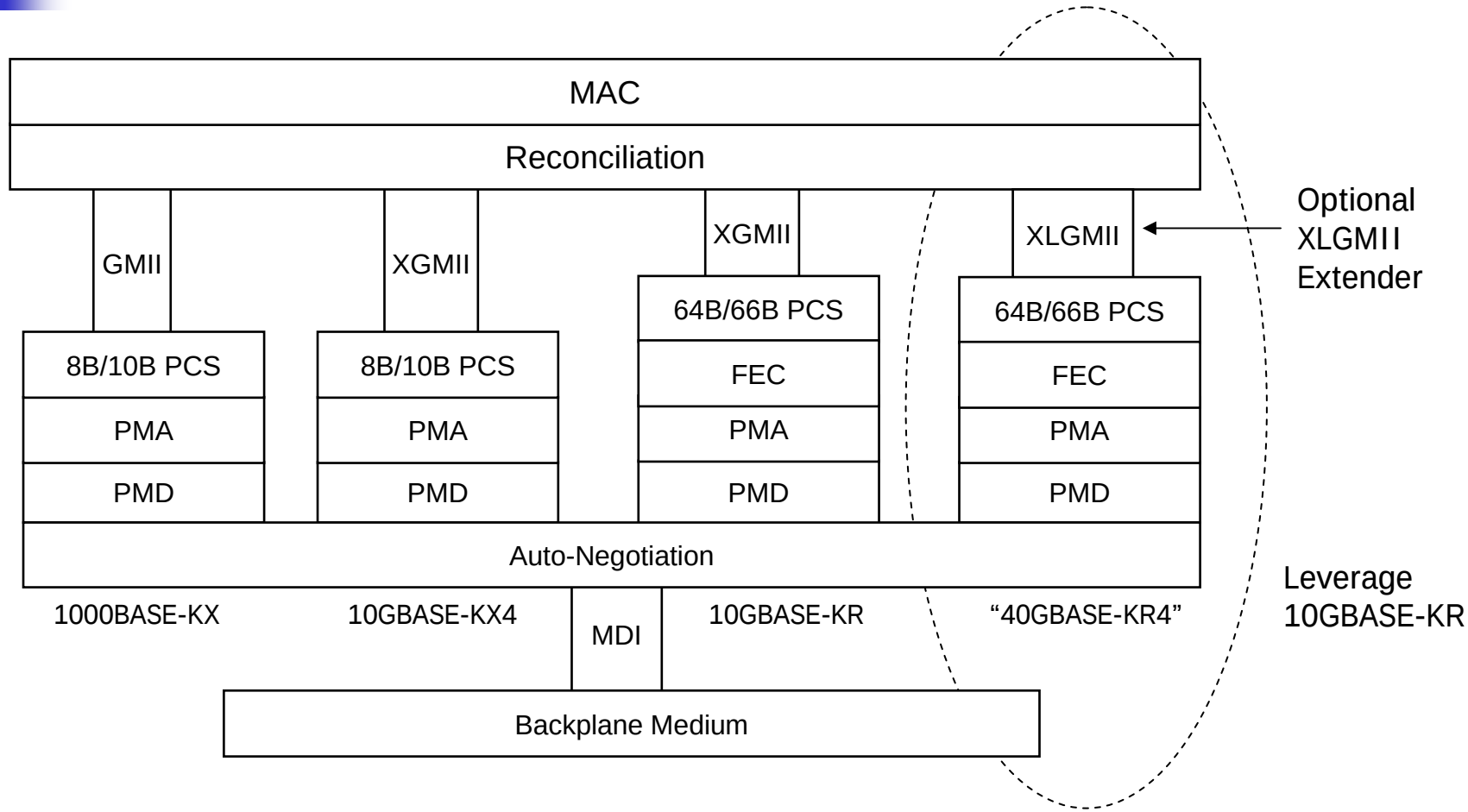
- Proposed 40/100G architecture
- Inter-sublayer interfaces
- Summary

Proposed 40GbE architecture

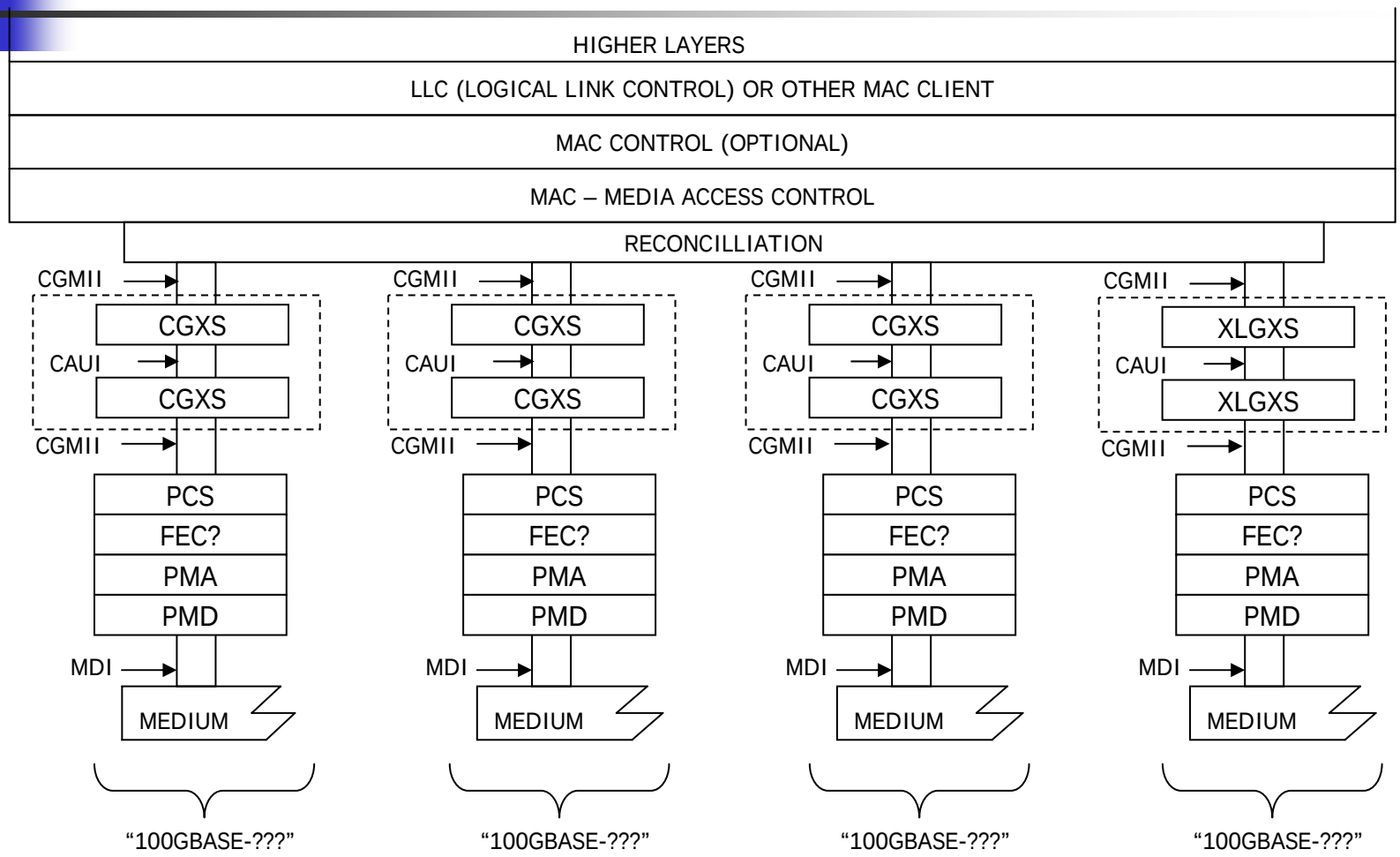
- Proposal based on discussions in HSSG
  - 4 lanes of 10G
  - R PCS (64B/66B code)
- Proposal for MAC/PHY interface
  - xMII for intra-chip connectivity
  - xAUI for inter-chip connectivity



Proposed 40GbE backplane architecture

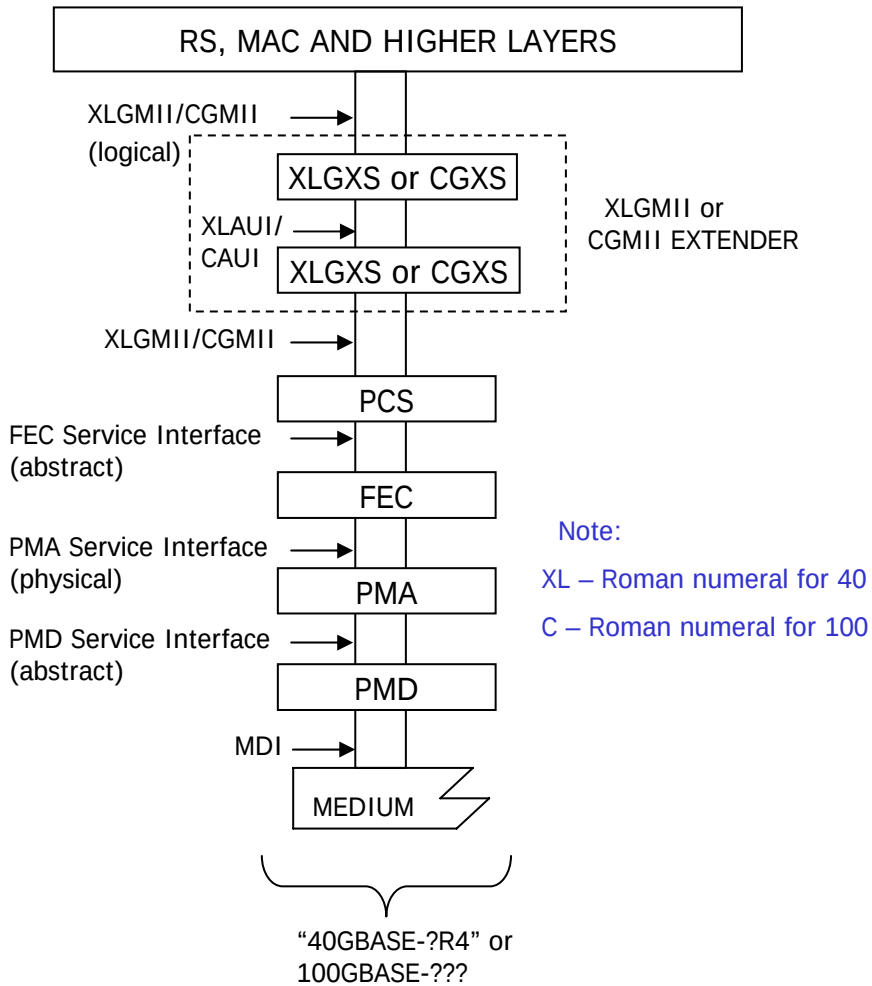


Proposed 100GbE architecture



Proposed 40/100GbE interfaces

- Inter-sublayer interfaces
  common to 40/100G where possible
  - XLGMII or CGMII
    - Logical; define data, clock, no electricals
  - XLAUI or CAUI
    - Physical, define electricals
  - FEC service interface
    - Abstract
  - PMA Service interface
    - Physical, define electricals
  - PMD Service interface
    - Abstract



Interface solutions needed (1)

- XLGMII (Forty Gigabit MII) or CGMII (100 Gigabit MII) – PCS interface
  - Interface between MAC and PHY layers needed for intra-chip connectivity
  - Need for Compatibility interface
    - Process advancements drive System on Chip (SoC) implementations
    - Example: 90nm, 65nm, 45nm and beyond
    - Multiple vendors develop IP blocks for same SoC, for example MAC and PHY layers from different vendors need to interoperate
  - Logical definition, data width, clock frequency, No electricals
  - XLGMII and CGMII can have same definition, different data width and clock frequency
- XLGMII or CGMII Extender (XLAUI / CAUI)
  - Interface between MAC and PHY layers needed for inter-chip connectivity
  - Plan for physical instantiation of an interface similar to XAUI for 10GbE
    - XAUI is widely used as MAC - PHY interface
  - Optimize for power, allows higher integration: e.g. Switches, multi-port LAN controllers
  - Physical definition, differential signaling, signaling rate, short reach channel
  - Lane width: 4 lane for XLAUI, and 4 or 10 lane for CAUI; 64B/66B encoding

Interface solutions needed (2)

- FEC Service interface
  - Abstract interface between PCS and optional FEC sublayer
- PMA Service interface
  - Optional physical instantiation allows implementations as Module interface
  - 4 lane serial interface for 40G
  - Decide on 10 lanes versus 4 lanes for 100G
  - Define electricals and channel characteristics
    - Short reach channels with minimum one pair of connectors
  - Historically module interface has been standardized outside of IEEE
- PMD Service interface
  - Abstract definition
  - PMA and PMD may be implemented together in the same module

Summary

- Build consensus on 40/100G high level architecture
  - Architecture to allow scalability and leverage 10G where possible
  - Consider dual or multi-speed system implementations with 10/40/100G
  - Define solutions based on architecture
- MAC/PHY interface
  - XLGMII/CGMII as compatibility interface for intra-chip connectivity
  - XLGMII/CGMII extender - XLAUI/CAUI interface for inter-chip connectivity
- Optional Physical instantiation of PCS, and PMA/PMD interfaces
  - Define PCS interface and electricals
  - Define PMA interface and electricals for module connectivity
    - Decide on Industry standard versus IEEE standard