

Overcoming Jitter Budget Issue with Use of “SLI” for nx10G Interface

IEEE 802.3ba Meeting
Portland
January 2008

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List of Contributors

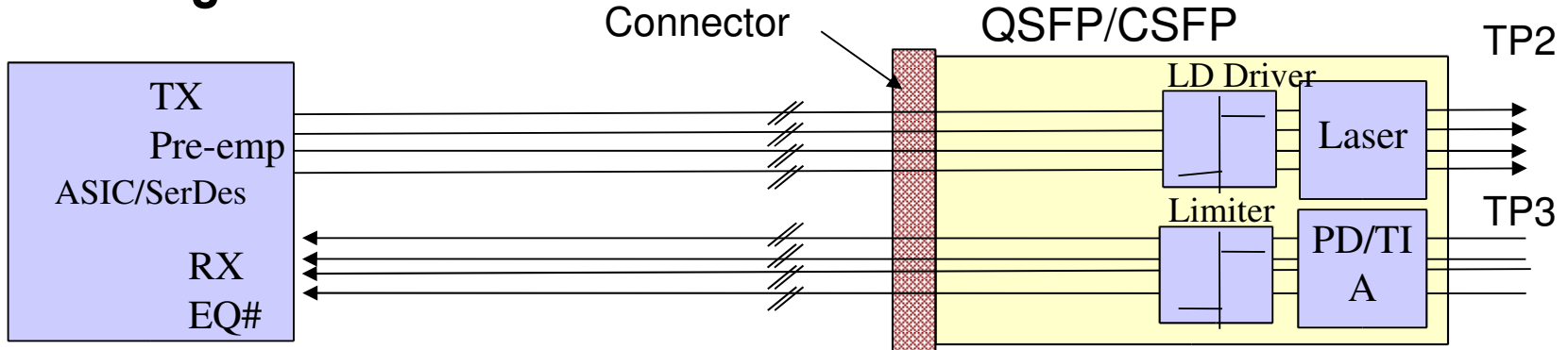
- **Tom Lindsay – ClariPhy**
- **Hossein Hashemi – Emulex**
- **Mike Dudek – JDSU**
- **Phil McClays – Zarlink**
- **Frank Chang – Vitesse**
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Overview

- **Scaling SFI single lane limiting specifications to 4x and 10x is too difficult without a CDR.**
- **TX pre-emphasis and EDC either adaptive or non-adaptive will be used for all implementations to overcome FR4 losses.**
- **Limiting module specifications would be difficult to close even if the fibre reach is reduced from 300 m to 100 m on OM3 due to transmit DDJ.**
- **Linear module specifications with adaptive EDC provides extra margin to close the link without using CDR in the module.**
- **Propose to use Simple Linear Interface “SLI” as the electrical interface for the nx10G interface with half the complexity of an SFI EDC.**

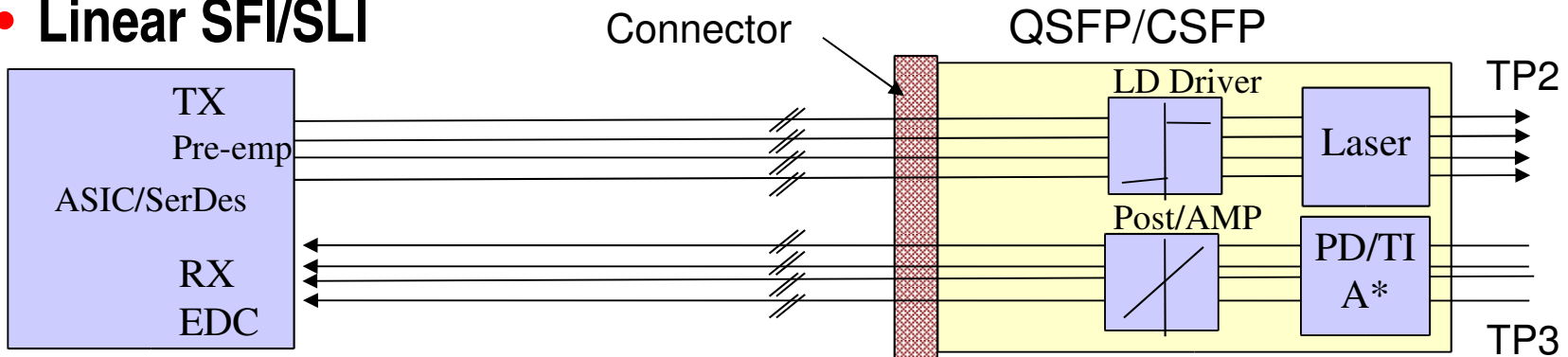
Block Diagram Limiting and Linear SFI/SLI

- **Limiting SFI/SLI**



Assumes continuous time equalizer or 1 tap DFE

- **Linear SFI/SLI**



* Common implementation incorporates AGC in the PD/TIA

The Benefit of Linear Module Interface with Adaptive EDC

- **EDC allow using slower lasers and detectors**
- **Allow longer fibre reach**
- **Support longer FR4 PCB traces**
- **No need for the CDR in the module**
 - Enable smaller form factor
 - Enable line card I/O capacity of over 1 Tb/s now.
 - Lower power dissipation
- **Lower cost**
- **Potentially common host chips with the backplane and copper cable.**

4X/10X Jitter Degradation Starting with SFI

- **SFI DDJ at B=0.1 UI**
 - DDJ at Host Output (B) for 4x link is expect at least 0.15 UI
 - DDJ at Host Output (B) for 10x link is expected to be at least 0.18

Degradation	4x Jitter (UI)	10x (UI)
SFI B	0.100	0.100
SerDes Penalty	0.025	0.040
PCB Routing	0.025	0.040
Total DDJ B	0.150	0.180
Total TJ B	0.320	0.360

Degradation	4x Jitter (UI)	10x (UI)
SFI C'	0.7	0.7
SerDes Penalty	-0.04	-0.07
PCB Routing	-0.02	-0.03
TJ at C'	0.64	0.6

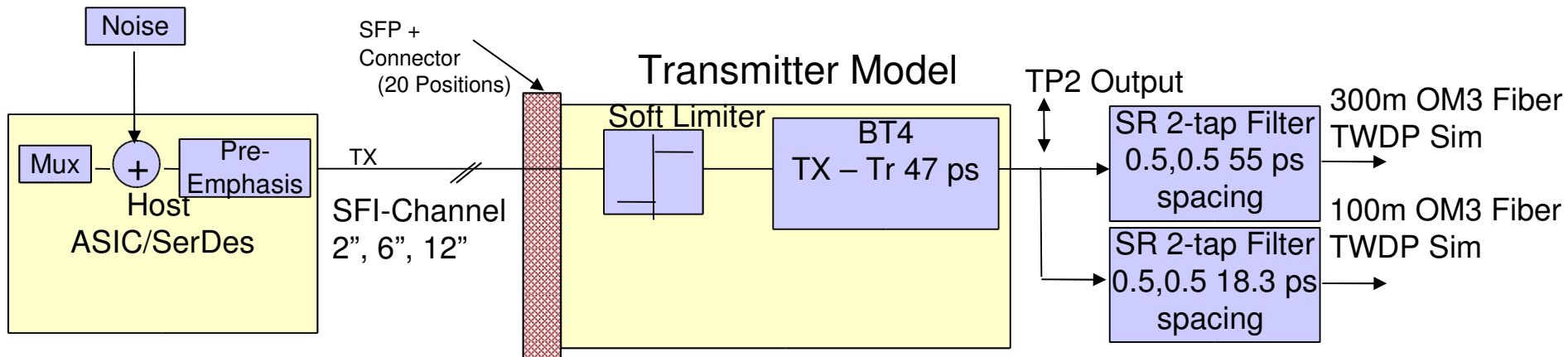
Starting Limiting Jitter Budget

- Assumption made
 - 10x10 Gig optics is given no excess penalty
 - DJ would increase by 0.05 UI

Jitter Compliance Points	B	TP2	Fiber	TP3	C*
4x10Gig					
DJ UI	0.150	0.300	0.050	0.350	0.450
TJ UI	0.320	0.500		0.550	0.715
1-sigma RJ at max DJ for BER 1E-12 (ps)	1.178	1.386		1.386	1.836
10x10 Gig					
DJ UI	0.180	0.330	0.050	0.380	0.480
TJ UI	0.360	0.550		0.600	0.765
1-sigma RJ at max DJ for BER 1E-12 (ps)	1.247	1.524		1.524	1.975

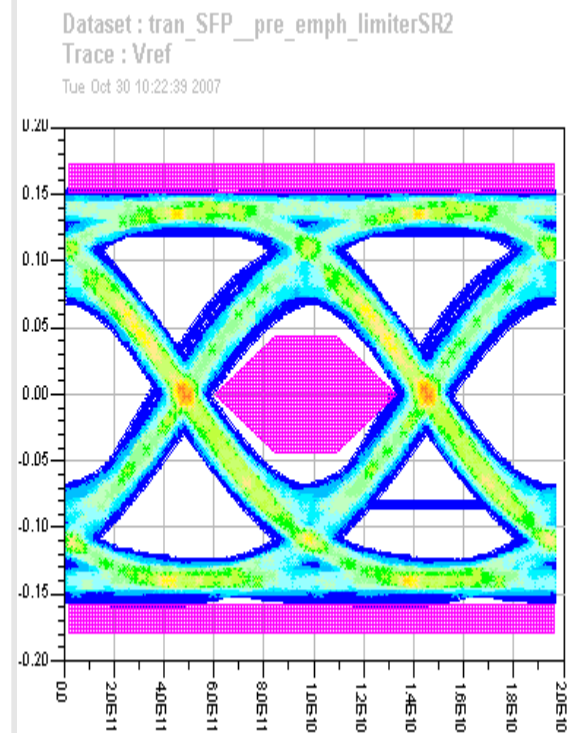
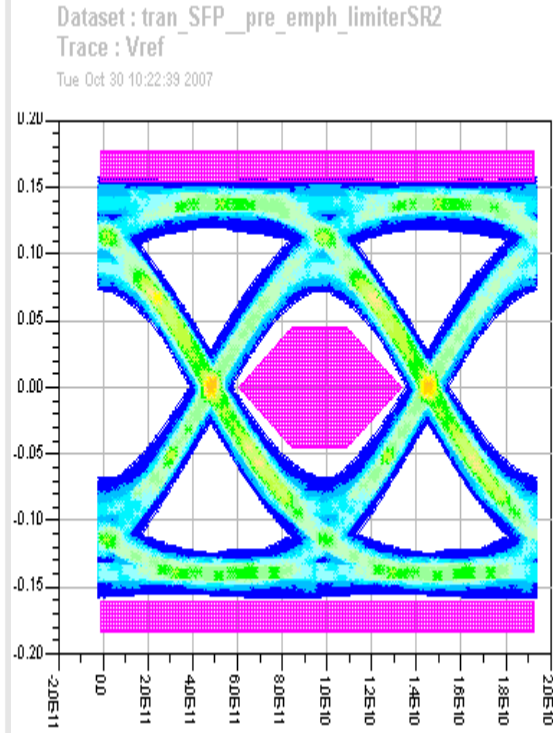
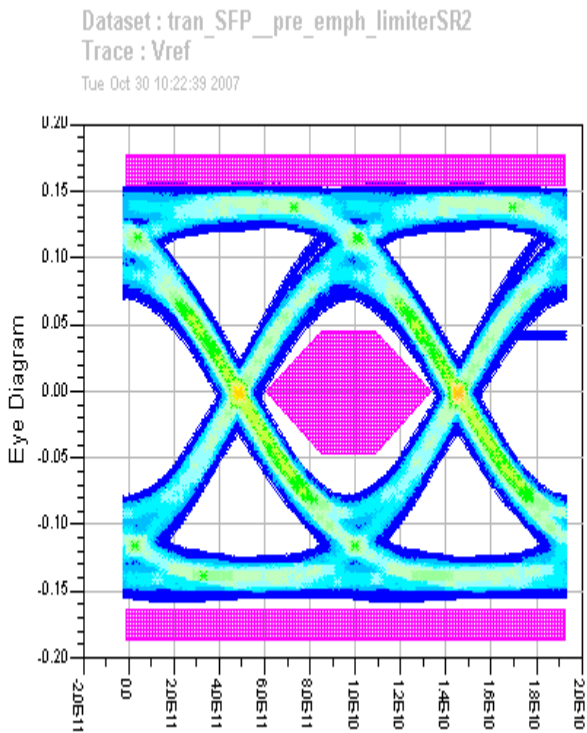
SFI TP2 Simulation Set-up and TWDP Results

- RIN penalty is not included
- Output rise time was calibrated with 2 inch stripline
- Noise source at the SerDes was adjusted for UJ of ~ 0.023 UI (RMS) at B.
- BT4 filter in the module was adjusted for Trise/fall of 47 ps 20-80%.



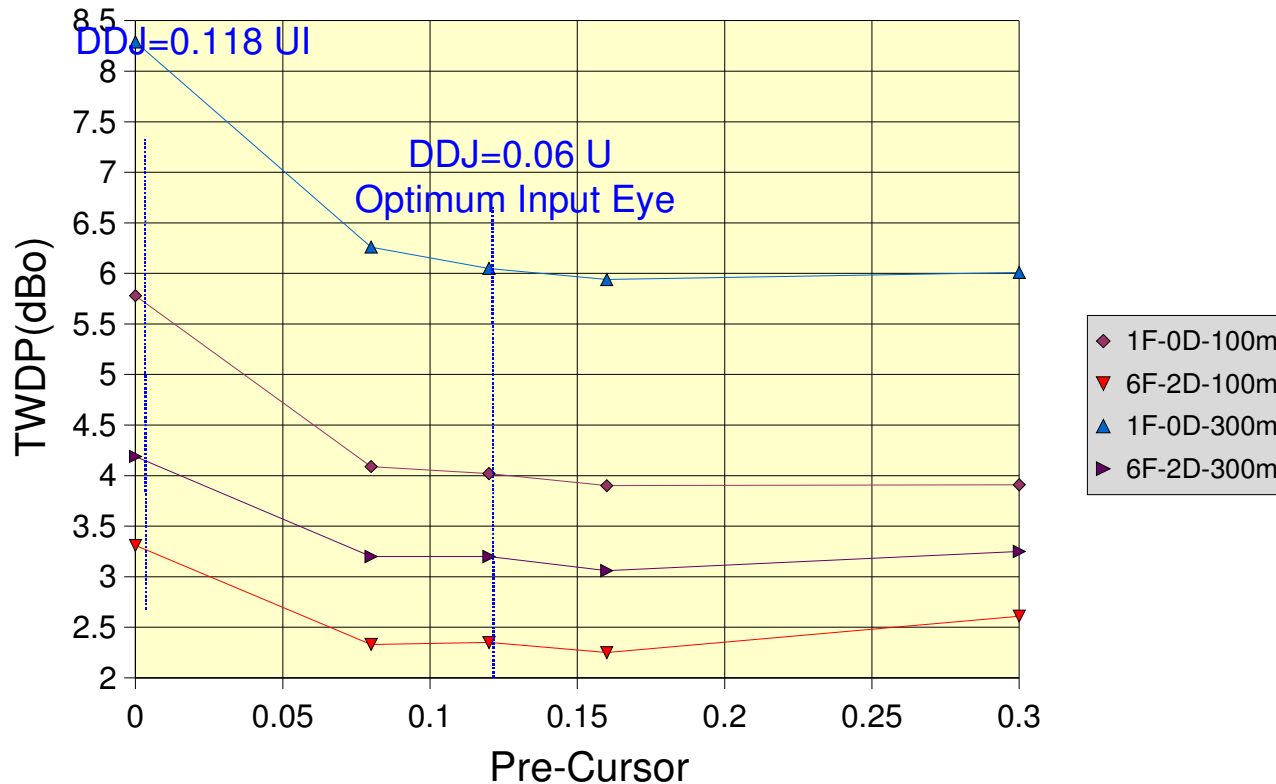
SFI Transmitter Output with Optimum Pre-emphasis

- Pre-emphasis single T-Spaced post
 - Eye mask will get degraded further due to PCB and IC variations!
 - 2" Fr4-13
 - 6" Fr4-13
 - 12" Fr4-13



TWDP as Function of Pre-emphasis

- Pre-emphasis=0 results in an input DDJ of 0.118 UI <the amount on page 8
 - 6" STL has TWDP of 5.8 dBo for 100m with 1FFE-0DFE but only 3.4 dBo with just 6T/2FFE+2TDFE!
 - Linear can do 300 m with about 1 dB less penalty than limiting can do 100 m!



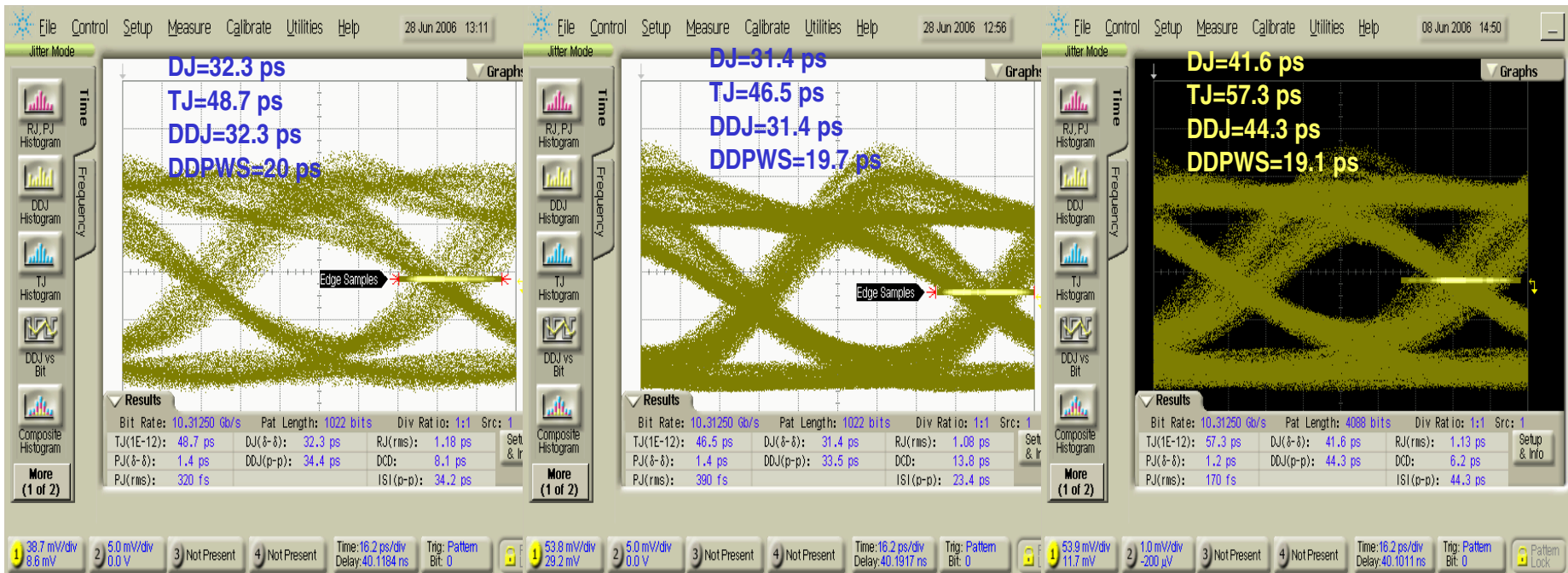
Eye Diagram for 3 Sub-10G Transmitters

- aronson_01_0907.pdf stated parallel link need more margin so we started with 3 sub-10G transmitters
 - The lasers DJ and TJ are similar to the jitter spreadsheet on page 9 at TP2!

Supplier-A

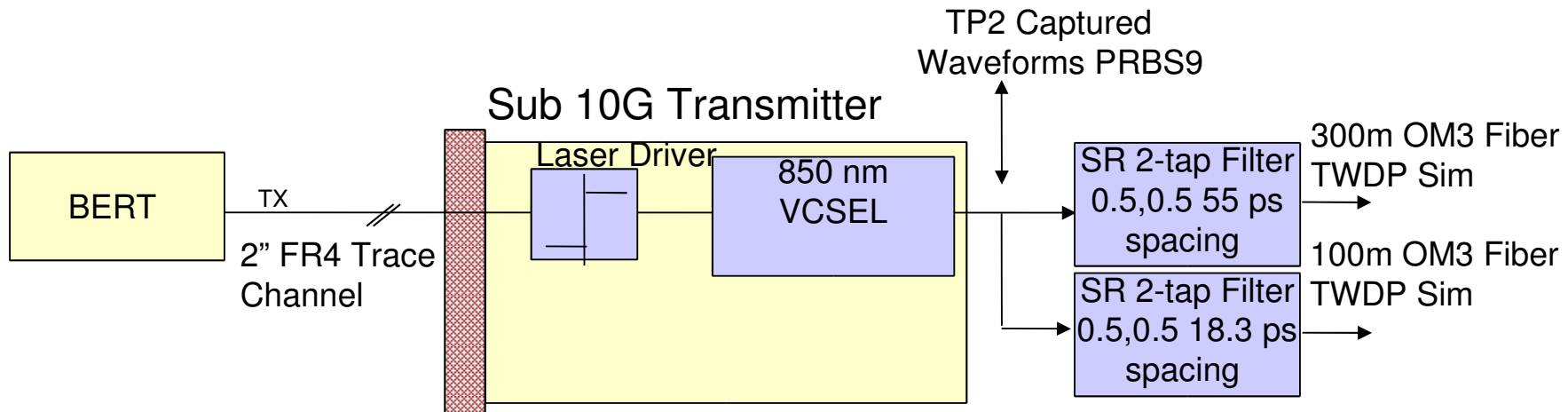
Supplier-B

Supplier-C



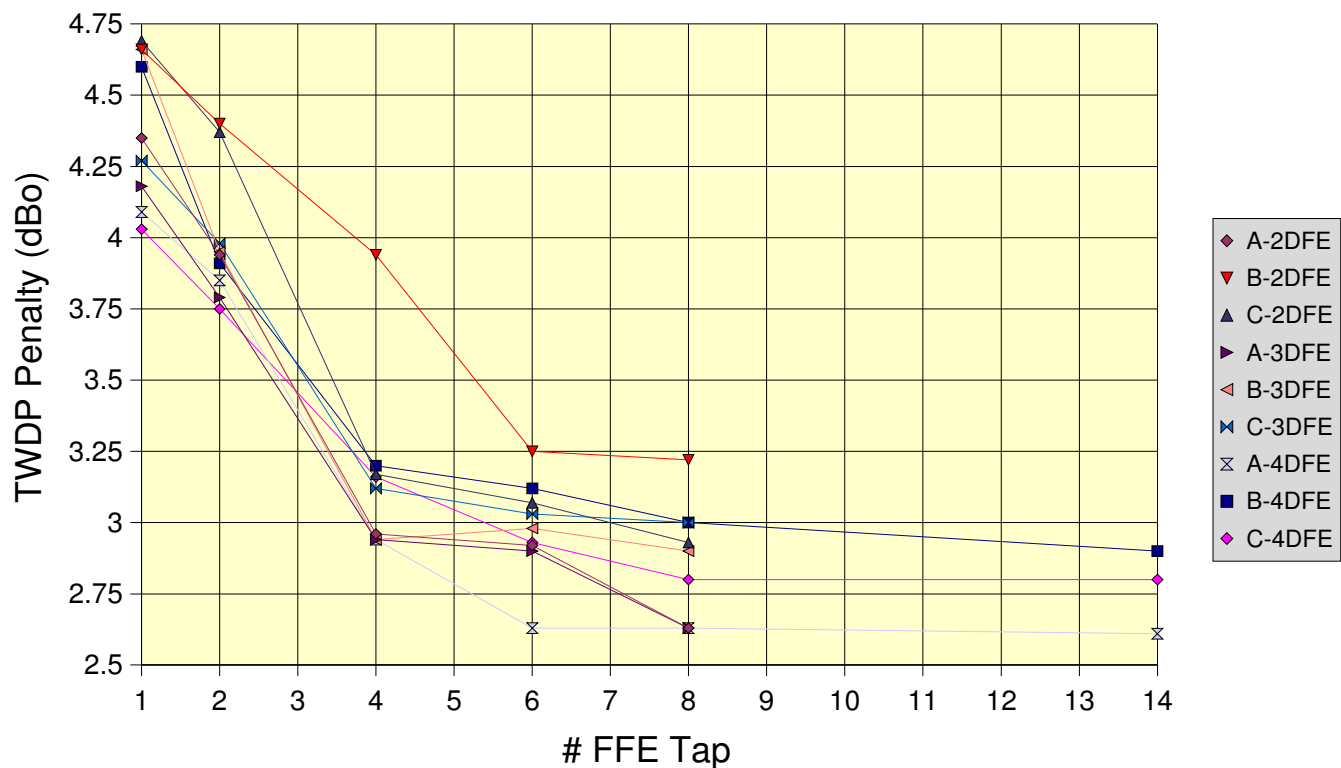
Sub 10G TWDP Simulation Set-up

- Code based on IEEE 802.3 CL 68
- LRM stressor in the IEEE code were replaced with
 - 2-tap FIR filter (0.5,0.5) with 55 ps delays to emulate 300 m OM3 fiber as defined by IEEE 802.3 CL 52
 - 2-tap FIR filter (0.5,0.5) with 18.3 ps delays to emulate 100 m OM3 fiber



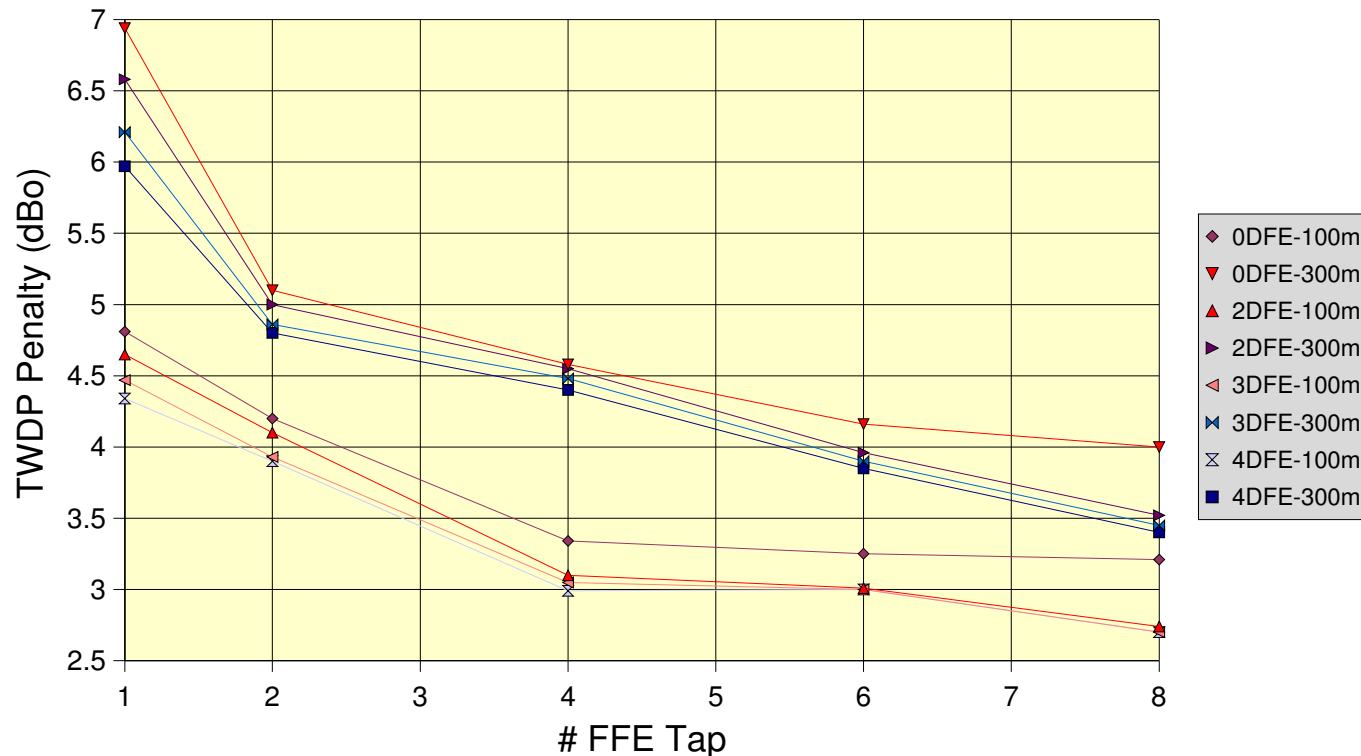
TWDP Penalty as Function of FFE and DFE Taps (no fibre stressor)

- Based on the study of 3 suppliers A, B, and C sub 10G transmitters
 - Fiber and the RX electrical PCB/connector not included
 - Min reference receiver would be 4 T/2 FFE+2 T DFE



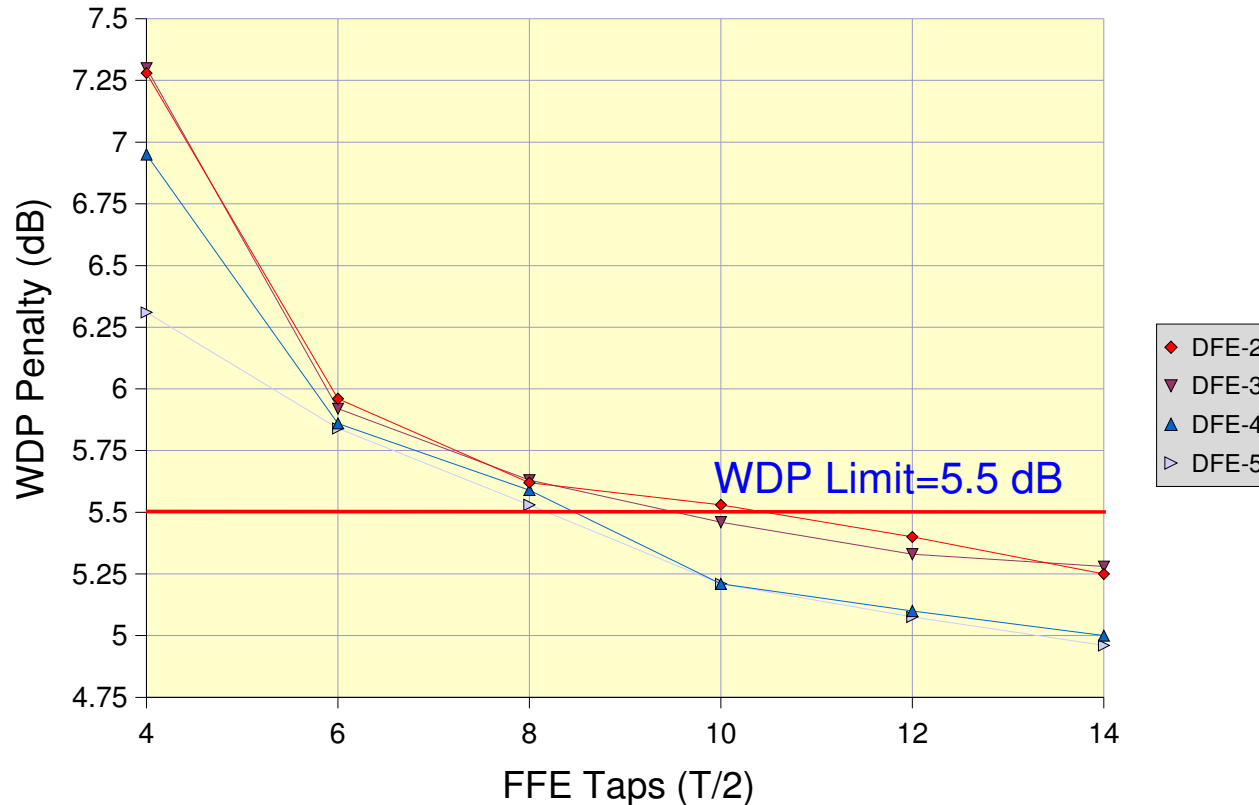
WDP Penalty as Function of FFE and DFE Taps for 100m and 300

- Transmitter A response with 100m and 300 m of OM3 fiber
 - RX electrical PCB/connector not included
 - Reference receiver with 4 T/2 FFE+2 T DFE should be sufficient for 100m
 - Reference Receiver with 6 T/2 FFE+ 2 T DFE should be sufficient for 300m



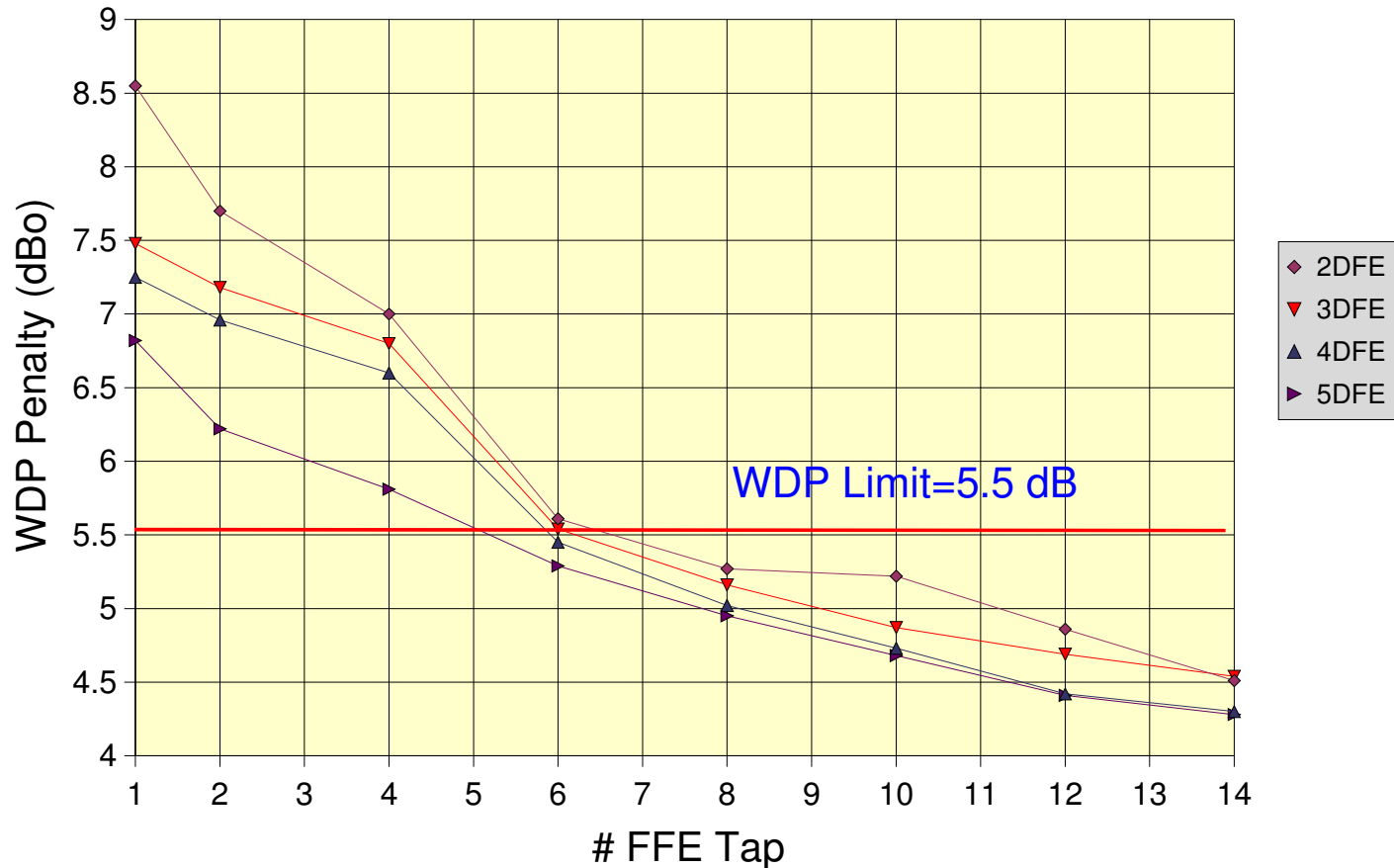
Copper Direct Attach WDP Penalty for Several EDC

- 10 m cable pre-emphasis=0
- Min EQ required =10 T/2 FFE+3 DFE



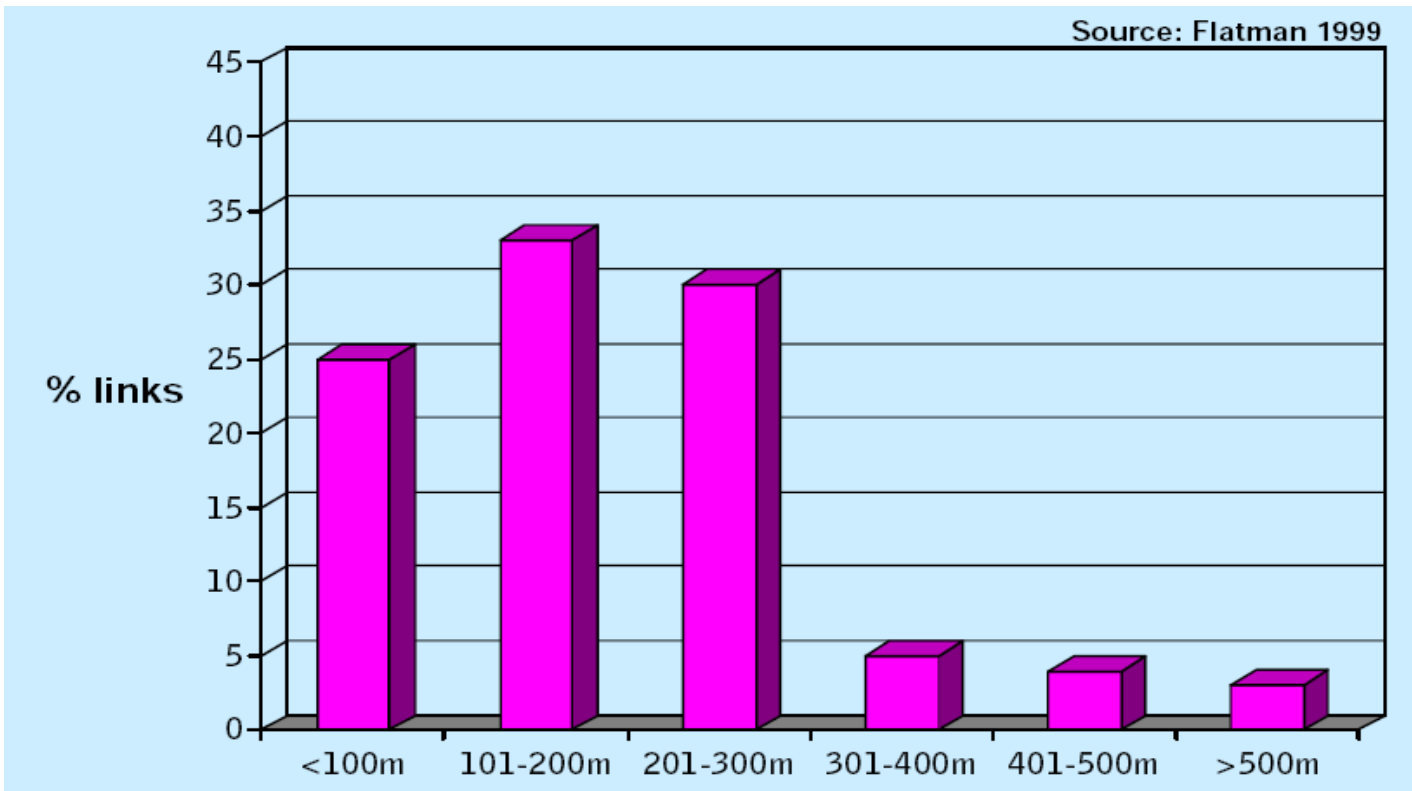
Copper Direct Attach WDP Penalty for Several EDC Implementations

- 10 m cable pre-emphasis=36%
- 10 m copper cable can be supported with SLI baseline Eq 6 T/2 FFE+2 T DFE



Does the Reach Objective of 100 m Enough on the nx10G Links

- As the Flatman_1_0304 shows to cover most of the backbone the reach should be extend to 200-300m.
- As demonstrated linear can extend the fiber reach to 220m or 300m without any real penalty for applications which have no other reach option available.



Form Factors Expected to Increase Line Card Density

- Parallel 850 nm (SR) and copper (CR) QSFP and CSFP are the solution which will actually increase the line card I/O capacity.
- The core switches with highest BW demand have no option beyond 100 m!
 - Even worse 40 GbE application have no solution beyond 100 m.

Solution	Link Bit Rate (Gb/s)	Electrical I/O (Gb/s)	Optical I/O (Gb/s)	Module Width (mm)	Year Beta	BW Gb/mm *
SFP+ (SR)/CR	10	10	10	13.3	2007	1.5
QSFP (SR)/CR	40	10	10	18.29	2008	4.37
X40 (LR)	40	10	10	40.64	2008	0.98
CSFP (SR)/CR **	100	10	10	26	2009	3.85
4x25G Gen 1	100	10	25	81.28	2009	1.23

* SFP+ and QSFP are assumed to be stacked. ** Assumes Molex iPass 12X

Conclusion

- **SFI limiting jitter specifications are challenging and would be very difficult to scale to 4x and 10x limiting link.**
- **This presentation shows a linear host (6T/2 FFE+2T DFE) can do 300 m with about 1 dB less penalty than a limiting host can do 100 m with both simulated SFI channel models and using Sub-10G lasers.**
- **Use of linear host with adaptive EDC can allow**
 - **Relaxing SerDes transmitter and receiver**
 - **Allowing more margin for the host implementations**
 - **Common electrical interface for 4x and 10x**
 - **Use lower cost optics**
 - **Increase line card I/O capacity compare to SFP+**
 - **Possible SerDes chip commonality with copper cable and backplane.**
 - **As the bounce the same host could support 10 m of copper!**