MLD (CTBI) Updates - MTTFPA

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Agenda

- Background on MTTFPA and CRC error protection
- 40GE MTTPFA Analysis
- 100GE Multi-mode MTTFPA Analysis
- 100GE Single-mode MTTFPA Analysis
- Notes about burst errors
- Next Steps and Summary

MTTFPA and MLD

- Ethernet's CRC32 has the following error detection capability
  - All 1, 2 or 3 bit errors are detected
  - All burst up to 32 bits
  - All two bit burst errors up to 8 bits
  - The above is true for at least up to 9k frames
- For the 10GBASER scrambler, single bit errors become 3 bit errors
- This was shown to not degrade the error detection capability of the IEEE CRC32 for 10GBASE-R [5], [1], [2]
  - No CRC degradation occurs if the CRC and the scrambler polynomial do not share common factors
  - IEEE CRC32 has no common factors with the X^58 scrambler
  - If the original errors can be detected, then the multiplied errors are also detectable
- The PCS/MLD does muxing and scrambling, does that impact MTTFPA?

Polynomial Background

- An N-bit message can be represented as a n-1 degree polynomial

  $M(x) = x^3 + x + 1$ is equivalent to the message b1011

- IEEE CRC Polynomial: $G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- FCS = remainder of $M(x)x^{32} / G(x)$

  Where $M(x)x^{32}$ is M(x) followed by 32 zeros

- Transmitted message: $T(x) = M(x)x^{32} + FCS$
- Remainder of T(x) / G(x) is zero
- What the receiver sees: $R(x) = T(x) + E(x)$

  Where E(x) is the error polynomial

- Received message is assumed correct if R(x) / G(x) has no remainder
- Remainder of R(x) / G(x) = remainder of E(x) / G(x)
- Error is detectable if E(x) / G(x) has a remainder
- Error detection capability is not changed if E(x) is shifted left or right
- This is summarized from [2]

Error Duplication

- Errors are duplicated by the $X^{58} + X^{39} + 1$ scrambler
- The error seen at the Receiver is D(x) = E(x) + E'(x) + E''(x)
- D(x) can be expressed as D(x) = E(x) $(x^{58} + x^{39} + 1)$
- We will detect a duplicated error if D(x) = E(x) (x58 + x39 + 1) is not a multiple of G(x) (assuming we can detect E(x))
- Our scrambler has no factors in common with G(x):

  Factorization for: $x^{58} + x^{39} + 1$ (scrambler)

  $(x^{58} + x^{39} + 1)$ (irreducible)

  Factorization for: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1$ (CRC32)

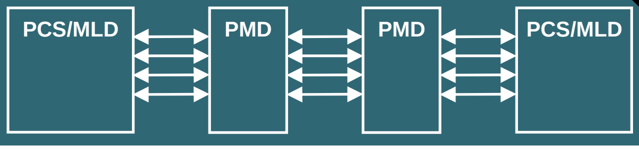
  $(x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1)$ (irreducible)
- Conclusion: D(x) is divisible by G(x) if and only if E''(x), E'(x) and E(x) are divisible by G(x)
- Therefore there is no change in error detection capabilities due to scrambling
  - At least for the cases where all errors are contained in the packet
- The above is extrapolated from [2]

Review of the PCS/MLD Processing

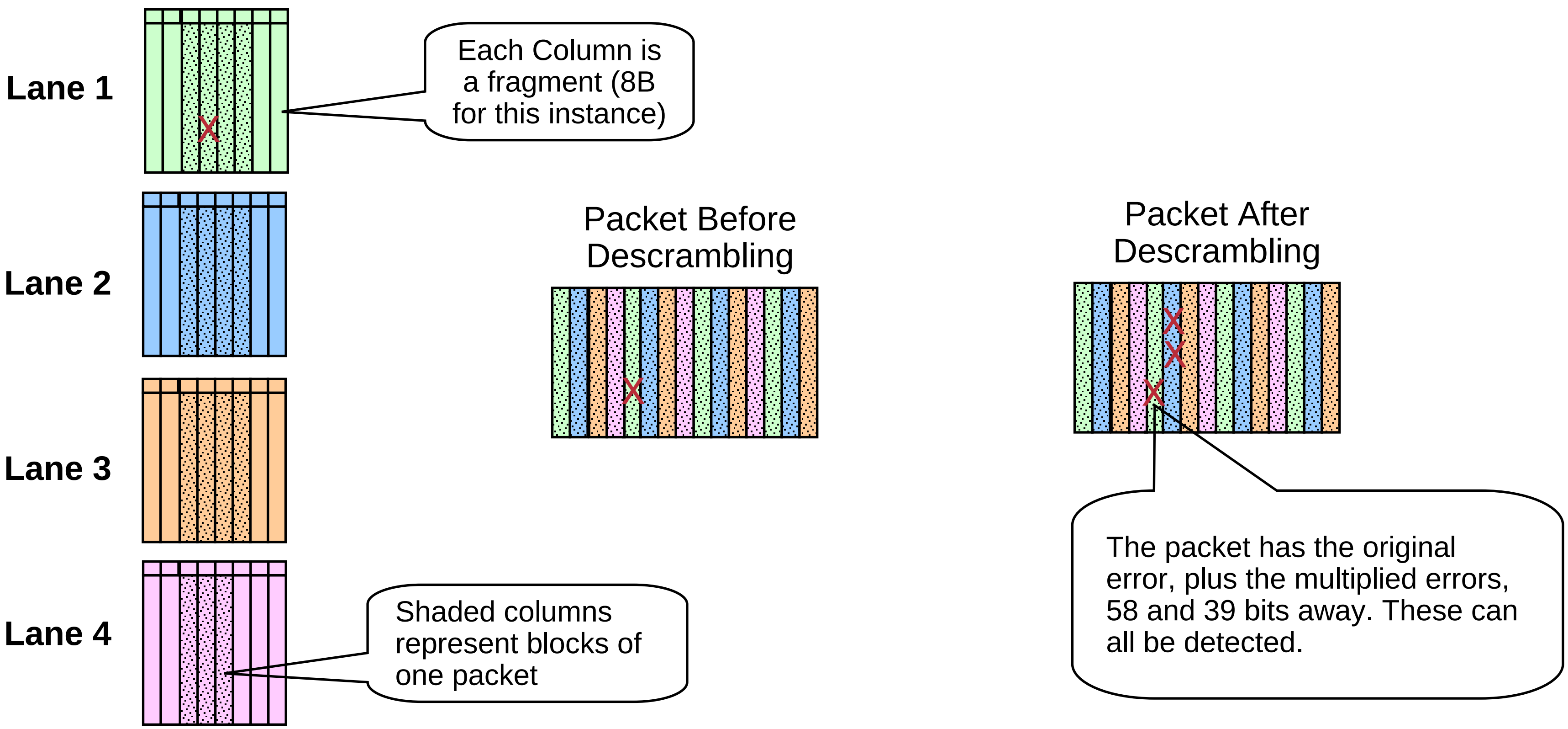
- The PCS/MLD layers have the following flow of functionality:
  1. Encoding (64B/66B)
  2. Scrambling ($x^{58}+x^{39}+1$)
  3. Striping of the data to multiple lanes from an aggregate stream
  4. De-striping of the data from multiple lanes to an aggregate stream
  5. Descrambling of the data
  6. Decoding (64B/66B)

- This is important, since the packet is reconstructed before descrambling, the multiplied errors are right where the scrambler polynomial says they should be (gustlin_01_1107)
- This simplifies the MTTFPA analysis greatly, it is the same as 10GBASE-R for random and independent errors

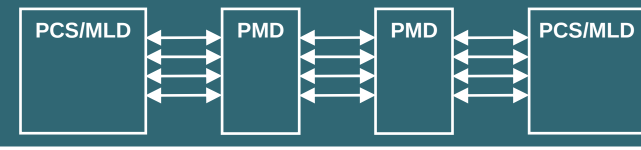
40GE – Single Bit Error



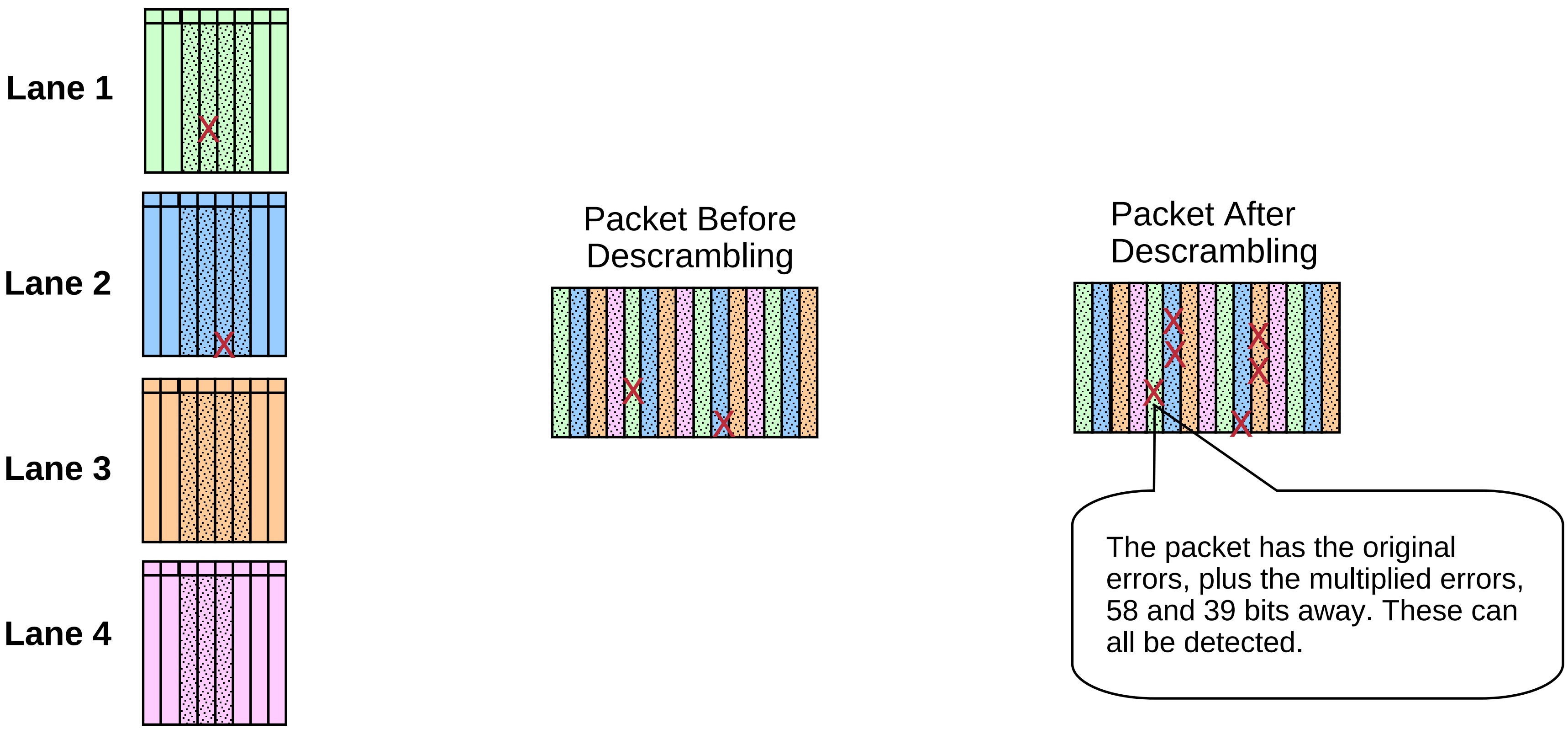
- Packet is re-constructed before descrambling
- The error is multiplied and becomes 3 errors
- All 3 bit errors are 100% detectable
- Same behavior as 10GBASE-R



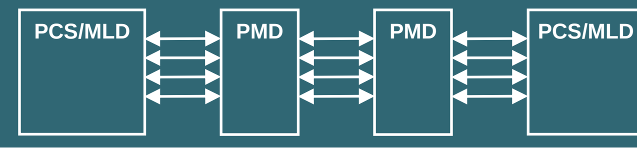
40GE – Two Bit Errors



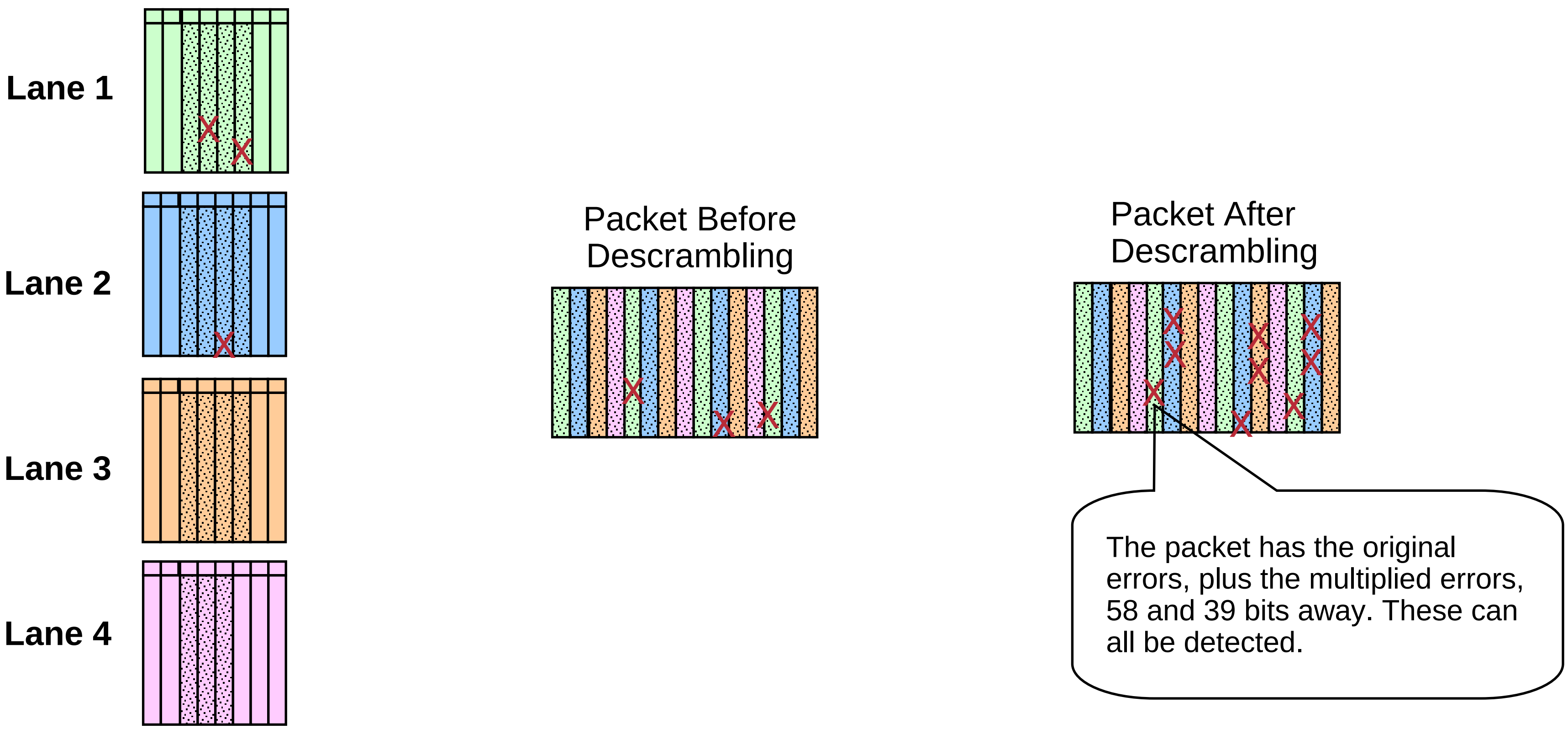
- Packet is re-constructed before descrambling
- The two independent bit errors are multiplied and become 6 errors
- Since the original 2 bit error is detectable, the multiplied errors are also 100% detectable
- Same behavior as 10GBASE-R



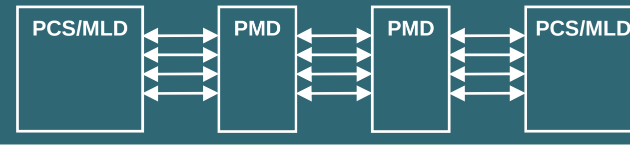
40GE – Three Bit Errors



- Packet is re-constructed before descrambling
- The three independent bit errors are multiplied and become 9 total errors
- Since the original 3 bit error is detectable, the multiplied errors are also 100% detectable
- Same behavior as 10GBASE-R



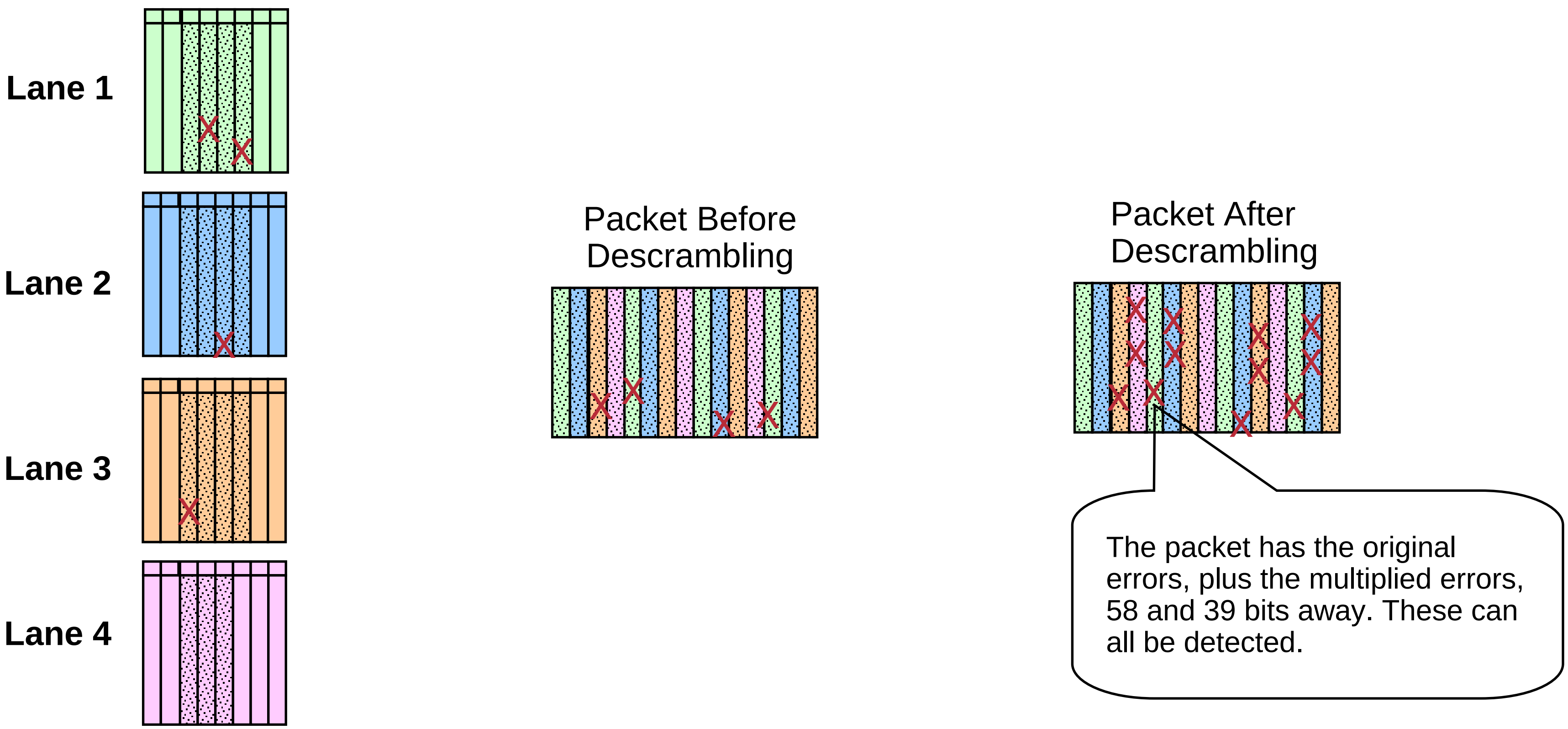
40GE – Four Bit Errors



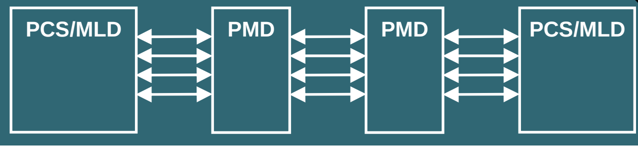
- Packet is re-constructed before descrambling
- The four independent bit errors are multiplied and become 12 total errors
- The original 4 bit error is not 100% detectable, the multiplied errors have the same detectability

  Probability of detecting the 4 bit (or the multiplied 12 bit) error is $(1-1/2^{32})$

- Same behavior as 10GBASE-R

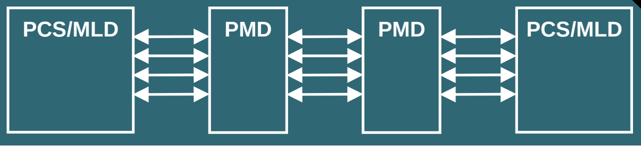


40GE Summary

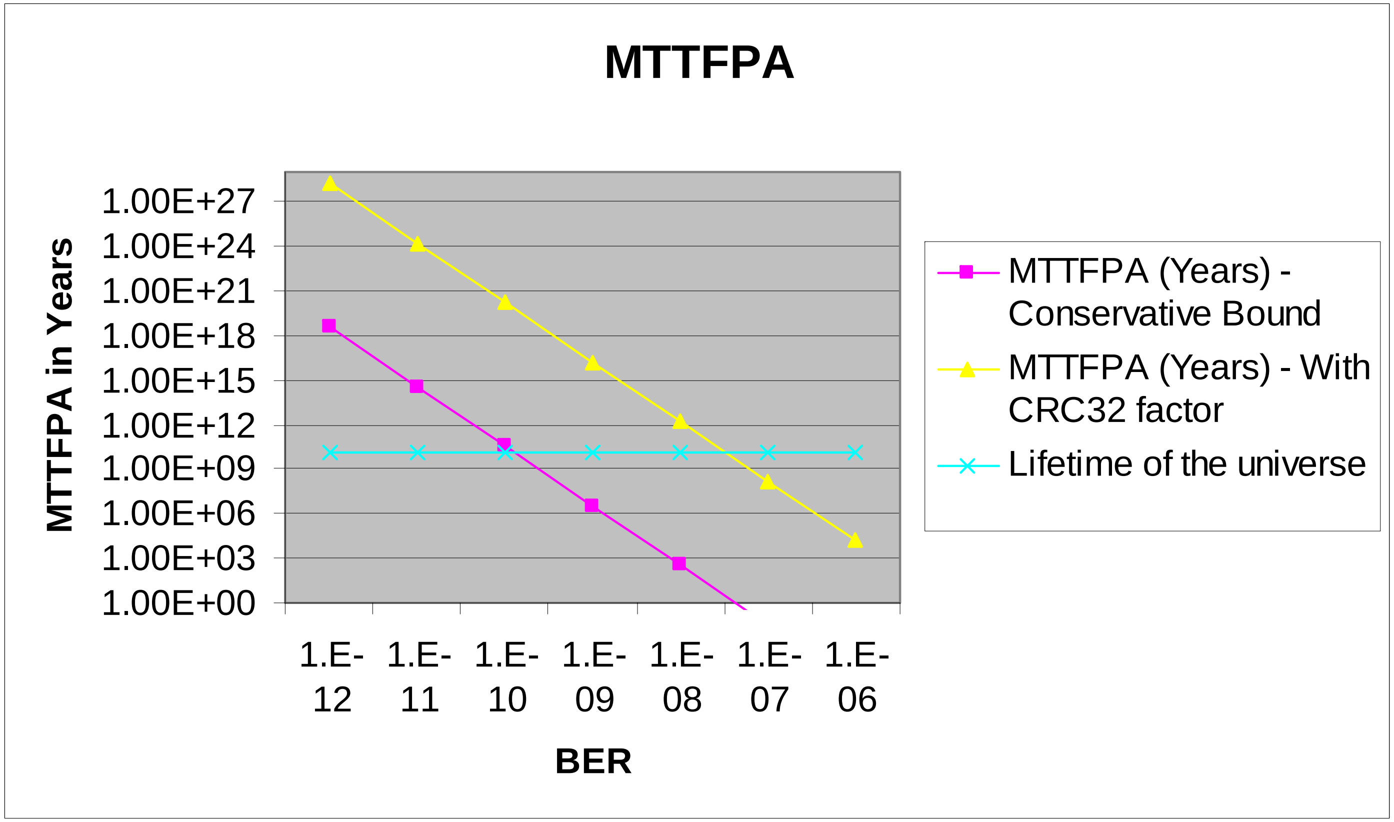


- Same error detectability as in 10GBASE-R
- No degradation due to the scrambler error multiplication
- This is due to scrambling before data is distributed, and descrambling after data is reassembled
- Corner cases such as error spill in and spill out are the same as 10GBASE-R so the analysis done for it applies here as well
- Still need to determine the probability of non random errors on both the electrical and the optical interfaces
    - Once this is understood then we can include that in this analysis

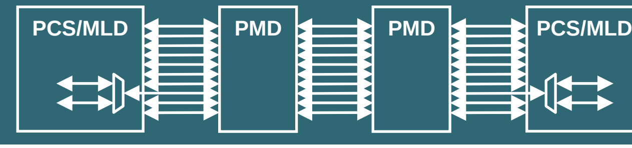
40GE MTTFPA



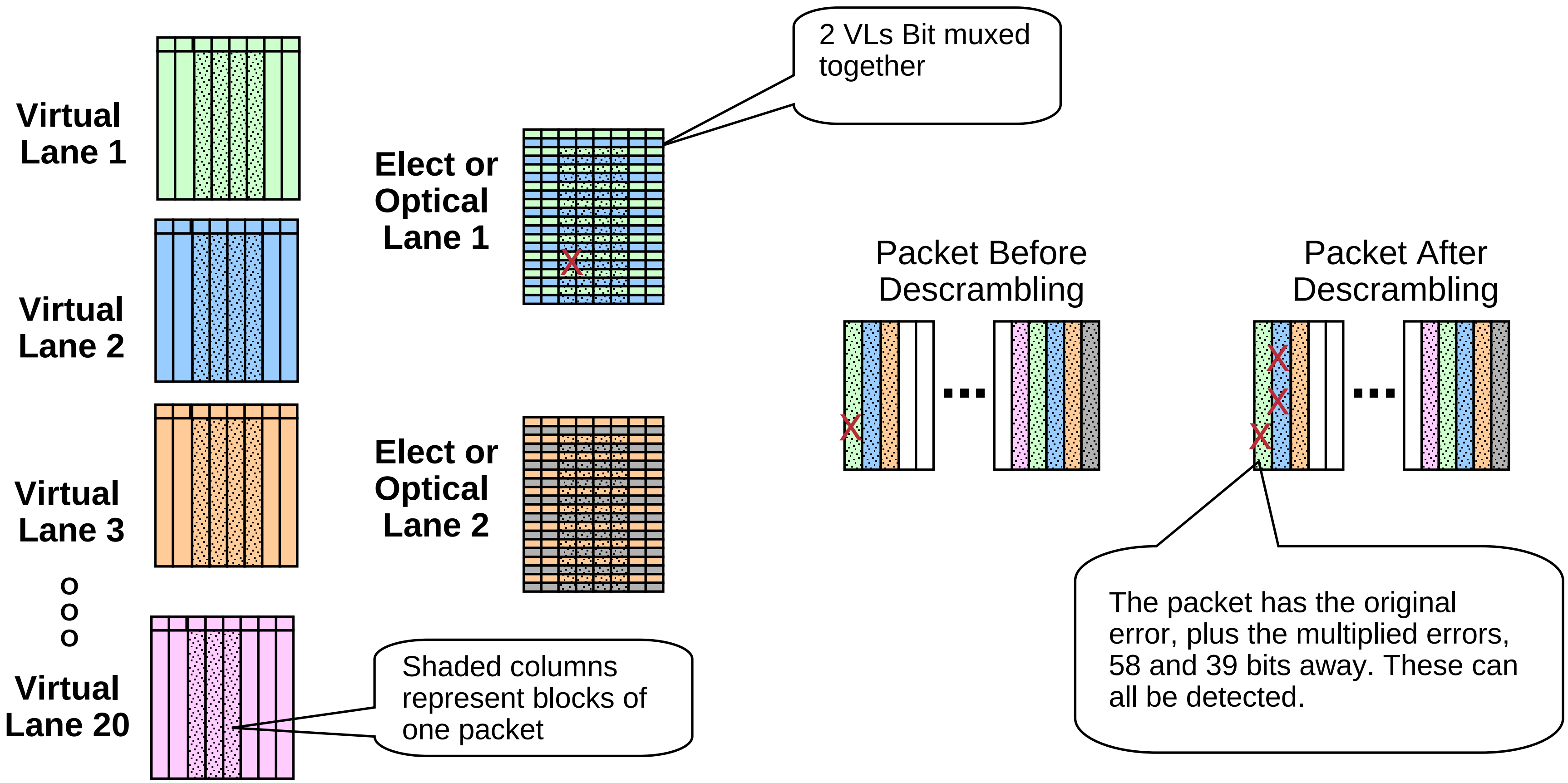
- 1, 2, and 3 bit errors are all 100% detectable with the IEEE CRC32
- 4 bit errors rely on the probability of catching errors with the CRC32
- Probability of 4 uncorrelated random errors is: $1x10^{-33}$ with BER of 10^{-12}
- Non random errors are not accounted for in this graph



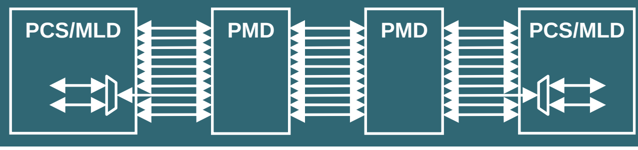
100GE (10:10) – Single Bit Error



- Packet is re-constructed before descrambling
- The error is multiplied and becomes 3 errors
- All 3 bit errors are 100% detectable
- Same behavior as 10GBASE-R



100GE (10:10)– Two Bit Errors



- Packet is re-constructed before descrambling
- The two independent bit errors are multiplied and become 6 errors
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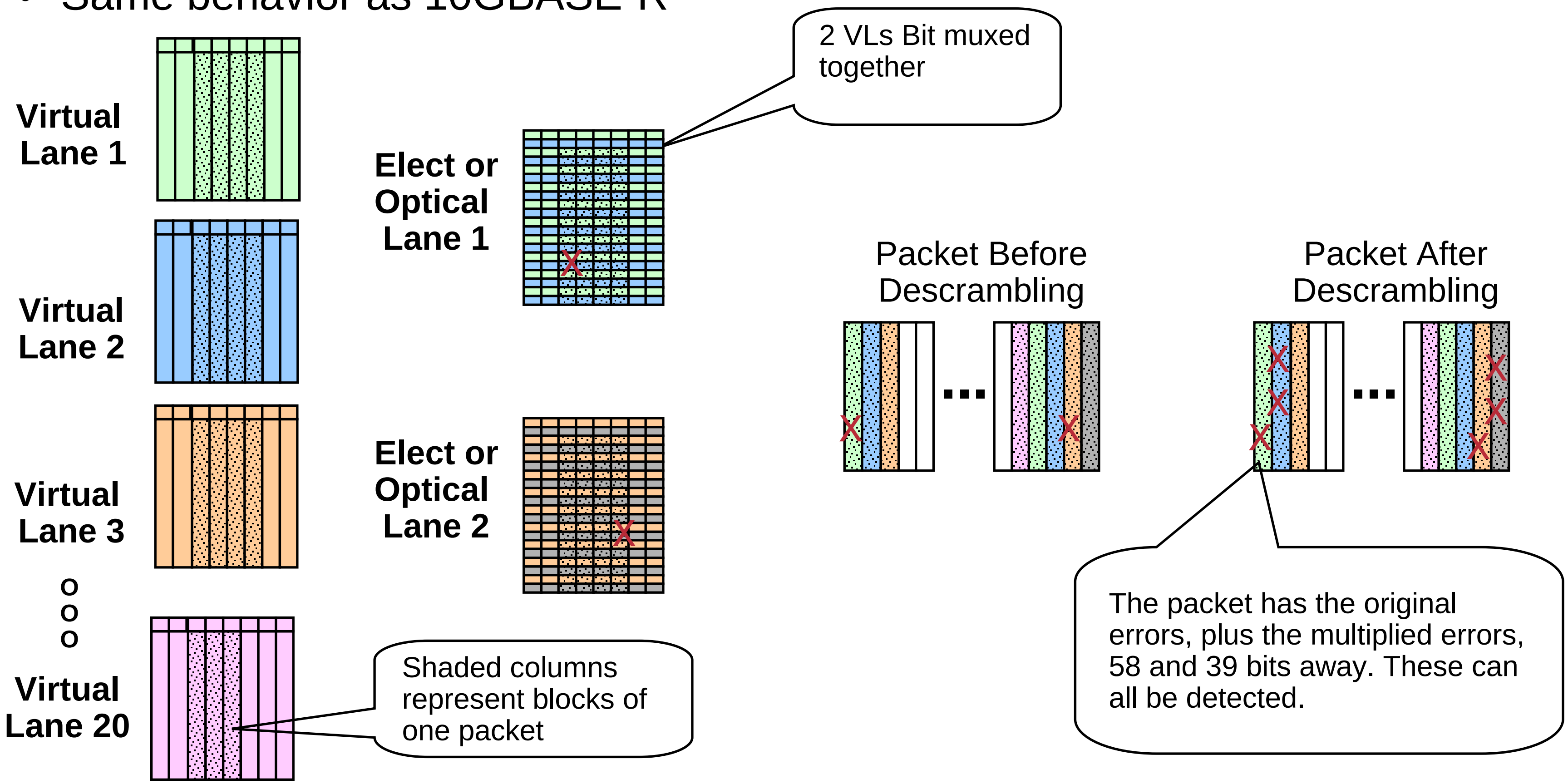

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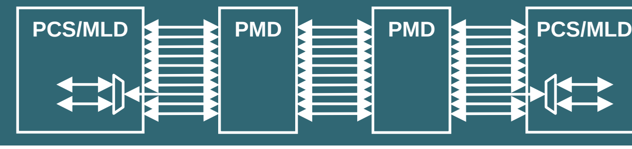

- Packet is re-constructed before descrambling
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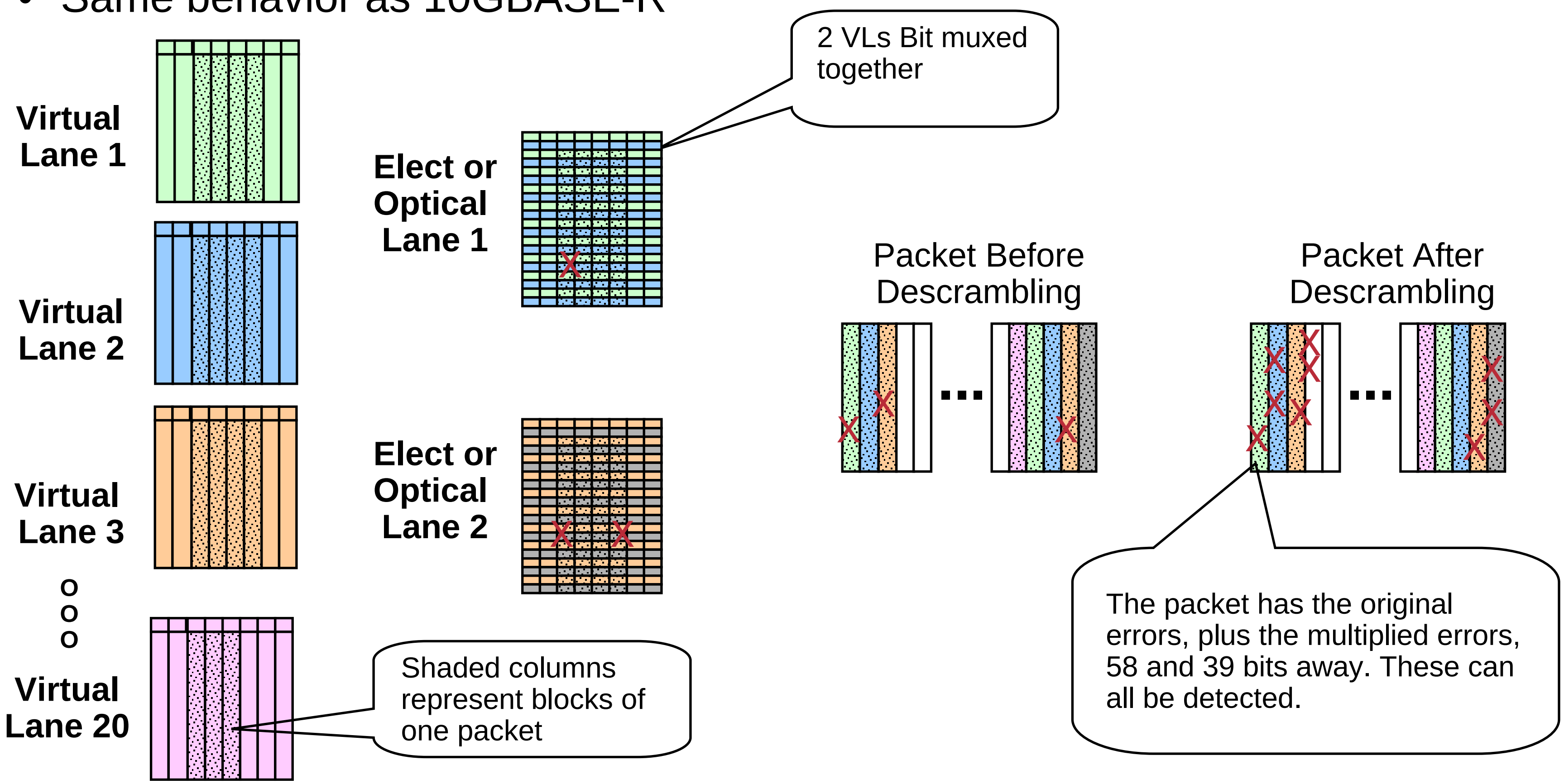

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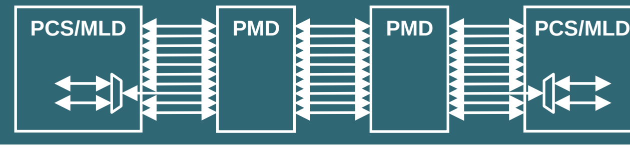
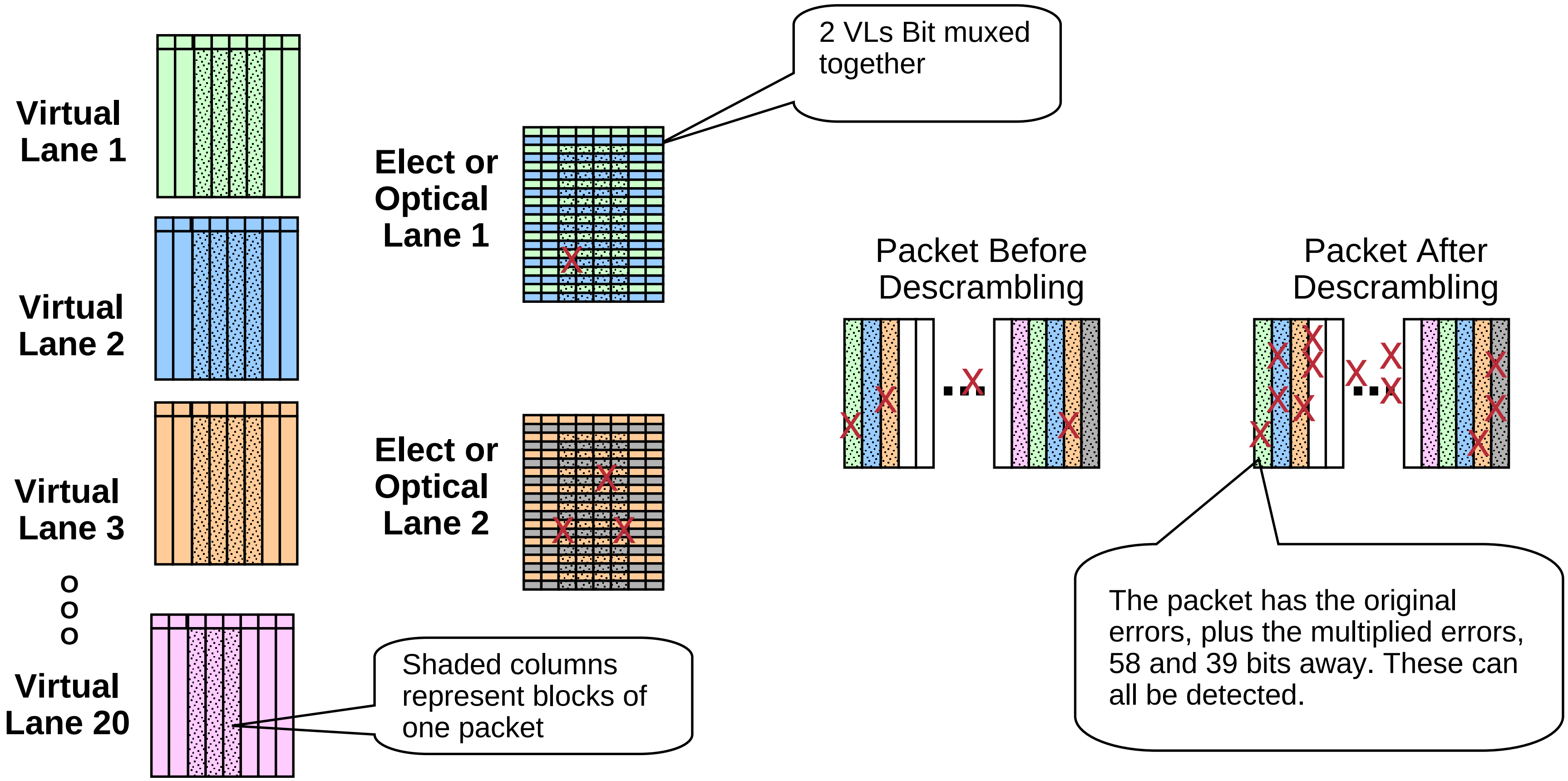
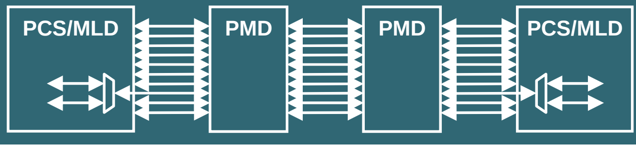


- The four independent bit errors are multiplied and become 12 total errors
- The original 4 bit error is not 100% detectable, the multiplied errors have the same detectability

  Probability of detecting the 4 bit (or the multiplied 12 bit) error is $(1-1/2^{32})$
- Same behavior as 10GBASE-R



100GE (10:10) Summary



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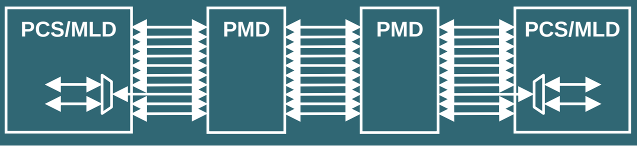
100GE (10:10) MTTFPA



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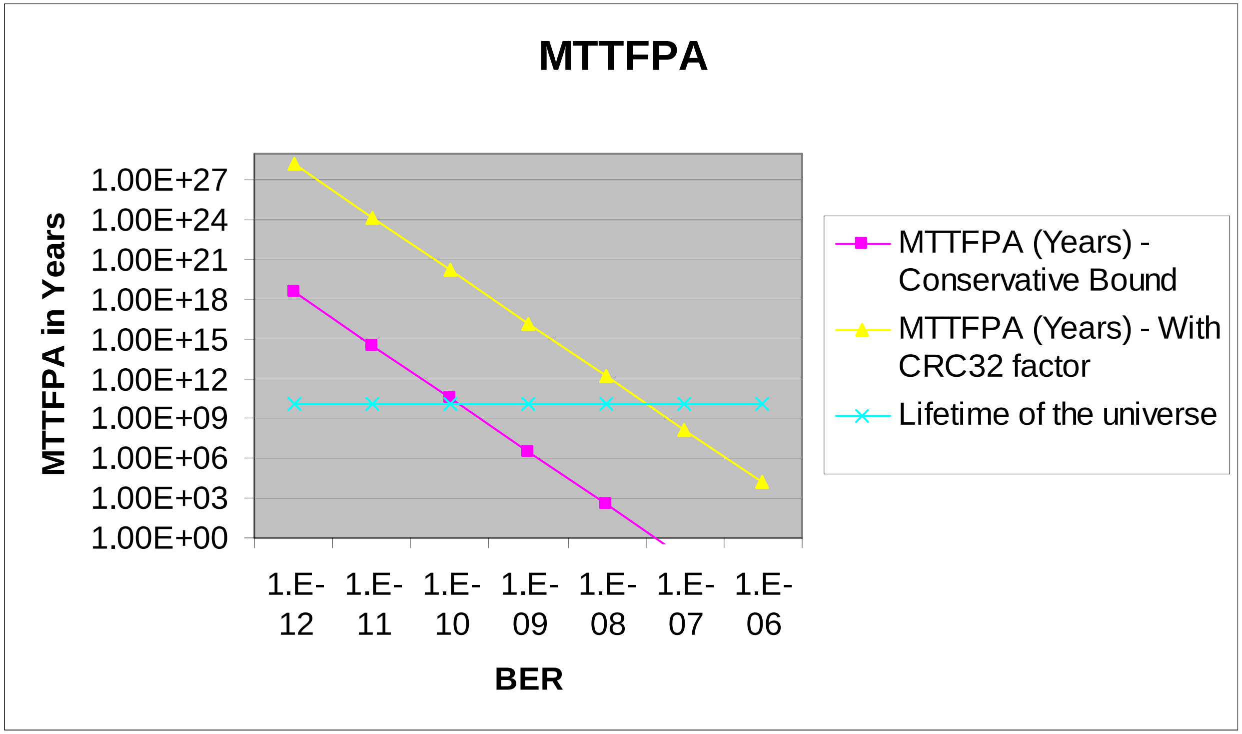
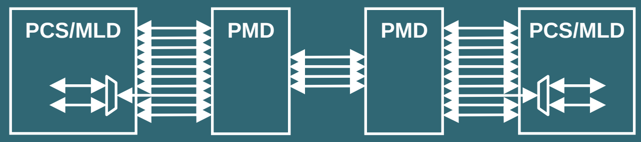


100GE (10:4) – Single Bit Error



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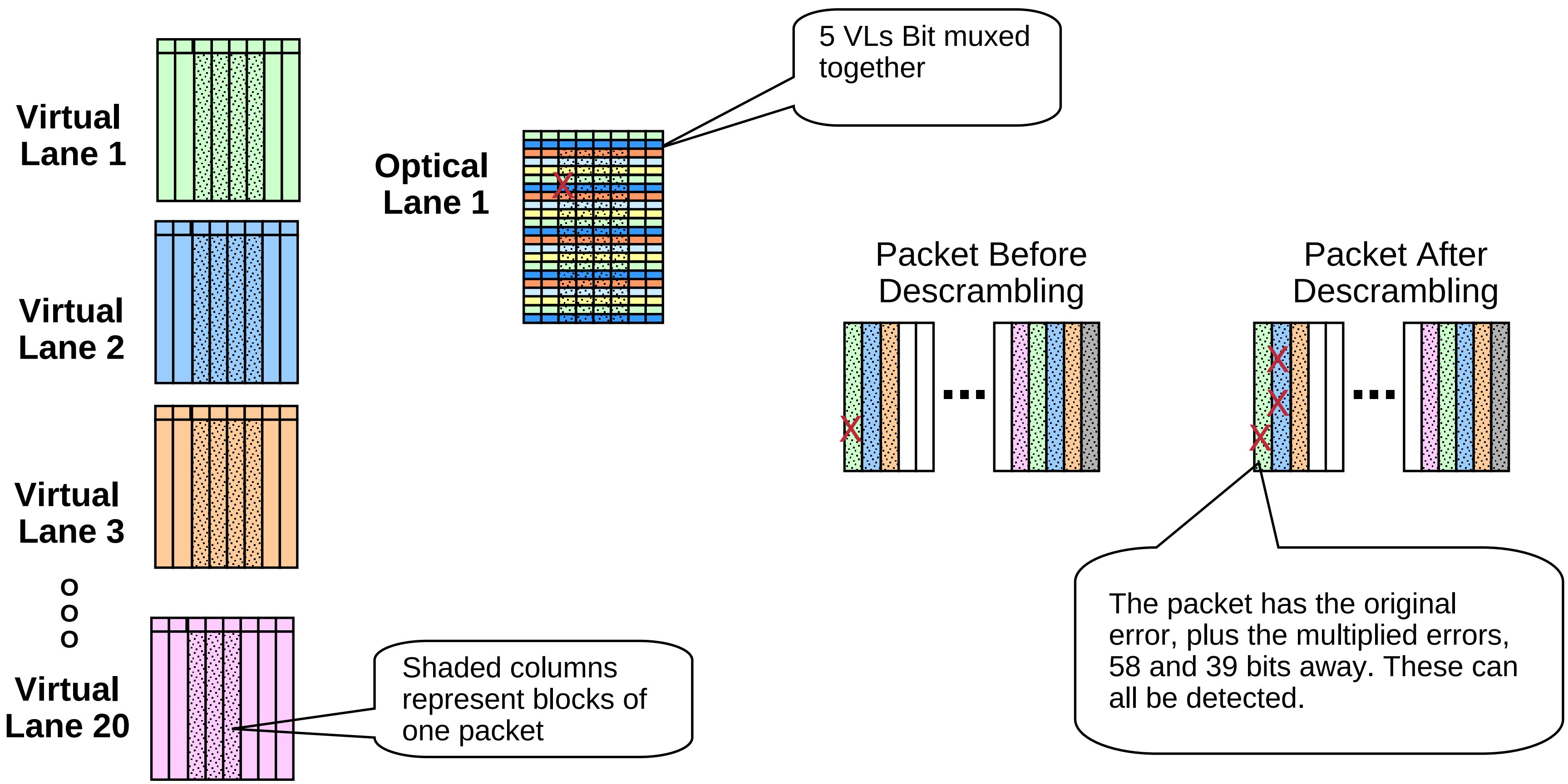
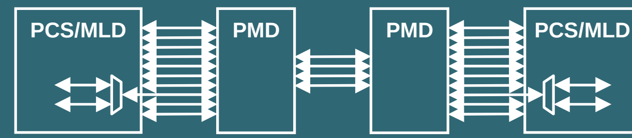


100GE (10:4) – Two Bit Errors



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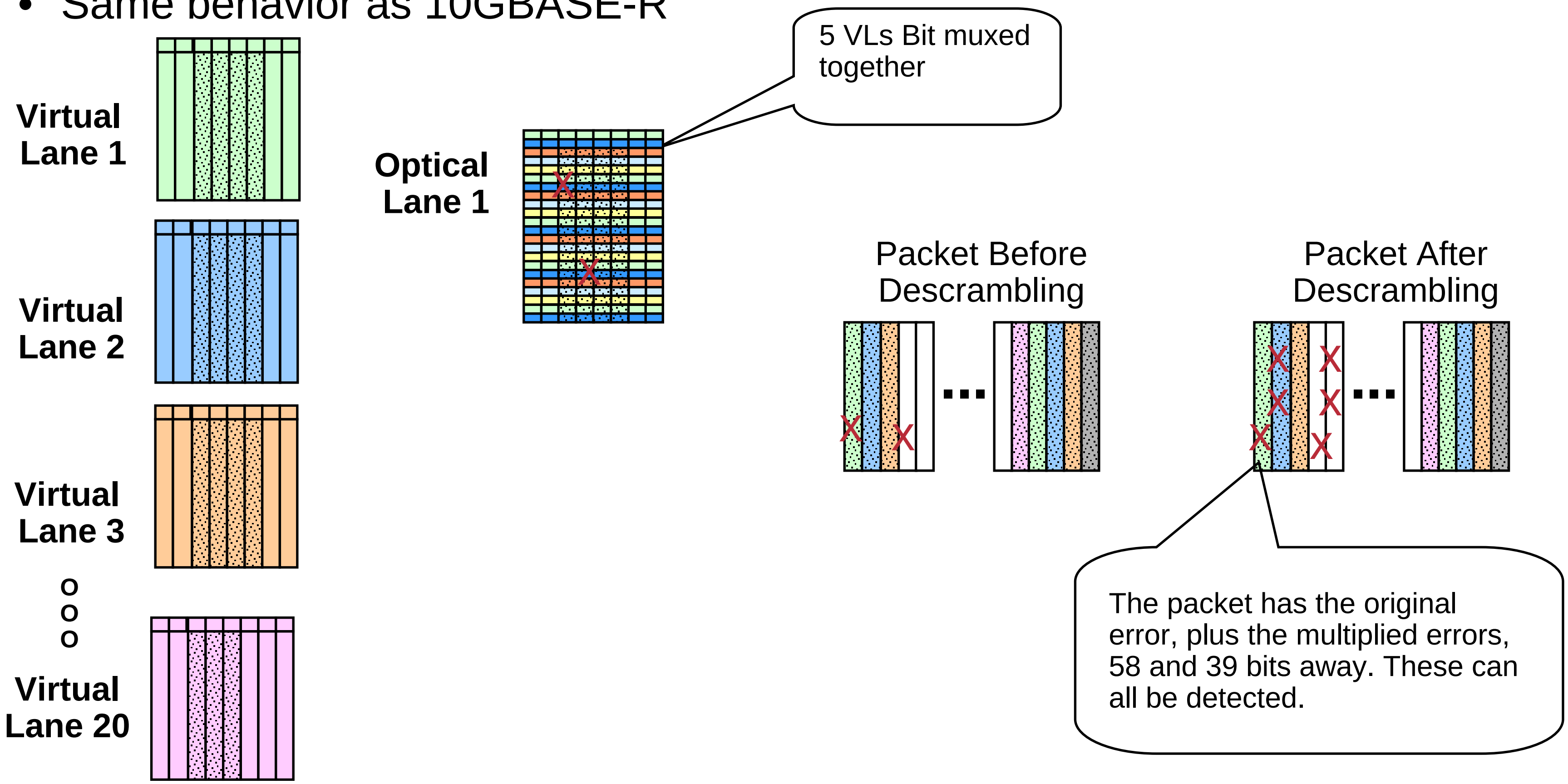
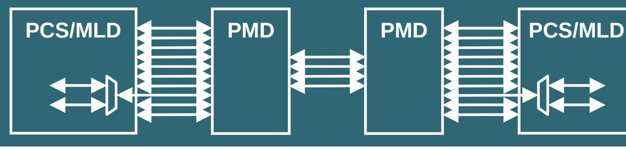


100GE (10:4) – Three Bit Errors



- Packet is re-constructed before descrambling
- The three independent bit errors are multiplied and become 9 errors
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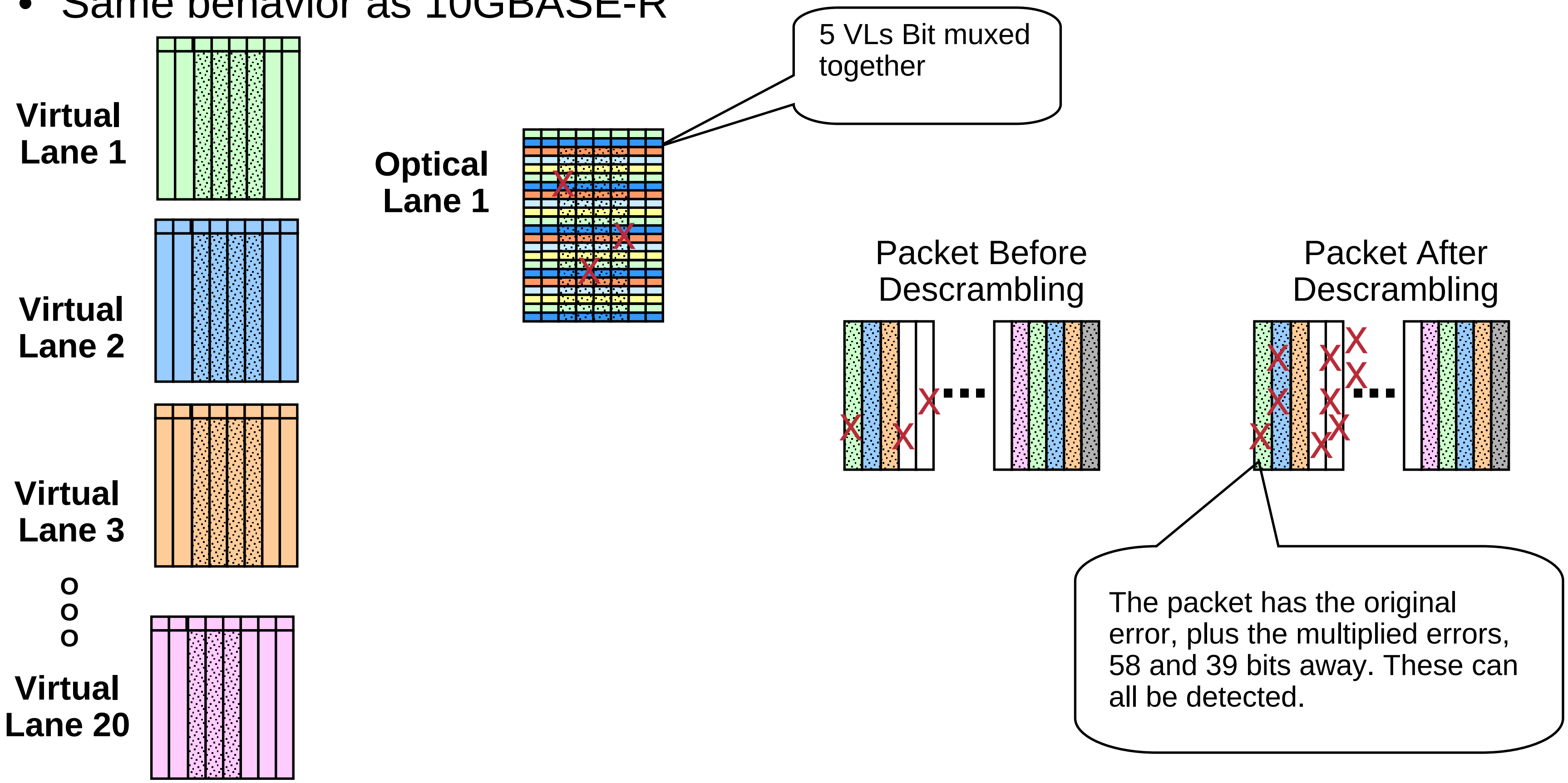
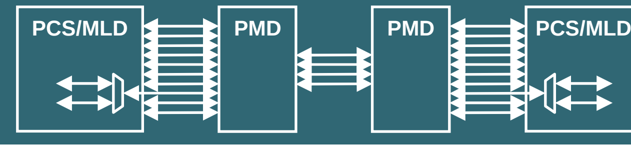


100GE (10:4) – Four Bit Errors



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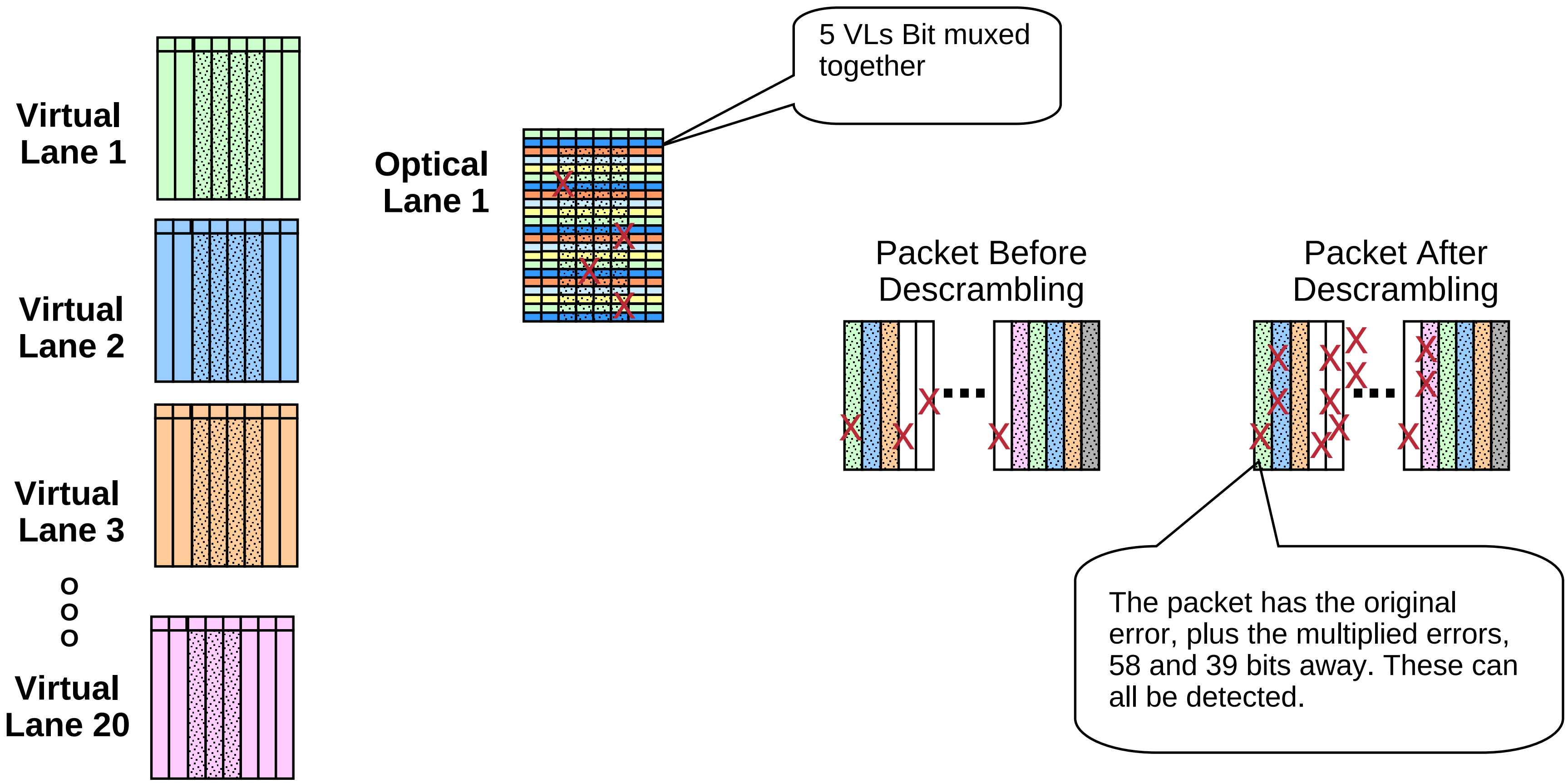
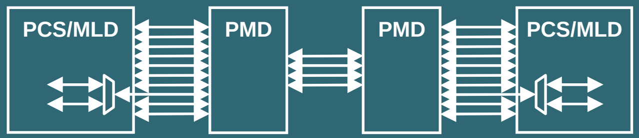


100GE (10:4) Summary



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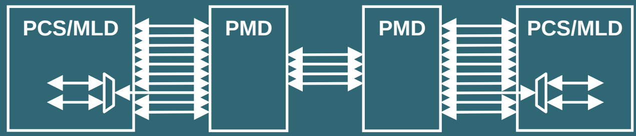
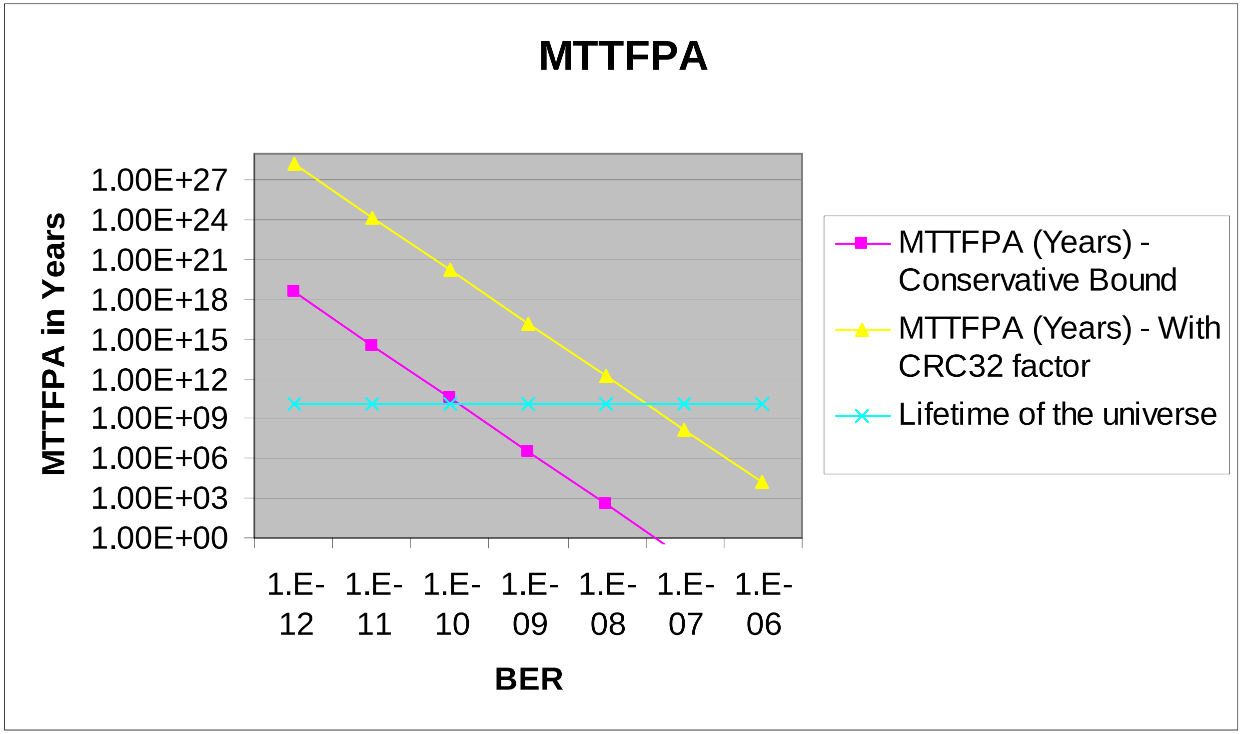
- This is due to scrambling before data is distributed and descrambling after data is reassembled
- Corner case such as error spill in and spill out are the same as 10GBASE-R so the analysis done for it applies here as well
- Still need to determine the probability of non random errors on both the electrical and the optical interfaces
  - Once this is understood then we can include that in this analysis

100GE (10:4) MTTFPA

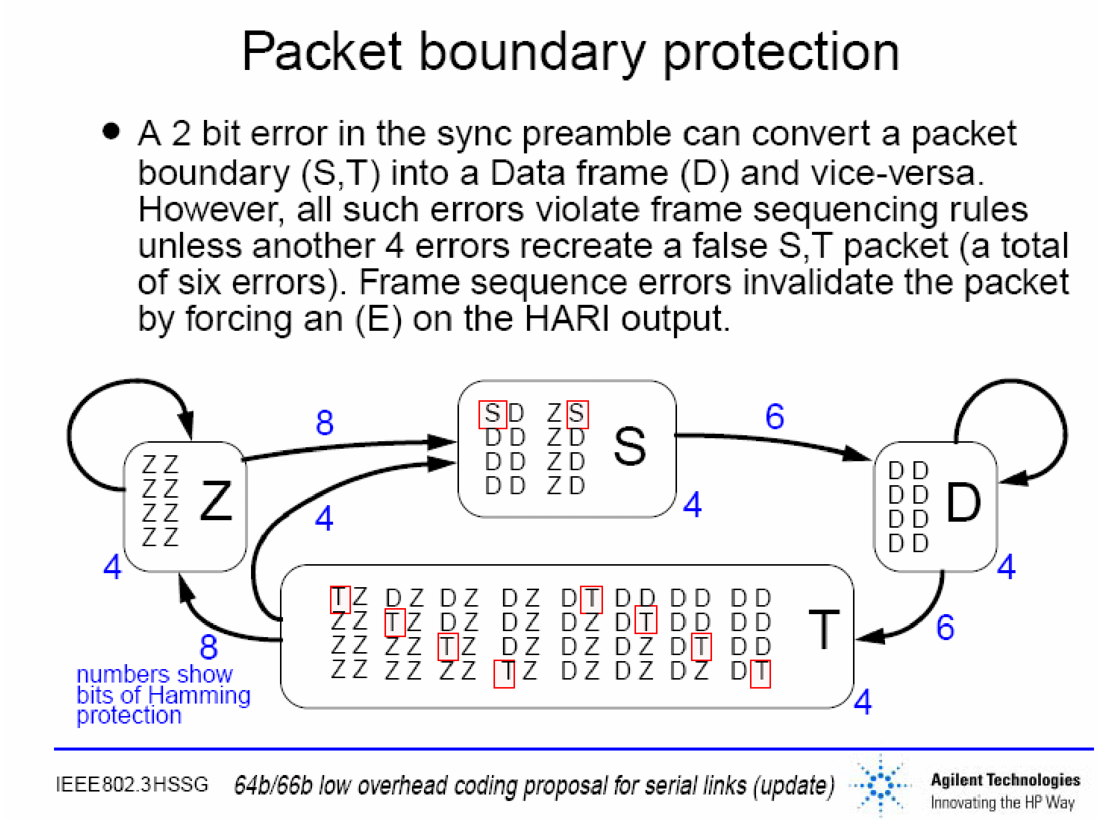


- **1, 2, and 3 bit errors are all 100% detectable with the IEEE CRC32**
- **4 bit errors rely on the probability of catching errors with the CRC32**
- **Probability of 4 uncorrelated random errors is: 1×10^{-33} with BER of 10^{-12}**
- **Non random errors are not accounted for in this graph**



Packet Boundary Protection

- For uncorrelated errors the analysis is the same as it was for 10GBASE-R since MLD uses the same PCS just running at 10x or 4x the speed
- Therefore we can conclude that the 4 bit packet boundary protection that was shown in walker_1_0100 holds for MLD



MTTFPA Next Steps and Summary

- For random errors, the MTTFPA analysis is the same as for 10GBASE-R
- MTTFPA is in the range of many billions of years
- Next Steps
  - Analyze the likelihood of burst errors on the electrical interface and incorporate that into this analysis (EDC would impact this analysis)
  - Continue to analyze the likelihood of burst errors on the single mode 100G optical interface
  - Analyze the likelihood of burst errors on the 100G multi mode optical interface
  - Once we have probabilities for different burst errors sizes we can revise our MTTFPA including this information

References

1. **P. E. Boudreau et al.,** ***Performance of a cyclic redundancy check and its interaction with a data scrambler,*** **IBM J. RES. DEVELOP. VOL. 38 NO. 6 NOVEMBER 1994**
2. **Norival Figueira,** ***Impact of the*** $X^{43}+1$ ***scrambler on the Error Detection Capabilities of the Ethernet CRC*****, IEEE 802.3 HSSG Meeting, Montreal, July 5-9, 1999**
3. **Pete Anslow,** ***Error Distribution in Optical Links*****, IEEE 802.3 HSSG, Atlanta, November 2007**
4. **Raj Jain,** ***Error Characteristics of FDDI*****, July 25th, 1990**
5. **Rick Walker,** ***64b/66b low-overhead coding proposal for serial links*****, walker_1_0100, 1/12/00**