

OTN Support for High Speed Ethernet

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Provide appropriate support for OTN

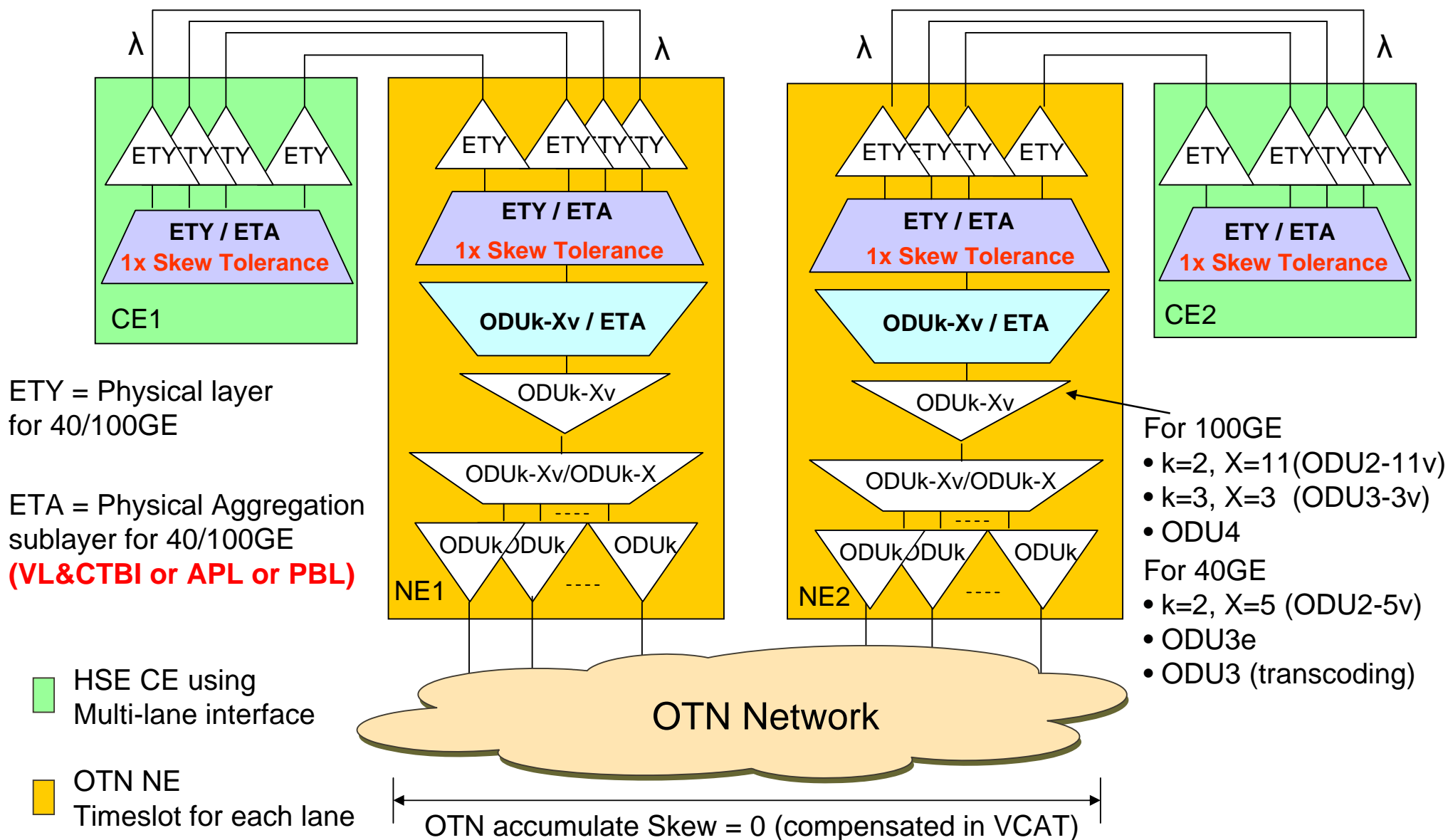
- Provide Physical Layer specifications which support 100 Gbps operation over
 - at least 10m over a copper cable assembly
 - at least 100m on OM3 MMF
 - at least 10km over SMF and at least 40km Over SMF
- Provide Physical Layer specifications which support 40 Gbps operation over
 - at least 100m on OM3 MMF
 - at least 10m over a copper cable assembly
 - at least 1m over a backplane

	40GE	100GE	OTN support (skew tolerance)
At Least 1m Backplane	4x10G KR		
At least 10m Cu Cable	4x10G T	10x10G T	Outside the scope of this discussion
At least 100m OM3 MMF	4x10G Array	10x10G Array	Discussed in this presentation
At least 10km SMF		4 x 25G Array	Discussed in this presentation
At least 40km SMF		4 x 25G Array	Discussed in this presentation

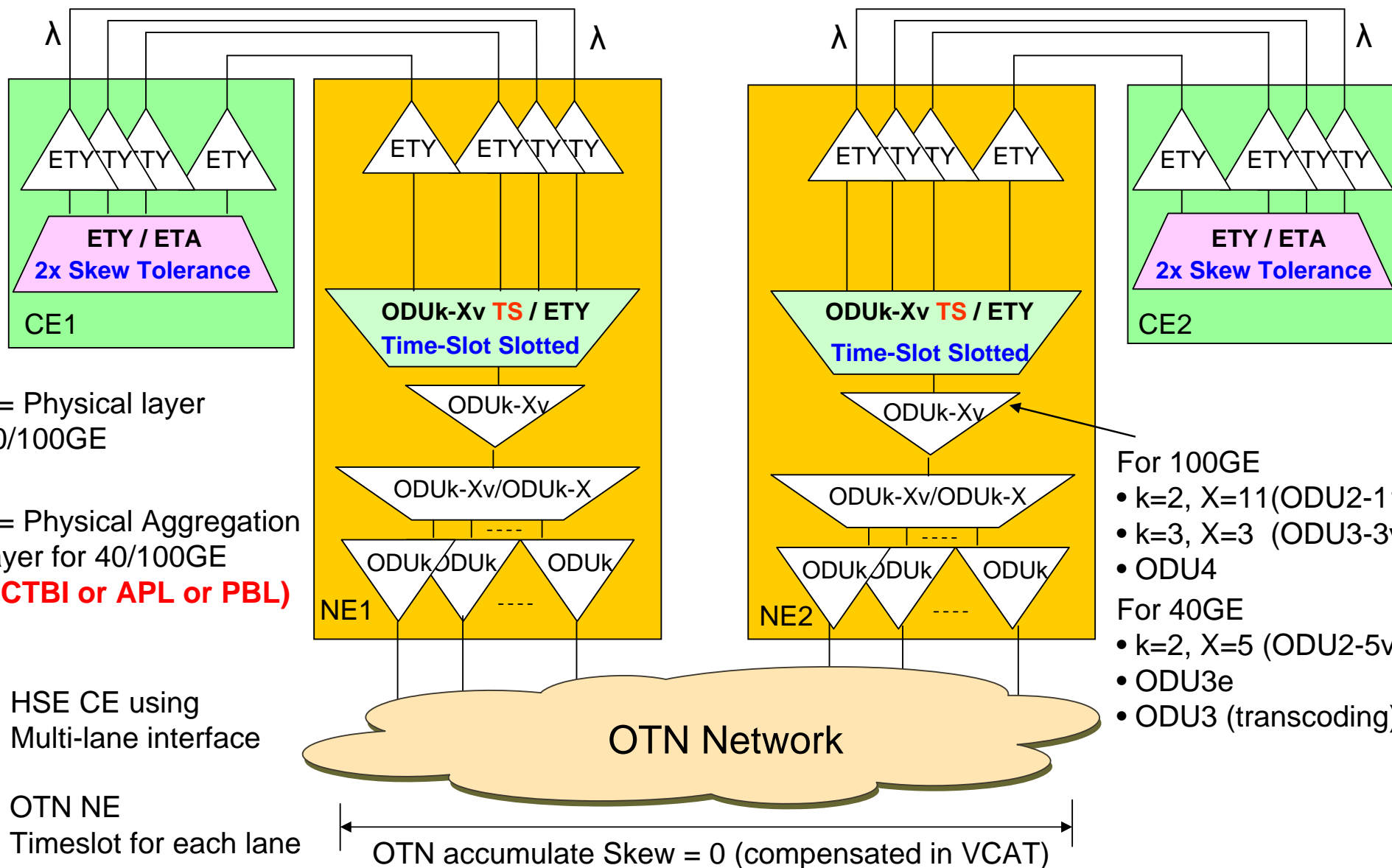
HSE OTN Transport Models

- **HSE Link-Aggregate OTN Transport Model**
 - The OTN Transport should not depend on the Ethernet PMD or the number of lanes, and be free to use different Ethernet PMDs at Ingress and Egress of OTN network (trowbridge_02_0907, trowbridge_01_1107).
 - Using a Uniform PCS architecture and HSE Link-aggregate OTN Transport would require termination of the multi-lane interface and aggregation of the lane data streams after finishing multi-lane skew compensation.
- **HSE Lane-Independent OTN Transport Model**
 - The OTN Transport should not depend on the Ethernet PCS and HSE multi-lane distribution architecture, and should support Bit Rate Agnostic Constant Bit Rate Transparency Transport. This would reduce the system complexity for HSE Support over OTN.
 - OTN transport skew will not accumulate in the Multi-lane LAN interface, VCAT skew and path differential delay will be compensated by VCAT in OTN. However, the LAN interface multi-lane skew will accumulate until the LAN interface lane aggregation destination point, so a 2x skew buffer is need.
- **Each Model accommodates different applications and requirements.**

HSE Link-Aggregate Transport Model



HSE Lane-Independent Transport Model



ETY = Physical layer for 40/100GE

ETA = Physical Aggregation sublayer for 40/100GE (VL&CTBI or APL or PBL)

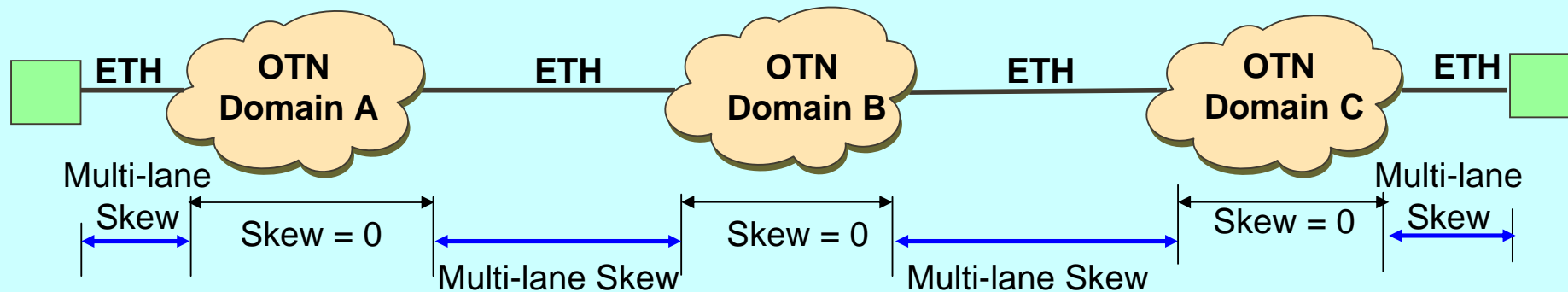
■ HSE CE using Multi-lane interface

■ OTN NE Timeslot for each lane

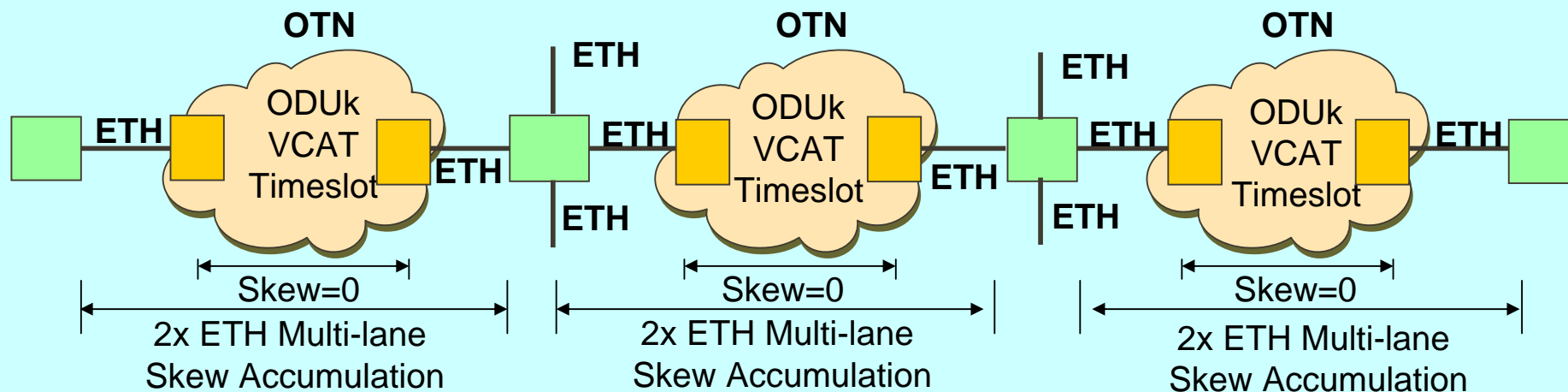
- For 100GE
 - k=2, X=11 (ODU2-11v)
 - k=3, X=3 (ODU3-3v)
 - ODU4
- For 40GE
 - k=2, X=5 (ODU2-5v)
 - ODU3e
 - ODU3 (transcoding)

Skew accumulation

Why not use an OTN link for the inter-domain interconnection ?



Multi-lane LAN Interface skew accumulation?



The most typical application scenario: the biggest skew accumulation is 2x!

OTN NE, Timeslot for each lane

Ethernet CE using Multi-lane interface

LAN Interface Skew Tolerance

	PMD type	1x Skew (Per Lane)	1x Buffer Size (Per Lane)	2x Buffer Size (Per Lane)
40GE 4x10G MMF 100m	4 ribbon fiber, 850nm	1.94ns (#1)	20 Bits	40 Bits
100GE 10x10G MMF 100m	10 ribbon fiber, 850nm	20 UI	20 Bits	40 Bits
40GE 4x10G MMF 100m	4 ribbon fiber, 850nm	<<10ns (#2)	100 Bits	200 Bits
100GE 10x10G MMF 100m	10 ribbon fiber, 850nm	100 UI	100 Bits	200 Bits
100GE 4x25G SMF 40km	IEEE LX4 CWDM (1275.7, 1300.2, 1324.7, 1349.2nm)	151.4 UI (#3)	152 Bits	304 Bits
	ITU-T CWDM near 1310nm (1291,1311,1331,1351 nm)	151.6 UI (#4)	152 Bits	304 Bits
	ITU-T DWDM 400G Grid Near 1310nm (1308-1316 nm)	9.1 UI (#5)	12 Bits	24 Bits

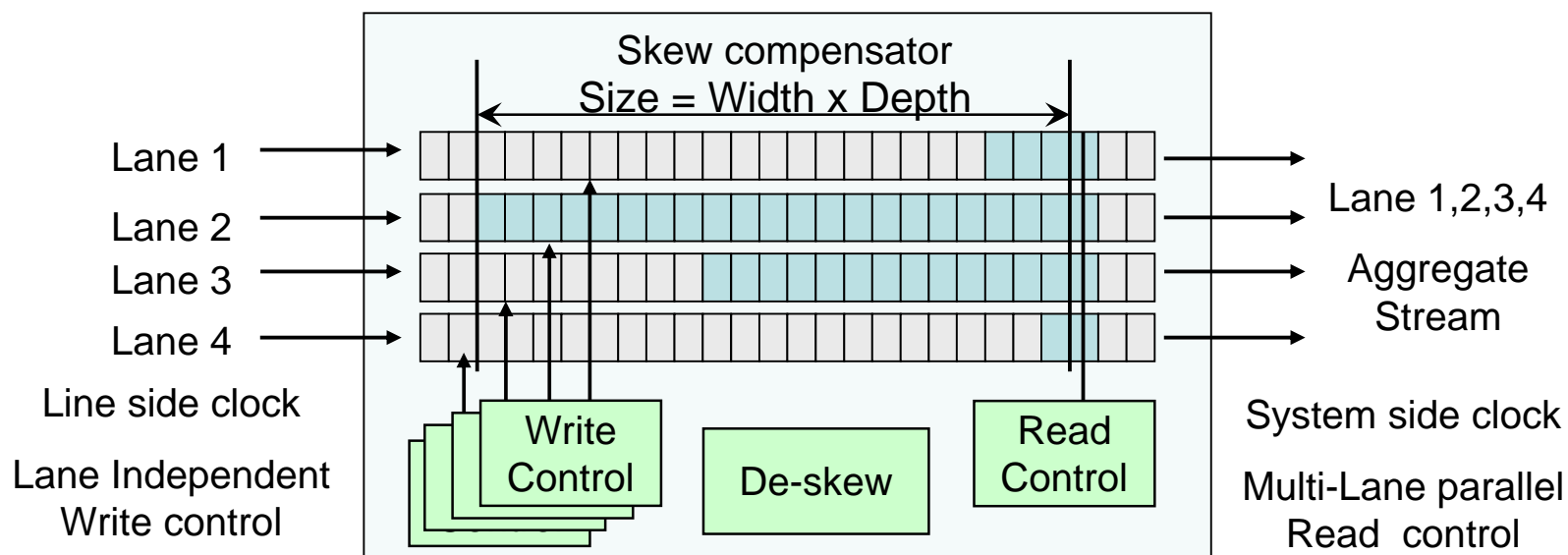
Note: The Total Link Skew Compensation Buffer RAM Size Requirement = # of Lanes x PerLaneSkewUI

(#1)(#2) MMF Ref: nishimura_01_0906; nishimura_01_1106; The Experimental Result was 5.8ns@300m. = 1.94ns@100m In nishimura_01_1106, the Max skew was considered <<30ns@300m, 30ns was the limit of the ribbon fiber skew. Here we think that 5.8@300m would be more reasonable.

(#3)(#4)(#5)SMF Ref: anslow_02_1107.pdf, anslow_03_1107.xls; the spreadsheet included the above three WDM options, the results (#3), (#4),(#5) are from the spreadsheet.

Worst Case 2x Buffer Size example

- **Max 2x Buffer RAM Size Per Lane = 304bits ~ 320bits = 40 Bytes**
 - If the system side Digital Logic is an 80-bit bus @ 312.50 MHz (80bit x 312.5MHz=25G)
 - The Buffer width is 10 bytes (80 bits), so a 40-byte buffer has a depth of 4
 - If the system side Digital Logic is a 160-bit bus @ 156.25 MHz (160bit x 156.25MHz=25G)
 - The Buffer width is 20 bytes (160 bits), so a 40-byte buffer has a depth of 2
- **A 4-lane de-skew buffer with a small depth such as 2, 3 or even 4 will not work well. So the Multi-lane HSE system side skew compensator may require a de-skew buffer far greater than the 2x requirement calculated here.**



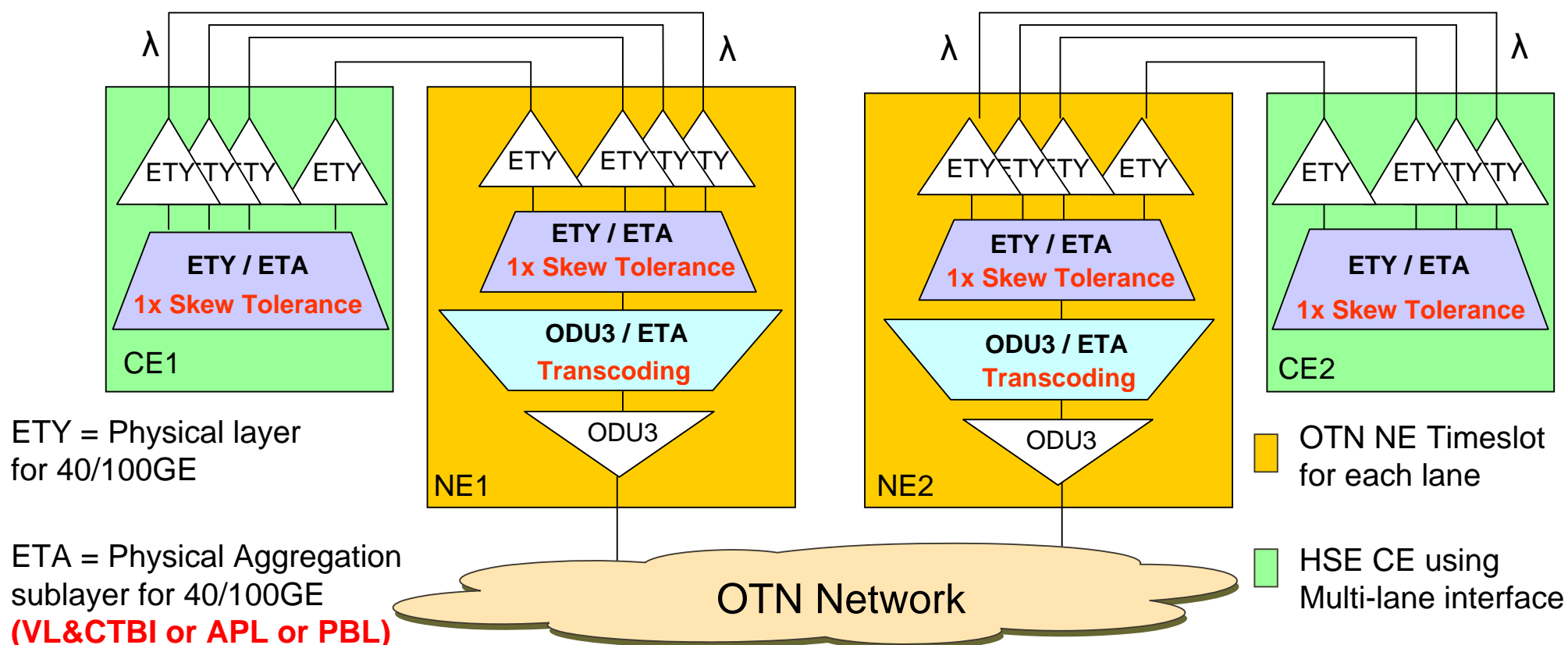
Comparing OTN Transport Support Models

	Link-Aggregate Transport Model	Lane-Independent Transport Model
Transparency	(ETA Aware) Standard PCS Codeword Transparency	Bit Transparency (Bit Rate Agnostic) Standard PCS Codeword Transparency
LAN De-skew	Need to do multi-lane skew compensation at the OTN ingress	Do not need to do Multi-lane skew compensation at the OTN ingress
OTN Skew	No OTN Skew or OTN Skew Compensated in OTN domain in VCAT	No OTN Skew or OTN Skew Compensated in OTN domain in VCAT
Alignment Marker Process	Many Options: Remove or Keep	Only one Option: Keep the alignment marker, Full Speed Transparency
Complexity	Higher	Lower
Standards Work	More and complex, standards work in ITU-T will be delayed until IEEE 802.3ba is completed	Less and simple, ITU-T and IEEE could work in parallel
Summary	Both The Lane-Independent and Link-Aggregate Models could be used to accommodate different applications and requirements.	

40GE OTN support consideration

- **40GE OTN support Options:**
 - **For current 4x10G 40GE multi-lane interface**
 - Lane-Independent Mapping into 4 slots slotted ODU3e
 - Lane-Independent Mapping into 4 slots slotted ODU2-5v
 - Lane-Independent Mapping into 4 slots slotted ODU3 (Lane Transcoded)
 - Link-Aggregate Mapping into ODU3 (Aggregate Transcoded)
 - **For Possible Future 40GE Serial interface**
 - Directly mapping into ODU3e
 - Directly mapping into ODU2-5v
 - Mapping into ODU3 (Transcoded)
- **For 4x10G Multi-lane 40GE mappings into standard ODU3 using transcoding**
 - the Lane-Independent and Link-Aggregate Models need further discussion

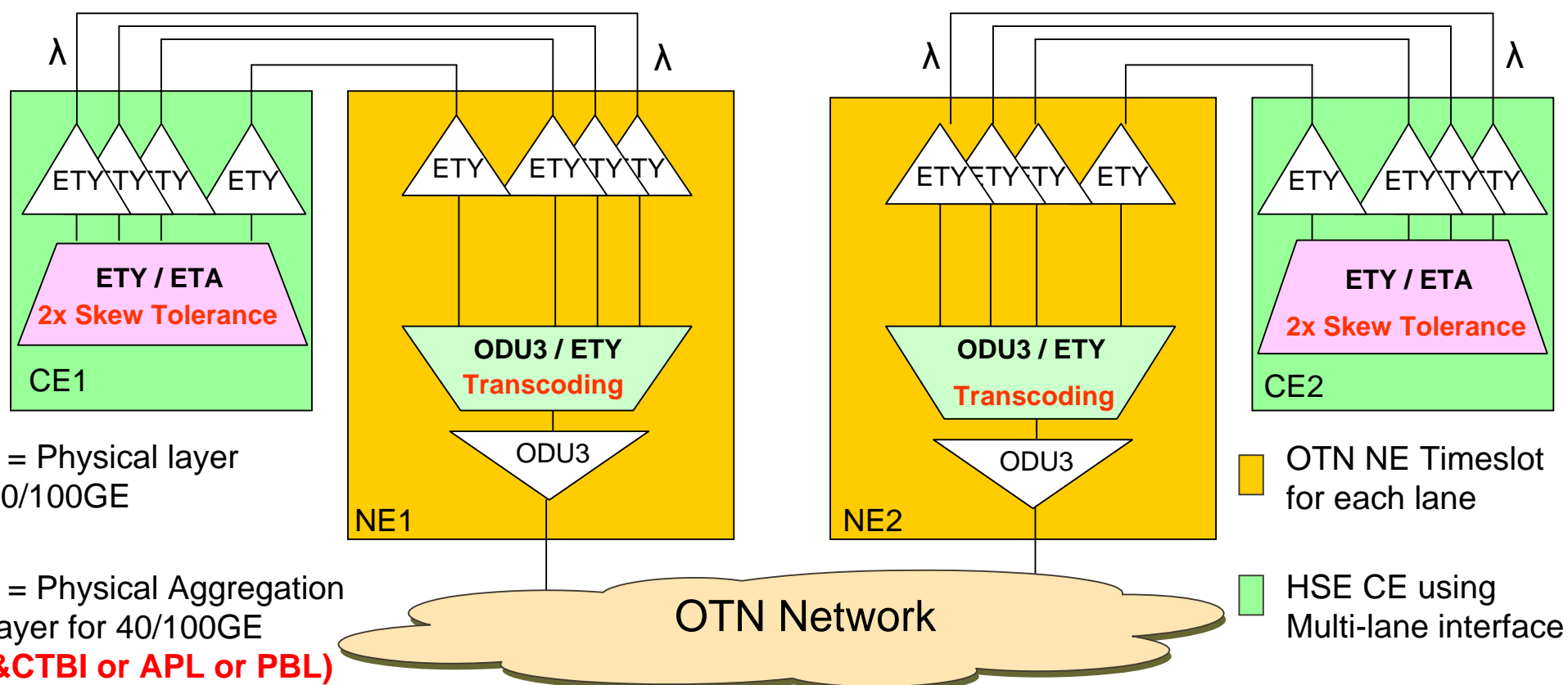
Link-Aggregate Transport of Transcoded 40GE



Link-Aggregate Mapping into ODU3 (Aggregate Transcoded)

Link-Aggregate Model: OTN equipment is aware of PCS codewords and alignment markers; can support a transcoding solution to carry 40GE in a standard ODU3. There are two logical function modules in OTN NE; most likely implemented in two separate devices.

Lane-Independent Transport of Transcoded 40GE



Lane-Independent Mapping into 4 slots slotted ODU3 (Lane Transcoded)

Lane-Independent Model: is essentially client signal bit rate agnostic, can also easily support a transcoding solution to carry 40GE in a slotted standard ODU3. One logical function module is most likely needed. This will enable 4x10GE to be carried in standard ODU3 also.

Summary and Proposal

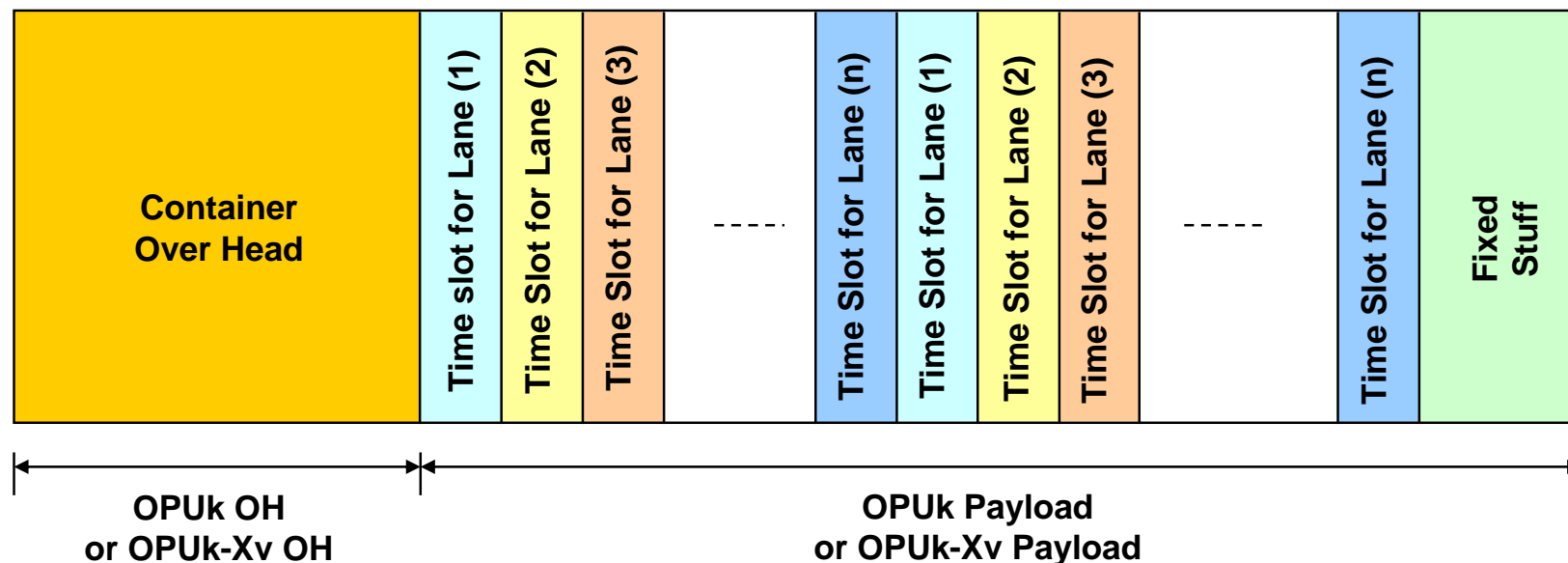
- **OTN Support for both 40GE & 100GE can be accomplished with two models**
 - **Lane Independent**
 - Supports Bit Rate Agnostic Bit Transparency per Lane
 - Supports VL&CTBI, APL, PBL, (Lane Architecture Agnostic)
 - Work in IEEE and ITU-T can be done in parallel
 - Simplifies OTN NE complexity for carrying 40/100GE
 - **Link-Aggregate**
 - Supports standard HSE Link Level PCS codeword transparency
 - Allows use of different PMDs at the ingress and egress of OTN
 - Skew accumulation needs further study
- **Transcoding solution for 40GE in ODU3 could work with both models.**
- **We propose to enable appropriate OTN support by introducing a 2x multi-lane Skew Tolerance with the Lane-Independent Model.**

Thank You

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Mapping Multi-lane in Slotted OTN Container



- In Lane-Independent Model, the OTN container was slotted into Time Slots according to the HSE PMD Lane number. HSE Multi-lane signals are mapped into the container, each lane mapped in a Time Slot Individual.
- The container still an logical entity traverse the OTN network domain without generating any Differential Delay/ Skew between the Time Slots. Every Time Slot have the capability to accommodate the signal clock rate to the OTN container clock rate, with certain space for Positive/Negative justification.
- Slotting OTN container is being discussed and developing in ITU-T.