Test modes and loopbacks

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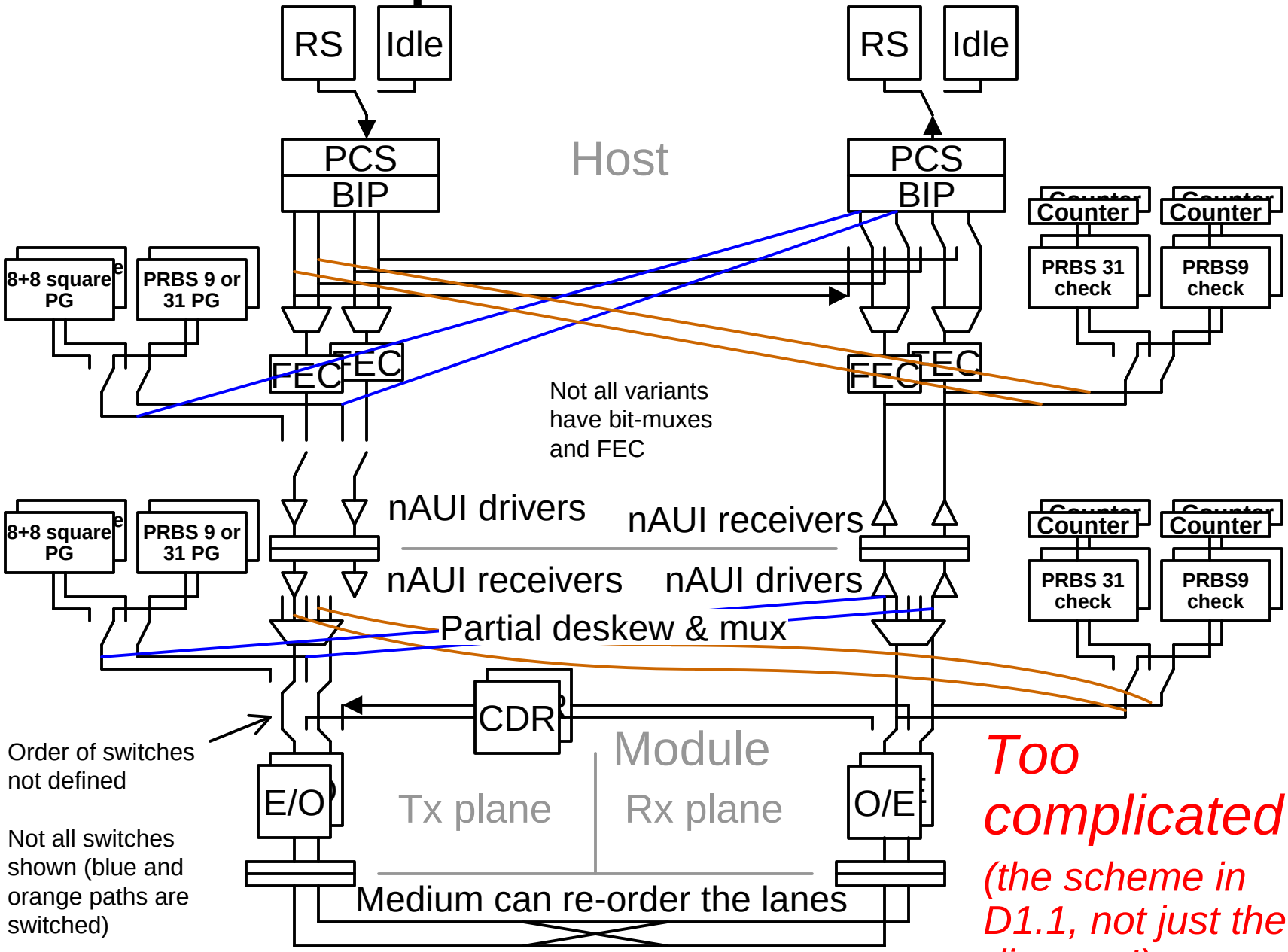
Numerous test modes

- Draft 1.1 Clause 82 has
  - Test pattern -- Idles striped, coded and lane-marked as normal
  - (System) Loopback mode
    - Data from MII returned to MII -- Draft not clear if this should exercise PCS or not
  - Clause 45 Errored blocks counter
  - BIP-8 error counting is proposed at this meeting
- Draft 1.1 Clause 83 has optional test modes
  - PMA system loopback
    - Uppermost PMA connects Tx lane x in to Rx lane x out
  - PMA line loopback
    - Lowest PMA connects Rx in to Tx out
  - Lane by lane test pattern generators and checkers
    - "Where the output lanes of the PMA appear on a physically instantiated interface XLAUI/CAUI or the PMD service interface (whether or not it is physically instantiated)"
    - Controlled for all lanes together, error counters per lane
    - Send Tx PRBS31 -- PRBS31 on each (physical) lane
    - Send Rx PRBS31
    - Check Tx PRBS31, check Rx PRBS31
    - Send Tx TBD, send Rx TBD, check Tx TBD, check Rx TBD
      - Expect TBD will be PRBS9
      - Transmit square wave
      - "only applies to the Tx direction PMA towards a physically instantiated XLAUI/CAUI or towards the PMD service interface whether or not it is physically instantiated"

Options in D1.1



Too complicated

(the scheme in D1.1, not just the diagram!)

Many ways to exercise nAUI transmit side

1. PCS test pattern, through module and loopback cord, 82.2.17 PCS test pattern checker and counter
2. If BIP-8 added
   - PCS test pattern, through module and loopback cord, BIP-8 checker and counter
   - Anything from PCS, through module and loopback cord, BIP-8 checker and counter
3. If FEC, anything from PCS, through module and loopback cord, FEC checker and counter
4. Upper PMA Tx PRBS31 generators, lower PMA Tx PRBS31 check & count
5. Upper PMA Tx PRBS31 generators, through module and loopback cord, upper PMA Rx PRBS31 check & count
   - Works for 40GBASE-SR4, 40GBASE-LR4, 100GBASE-LR10, electrical PMDs
   - Works for other 100G if lanes are not skewed at bit-mux or if checker is smart enough
6. PCS test pattern, through module (or socket), to test equipment
   - General purpose test equipment won't recognise the pattern
   - Future comms analyser or a chip on an evaluation board will
7. If BIP-8 added or FEC present
   - PCS test pattern, or anything from PCS, through module (or socket), to test equipment
     - General purpose ("dumb", "bit-oriented") test equipment won't recognise the pattern
     - Future comms analyser or a chip on an evaluation board will
8. Upper PMA Tx PRBS31 generators, through module (or socket), to test equipment
   - For 40GBASE-SR4, 40GBASE-LR4, 100GBASE-LR10, electrical PMDs, or if lanes are not skewed at bit-mux, general purpose test equipment can recognise PRBS31
   - Smarter checker could recognise pattern even if muxed after skew

- *There are more alternatives than we need*
- We need something for Ethernet-aware test equipment, something for general purpose test equipment, something for self test, and for with and without medium or PMD plugged in

Difficulties with D1.1 scheme 1/2

- Too complicated
- The "options" aren't really options
  - Customers demand all options!
- Even with all these options, not everything is convenient
- e.g. cannot check PMA mux and demux (or FEC) operation without a PMD present because PMA system loopback is high up
  - Not the usual way 802.3 loopbacks are done. Examples
    - 51.8 NOTE-Loopback mode may be implemented either in the parallel or the serial circuitry of a device
    - 50.3.9 NOTE-The signal path through the WIS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that this signal path encompass as much of the WIS circuitry as is practical.
    - 48.3.3 NOTE-The signal path that is exercised in the Loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this Loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.
- Cannot use system loopback to verify electrical connections of retimed module PMA system loopback is high up above module connector
- For 100G, any loopback in the module is unfeasible because transmit and receive sides are likely to be physically separated with no satisfactory way of making a high speed connection between them

Difficulties with D1.1 scheme 2/2

- Line loopback
  - If done low down, require transmitting off a received clock(s) which is not otherwise done and would have questionable signal integrity without extra expense
  - Line loopback, if present, should be in the host not the module, where there is a digitally-oriented ASIC, able to use de-Dynamic-Skew buffers as jitter filters
- If generating PRBS lane by lane e.g. in the upper PMA, need to enforce an offset between patterns to avoid an abnormal pattern when serialised
  - Draft may say that it's not for serialising, but people will use it that way
  - With single PRBS, bit-striped across the lanes, as long as not skewed, we get a PRBS when muxed (and naturally when demuxed again)
    - and after a 10:4 mux?
- Host can do things autonomously without a module, but module is helpless unless plugged into something
  - Therefore, host or eval board or test equipment can do pattern generation and checking (or line loopback, especially if no bit-mux present). Module options are unnecessary
- Test generators and checkers are a burden particularly on small low-power modules
    - Not needed for any module without a bit-mux. Questionable for modules with bit-mux
- See another presentation for recommendation for square wave

Test priorities

- The primary use for test modes is to confirm that everything's working
- Then, to confirm that particular interfaces or sublayers or physical entities (PCB or module) are working
- Also to support BER-based specs such as TDP and stressed sensitivity
- Users don't need to know which lane is bad (if any lane is) because they can't replace just one lane
  - Nice to have but less important than controlling cost, power consumption and complexity and providing good test coverage

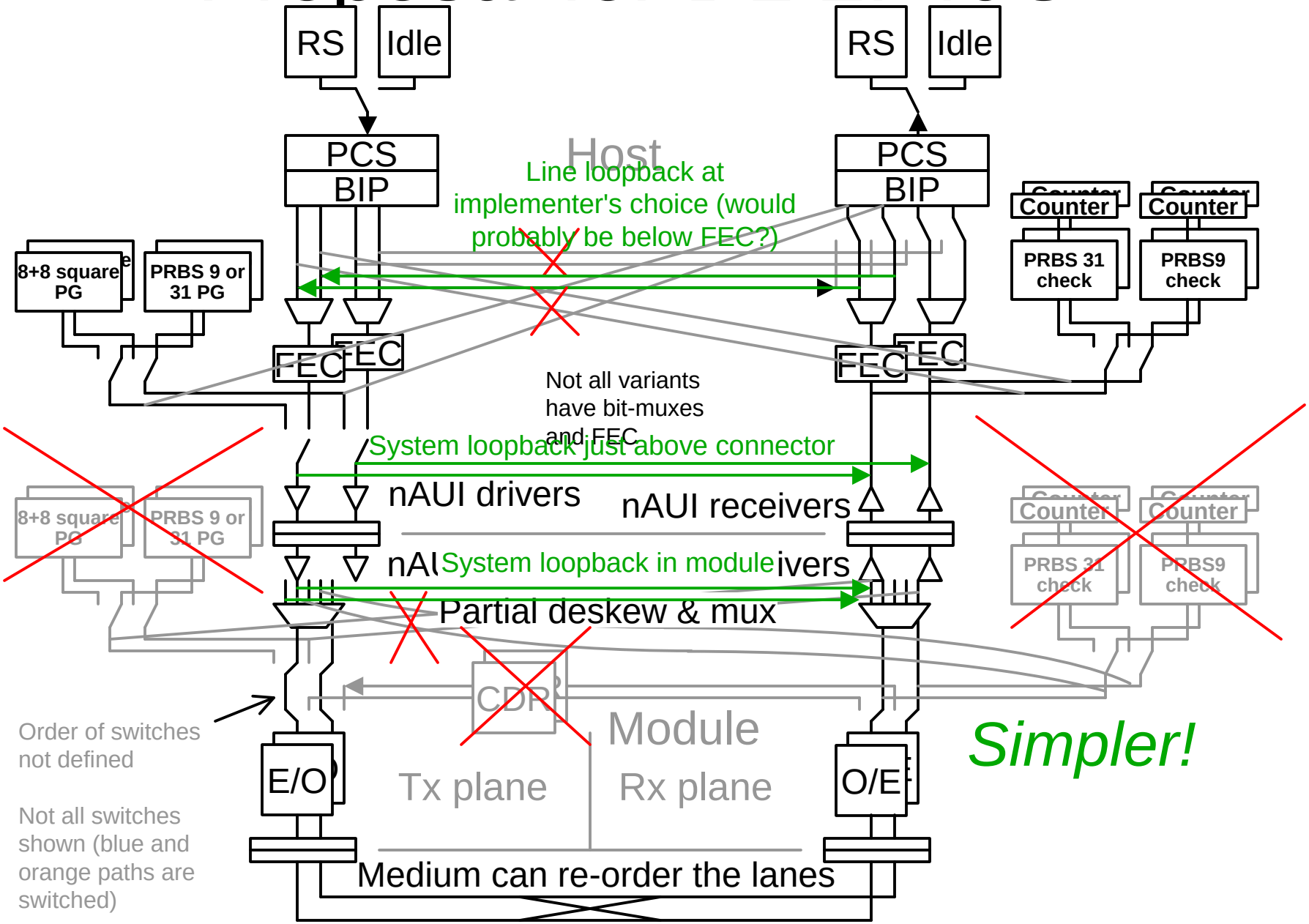
Fault isolation to a physical lane

- If we have lane-by-lane PRBS31 and PRBS9, then we can
  - Set all but one transmit lane to PRBS9, last lane to PRBS31
  - Set all but one receive lane to PRBS9, last lane to PRBS31
  - Change which lane is special at both places until fault is located
- Works even if the lanes have been swapped
  - Partly works even if (100G) some lanes have been sliced in two
- PRBS31 generator and checker and PRBS9 generator and checker can be much the same circuitry (switch the taps in a delay line)
- But is this more than we need?

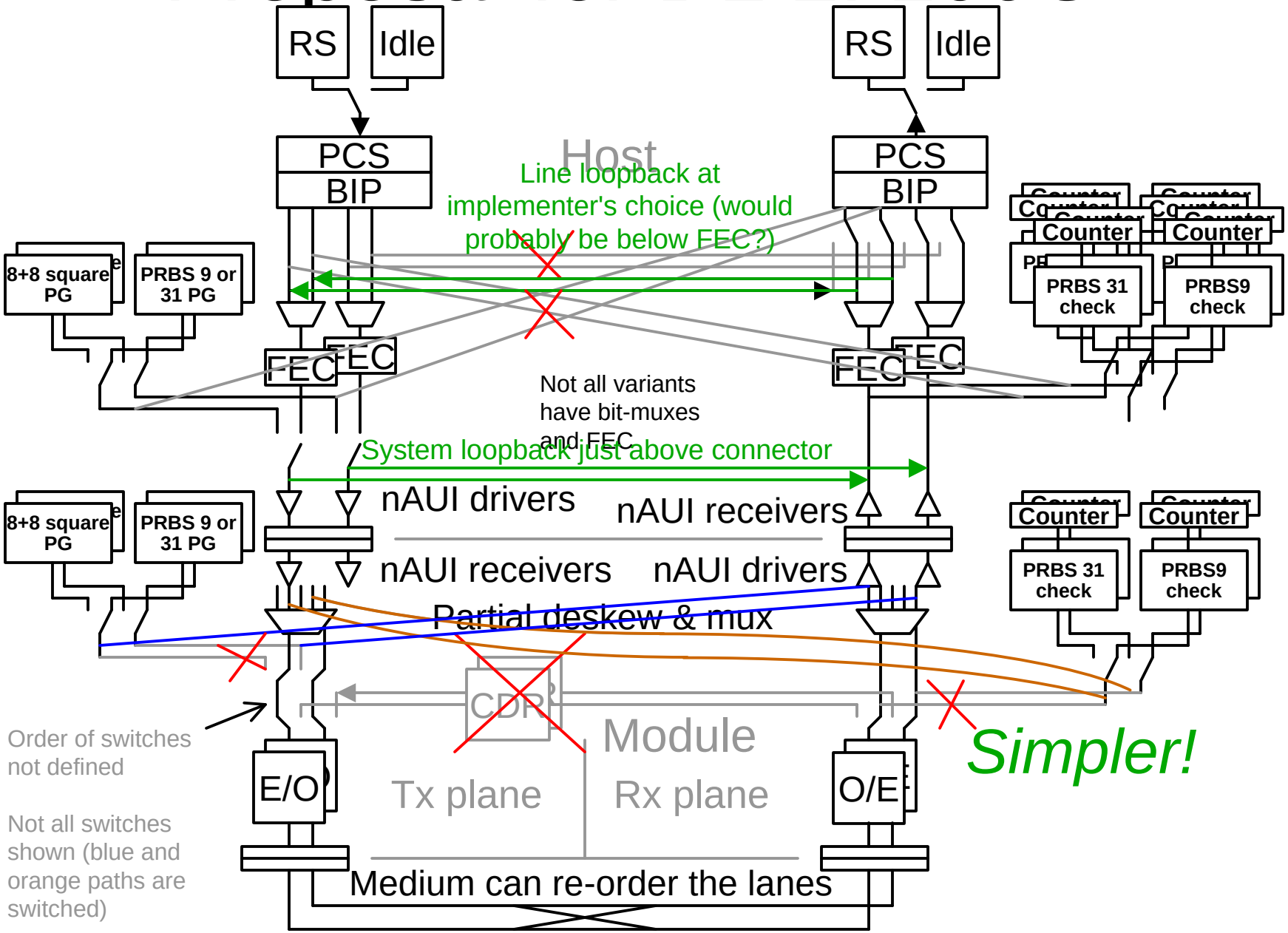
Position of PMA loopbacks

- The draft puts system loopback at the top of a PMA and line loopback low down in the stack to avoid lane swapping
  - But the medium can swap the lanes anyway
  - 100G is even more "interesting" as one of the 10 lanes could get divided among two lanes
    - PCS can cope with this
- We should just accept that lane swapping may happen
  - Put the internal system loopback just above the connector
    - If PMD is present, can always connect its output to its input for an all-sublayers system loopback
  - Put the line loopback in the upper PMA (above the connector)
    - There's a comment that recommends deleing it altogether

Proposal for D1.2: 40G



Proposal for D1.2: 100G



Recommendations

1. No line loopback in module without bit-mux
2. No system loopback in module without bit-mux
3. No pattern generators in module without bit-mux
4. No pattern checkers in module without bit-mux
5. System loopback at lowest PMA above module connector
6. Line loopback at a level in PMA of implementer's choice
   - so e.g. Dynamic Skew buffers can be used as jitter filters
7. If BIP-8 adopted, use it for PCS pattern checking – no additional checker
8. Consider deleting 40G transmit side pattern checkers
   - Relying on system loopback or test equipment or 2nd DTE
9. Consider deleting 40G receive side pattern generators
   - Relying on system loopback or test equipment or 2nd DTE

- Because the PCS lanes are physical lanes at the top of the PMA stack and if muxed in future 2-lane or serial PMDs, it's a simple binary tree
  10. No line loopback in 40G module
  11. No system loopback in 40G module
  12. No pattern generators in 40G module
  13. No pattern checkers in 40G module
- Because there is always an alternative method, and for module physical reasons
  14. No line loopback in module
  15. No system loopback in 100G module
  16. No Tx side pattern generators in module
  17. No Rx side pattern checkers in module

18. Either: use PRBS9 and PRBS31 to create one "special lane"
19. Or, no need for "special lane" provision and consider delete PRBS9 checker
    - Thought to be cheap but without a specific purpose
20. Make square wave mandatory for KR4 and CRn if they need it
21. Make no provision for square wave for optical PMDs or nAUI