FEC multilane bit serial interface for 40GBASE-R and 100GBASE-R

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Jan 13, 2009

Overview

- Proposed modifications to Clause 74 FEC for multilane bit serial operation with 40GBASE-R and 100GBASE-R PHYs
  - This presentation addresses comment #351 on P802.3ba-D1.1

Background

- Clause 74 FEC functional interfaces were originally defined for use with 10GBASE-R PHYs
  - The 10GBASE-R FEC service interface uses 16-bit XSBI interface as specified in 74.5
  - The FEC function operates on 64B/66B data code blocks
  - Hence a reverse gearbox function defined in 74.7.4.1 provides functionality to adapt between the 66-bit width of the 64B/66B blocks and the 16-bit width of the FEC service interface

Proposed changes

- The reverse gearbox functionality has to be modified to adapt the 66-bit width of 64B/66B blocks to the multilane bit serial 40/100GBASE-R FEC service interface or its physical instantiation of XLAUI/CAUI
- Changes needed for the following functions
  - 74.7.4.1 Reverse gearbox function
  - 74.7.4.3 transmission bit ordering Fig 74-3
  - 74.7.4.4 FEC encoding, Fig 74-4
  - 74.7.4.5.1 FEC decoding, Fig 74-6
  - 74.7.4.6 FEC receive bit ordering, Fig 74-7
  - 74.6 Delay constraints, adjust the value for 40G & 100G bit time

74.7.4.1 Reverse gearbox function

Proposed changes to 74.7.4.1
Change title of

- *Change title of 74.7.4.1 to:*

  74.7.4.1 Reverse gearbox function for 10GBASE-R
- *Insert a new subclause below 74.7.4.1*

  74.7.4.x Reverse gearbox function for 40GBASE-R and 100GBASE-R

  The reverse gearbox function adapts between the 66-bit width of the 64B/66B blocks and the 1-bit wide lane of the 40GBASE-R or 100GBASE-R PCS to FEC interface. It receives the 1-bit stream from the FEC service interface and converts them back to 66-bit encoded blocks for the FEC Encoder to process. The reverse gearbox function operates in the same manner as the lane block sync function defined in 82.2.11.

  The reverse gearbox function receives data via 40GBASE-R and 100GBASE-R FEC_UNITDATA.request*x* primitive (see 74.5.2). It obtains lock to the 66-bit blocks in each bit stream using the sync headers and outputs 66-bit blocks to the FEC encoder function (see 74.7.4.4). PCS lane lock is obtained as specified in the PCS lane lock state diagram shown in Figure 82–10.

  The reverse gearbox functionality is necessary only when the physical instantiation of FEC service interface XLAUI/CAUI is implemented between the PCS and FEC functions, since that interface passes data via bit serial 4 or 10 lanes. When the XLAUI/CAUI is not implemented, the internal data-path width between the PCS and FEC is an implementation choice. Depending on the path width, the reverse gearbox function may not be necessary.

74.7.4.3 FEC tx bit ordering, Fig 74-3

- *Replace Fig 74-3 as shown:*

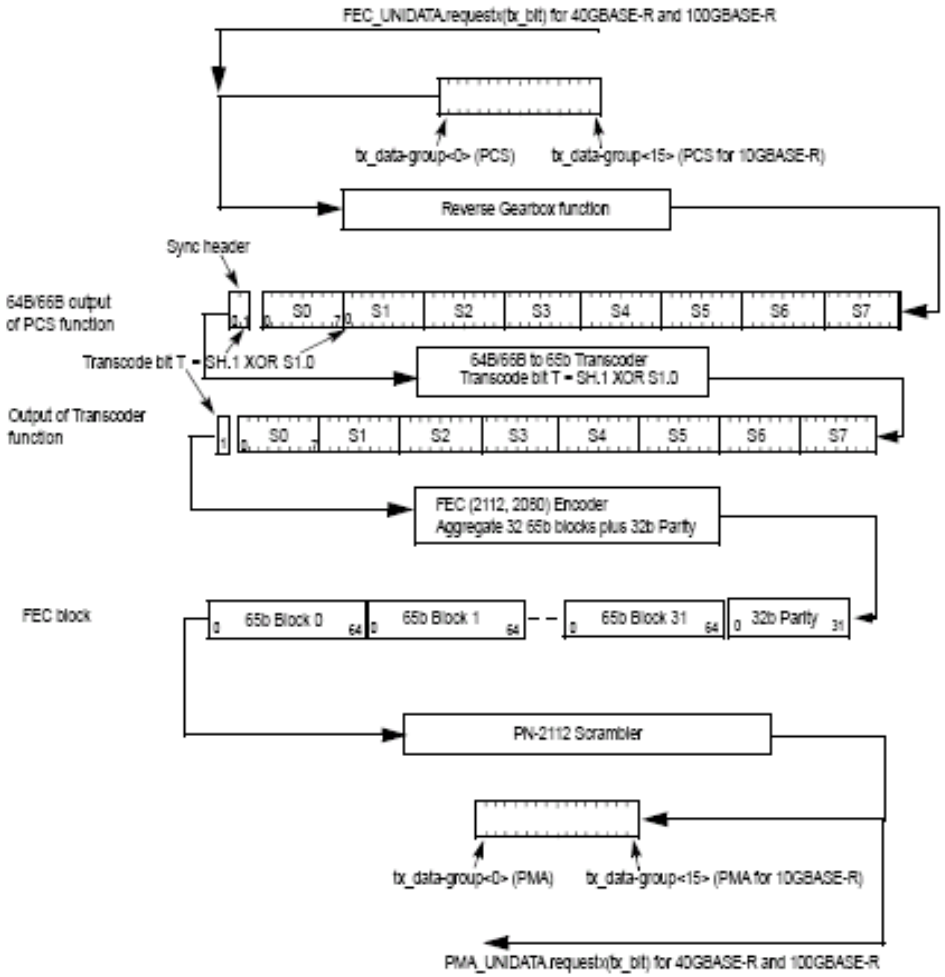

Figure 74–3—FEC Transmit bit ordering

74.7.4.4 FEC encoder, Fig 74-4

- *Replace Fig 74-4 as shown below:*

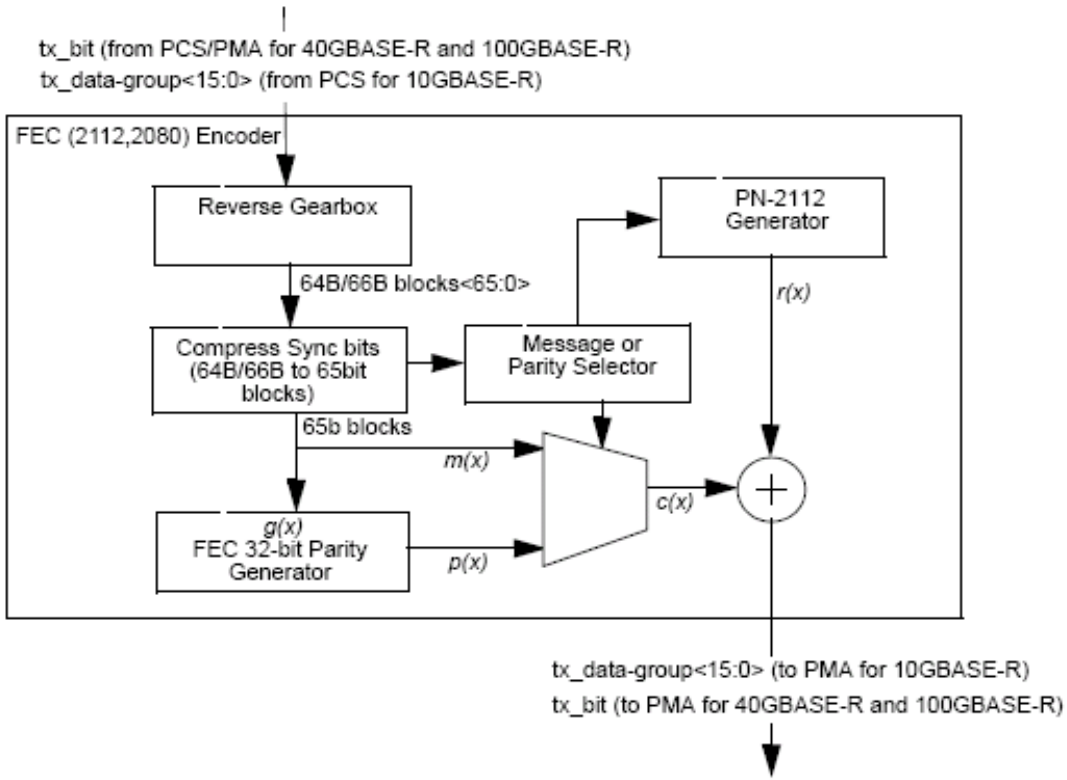

Figure 74–4—FEC (2112,2080) encoding

74.7.4.5.1 FEC decoding, Fig 74-6

- *Replace Fig 74-6 as shown below:*

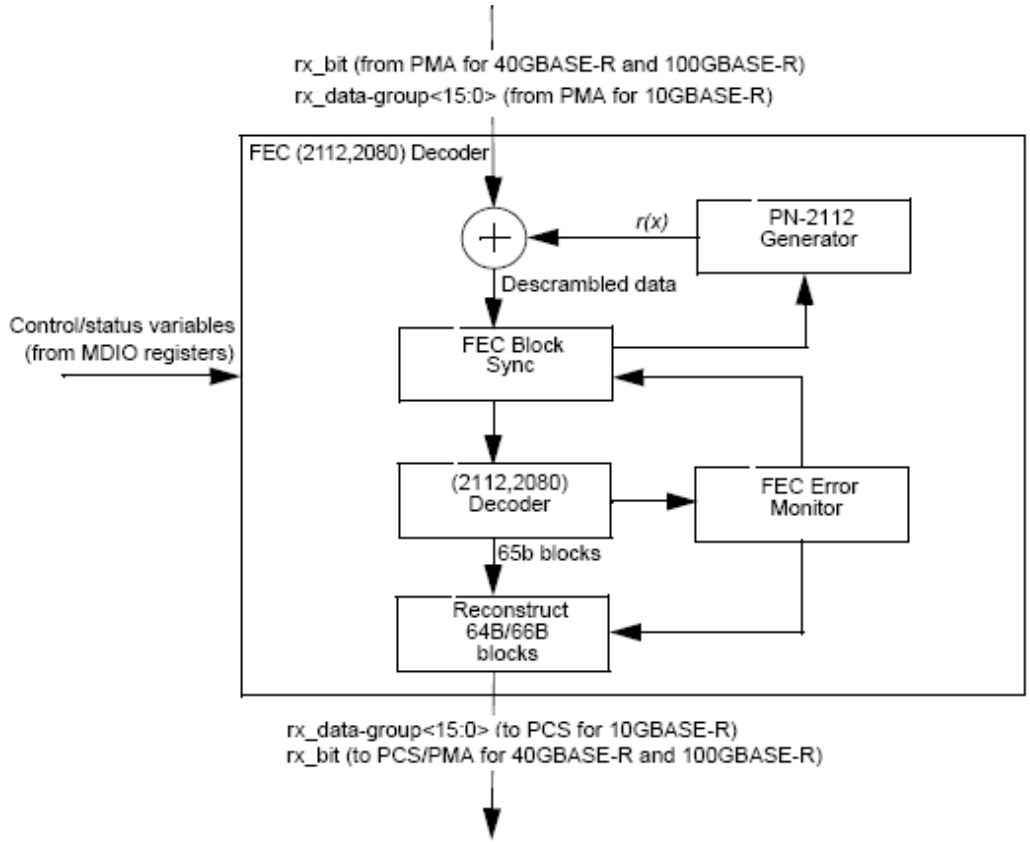

Figure 74–6—FEC (2112,2080) decoding

74.7.4.6 FEC rx bit ordering, Fig 74-7

- *Replace Fig 74-7 as shown:*

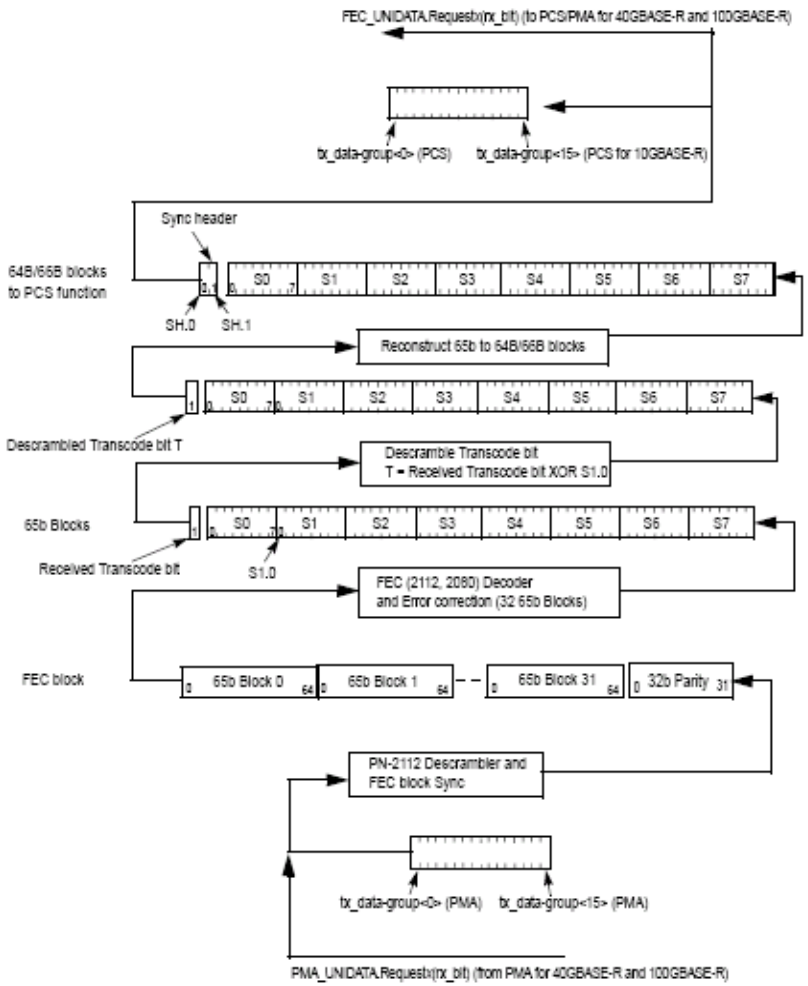

Figure 74–7—FEC Receive bit ordering

Delay constraints

Proposed changes to 74.6

- *Add following lines to the end of 74.6*

  The sum of transmit and receive delay contributed by the 40GBASE-R FEC shall be no more than 24576 BT. The sum of transmit and receive delay contributed by the 100GBASE-R FEC shall be no more than 61440 BT.

Other Misc. changes

- *Change last sentence of 74.7*

  ..and sends the data to the BASE-R PCS.

- *Change first sentence of 74.7.3*

  The BASE-R 64B/66B PCS maps 64 bits of scrambled payload..

- *Change other instances of 10GBASE-R to BASE-R or 40GBASE-R and 100GBASE-R as appropriate throughout Clause 74*

Thanks!