

Channel and Link Specifications
for IEEE P802.3ba electrical links

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January 2009 Interim



Outline

- 1 Channel
- 2 Simulation Results
- 3 Specifications Tables
- 4 Conclusion

Channel consists of 3 parts

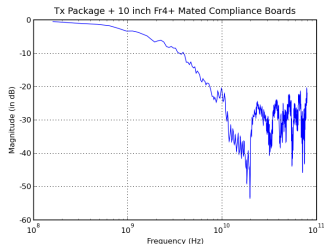
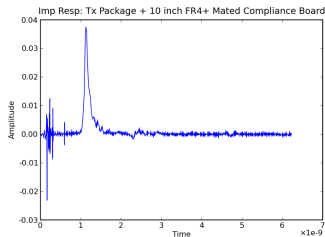
There are three channels competing for the budget.

- Channel 1: Host Tx (TP0) to PMD (TP1a) (Host Tx + Fr4 +connector + module Rx)
- Channel 2: Module Tx (T41) + Channel +Module Rx (TP4)
- Channel 3: PMD (TP4) to Host Rx (TP5) (Module Tx + connector + Fr4 + Host Rx)

There are two (somewhat independent) electrical point to point links. Channels 1 and 3 are the electrical channels that (can) differ in the equalizing power of the Tx and Rx.



Electrical Channel Target



The Channel has:

Host Package about 1dB loss at Nyquist in package,

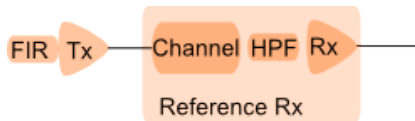
Host Board 12 inches FR4– 10" on board +2" in HCB,

Connector HCB + MCB

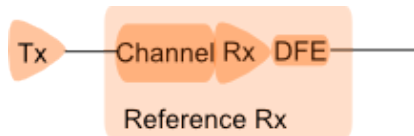
... around 15dB loss end to end at Nyquist.



Host to Module vs Module to Host

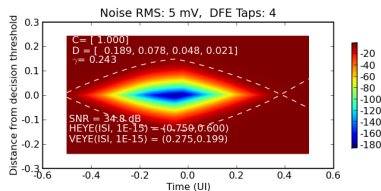
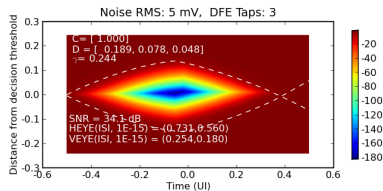
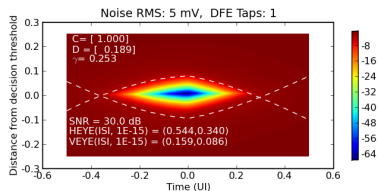


Host Tx: 3-Tap FIR&Low Rj
Module Rx: simple linear boost



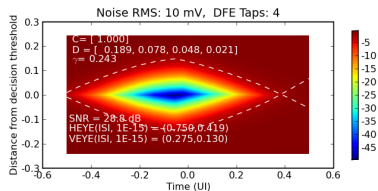
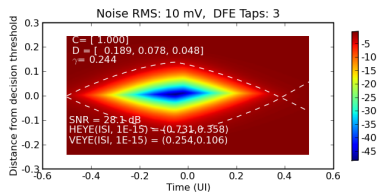
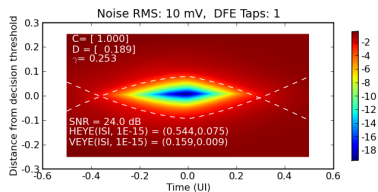
Module Tx: with no FIR
Host Rx: with 3T DFE

Statistical EYES over DFE taps @5mV noise



- A normalized 1V launch has 86 to 200mV vertical Eye, and
- 340 to 580 mUI horizontal Eye with 5mV rms noise.

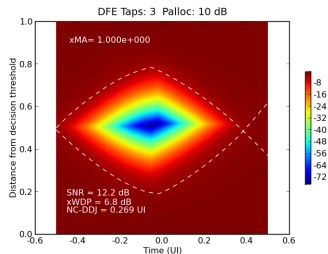
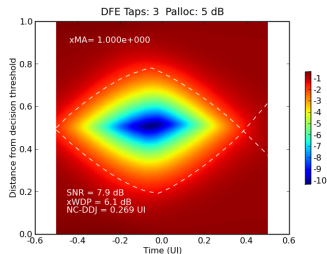
Statistical EYES over DFE taps @10mV noise



- A normalized 1V launch has 9 to 130mV vertical Eye, and
- 75 to 419 mUI horizontal Eye for 10mV rms Noise.



WDP EYES for different Palloc



- A normalized 1V launch has 6.1 to 6.8dB WDP penalty, and
- 269 mUI non-compensable deterministic jitter.

Host to Module Specifications

Tx Parameters			
Test		Units	Value
Vpp	Max	mV	
VMA	Max	mV	
	Min	mV	
UJ	mUI		
Palloc	dBe		
TWDP	dBe		
NC-DDJ	mUI		

Rx Parameters		
Test	Units	Value
VMA	mV	
BUJ	mUI	
RJ	mUI	
RI	dBe	
WDP	dBe	
NC-DDJ	mUI	

- Tx options: 3 Tap FIR
- Rx options: Single Zero Boost



Module to Host Specifications

Tx Parameters			
Test		Units	Value
Vpp	Max	mV	
VMA	Max	mV	
	Min	mV	
UJ	mUI		
Palloc	dBe		
TWDP	dBe		
NC-DDJ	mUI		

Rx Parameters		
Test	Units	Value
VMA	mV	
BUJ	mUI	
RJ	mUI	
RI	dBe	
WDP	dBe	
NC-DDJ	mUI	

- Tx options: Sufficient VMA, low Jitter RJ
- Rx options: 3-tap DFE



Conclusion

Board 12 inches FR4 +connectors feasible

Host to Module Needs Tx FIR +sufficient module EQ

Module to Host Needs sufficient on Module VMA and Host EQ



Thank You

