Clause 74 FEC and MLD Interactions

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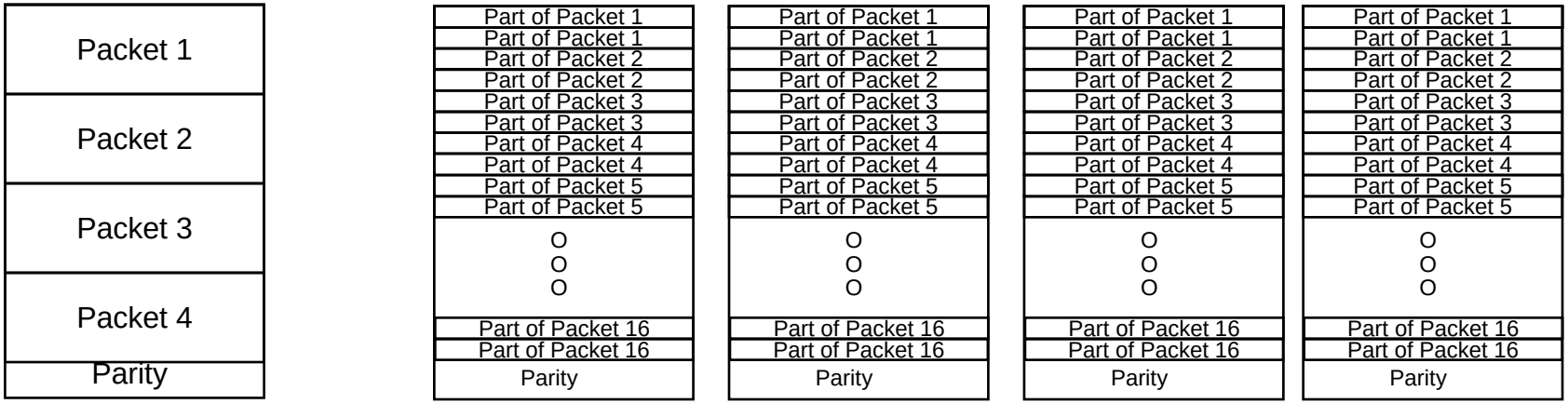
Introduction

- **The following slides investigate whether the objectives of the Clause 74 FEC* can be met with MLD for KR4, and CR4/CR10**
  - **Improve BER from 1e-12 to beyond 1e-15**
  - **Increase MTTFPA for borderline channels with burst errors**
- **This includes**
  - **Interactions between the FEC and how MLD stripes and multiplexes data**
  - **Reduction of the FEC gain and increase in latency**
  - **Error properties of copper cable channels**

***** **www.ieee802.org/802_tutorials/july06/10GBASE-KR_FEC_Tutorial_1407.pdf**

Concern #1

- **With MLD, packets are spread to multiple lanes, 66b blocks at a time.**
- **Packets are spread out into multiple FEC blocks across multiple lanes**
- **If there is an unrecoverable error in a FEC block, all packets are dropped from that FEC block**
- **For 40GE, and 64B packets, 16x64B packets are dropped compared to 4 in 10G**
  - **This decreases the FEC gain**

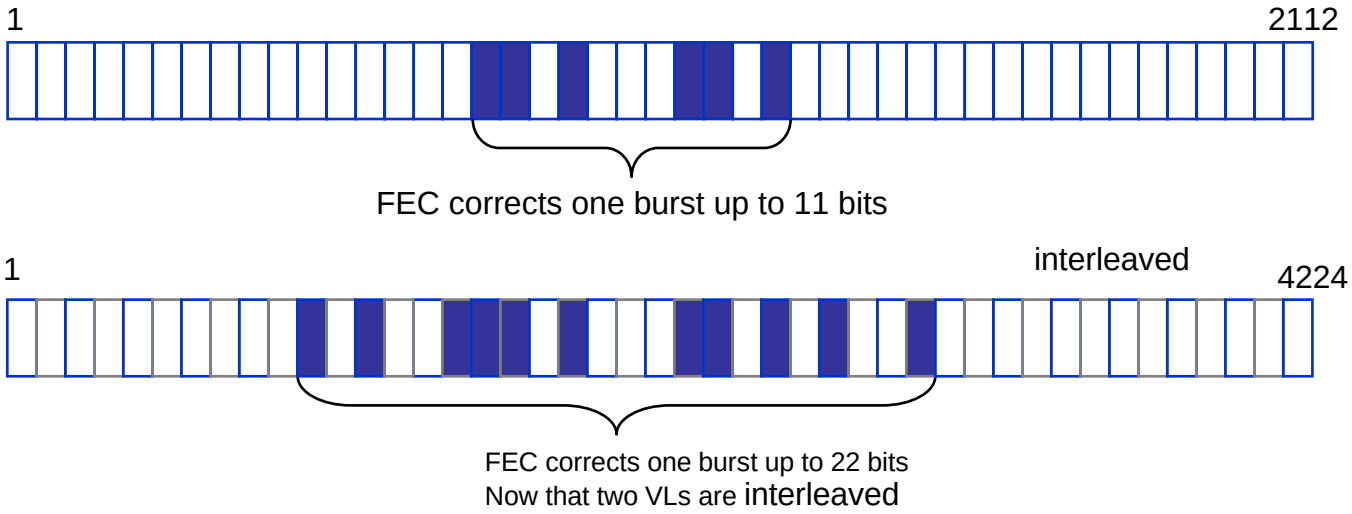


10G KR FEC Block
(Serial)

40G KR FEC Blocks
(4 Lanes)

Concern #2

- **For the 100GE copper interface, we interleave two VLs on each physical lane bit by bit. If FEC is needed, then the interleaving extends the effective block size, and with burst propagation it exposes each FEC block to a greater chance of multiple errors**
- **We do gain longer burst error protection, but is that needed?**



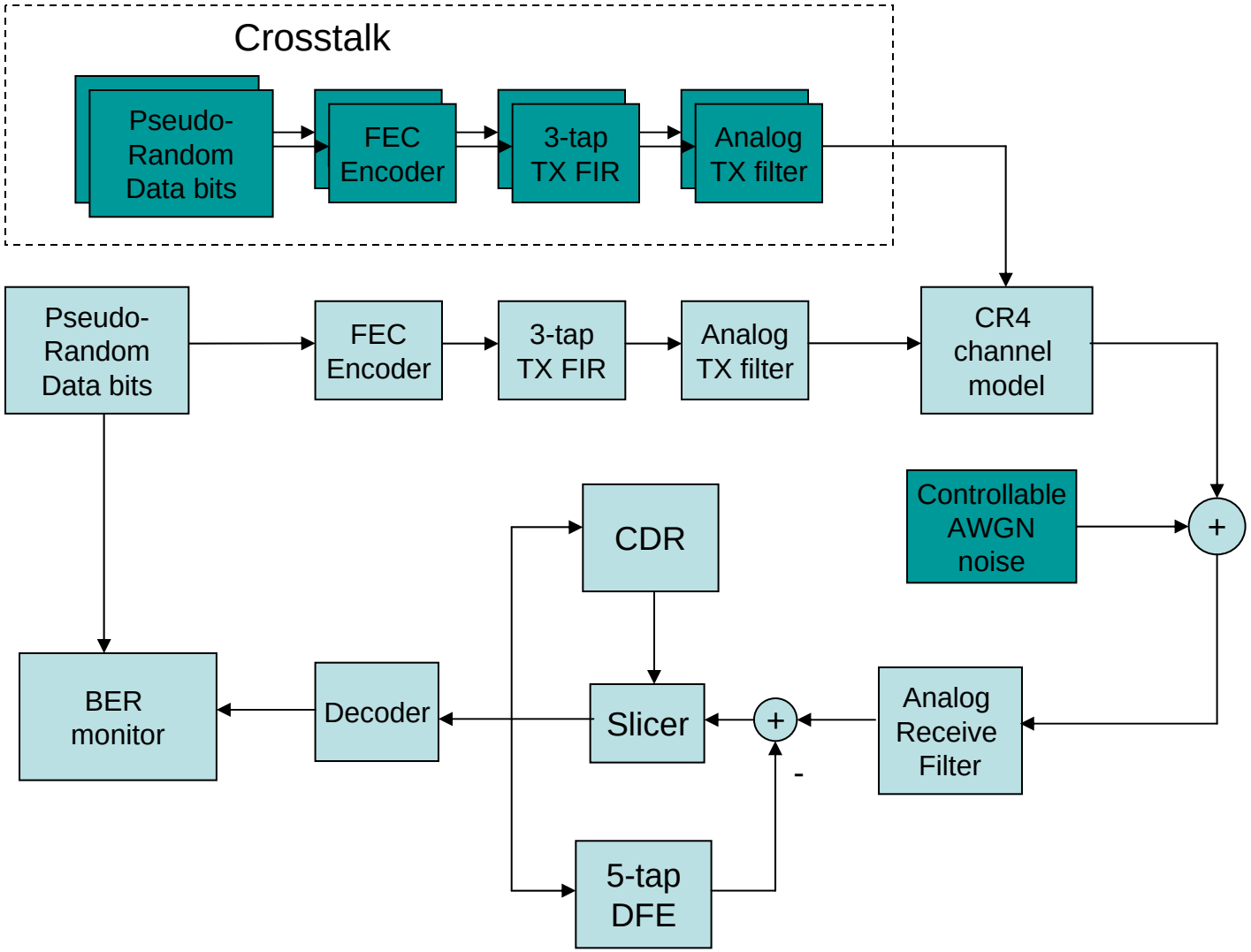
More on Concern #2

- **So we get better burst protection, but for KR we don't really have many bursts > than 11 bits anyhow, so that is not really needed**
- **And with the longer blocks, and if errors are propagated, then there is a bigger chance that two errors occur in the block**
  - **10-25% chance of error propagation in some KR channels**
- **Both concerns evaluated by simulation in following slides for CR4/CR10**

CR4/CR10 Channel Error Propagation

- BER better than 1e-16 can be achieved without FEC
  - http://www.ieee802.org/3/ba/public/jan08/diminico_01_0108.pdf
- FEC can be used for additional margin or tolerance
- Time Domain Simulation Setup to investigate error propagation
  - Single lane of 10m copper cable assembly – from a CR4 model
  - TX
    - 0.28 UI TJ, KR compliant worst case
    - 3-tap FIR
    - Simple RC model for transmitter
  - Package model included
  - Crosstalk – 7 aggressors with same TX FIR, but higher NEXT amplitude
  - RX
    - Adaptive CDR circuit
    - 5-tap DFE
    - Ideal slicer
  - AWGN noise source controlled to change BER
  - Simulated over 2e10 bits
  - Pseudo random bits, PCS not modeled

Time Domain Simulation Setup



Simulation Results

- At an uncoded BER of 2.7e-7,
  - ~4000 error events occurred
  - Only 1 error event was uncorrectable (BER ~= 3e-10)
- The error propagation statistics are

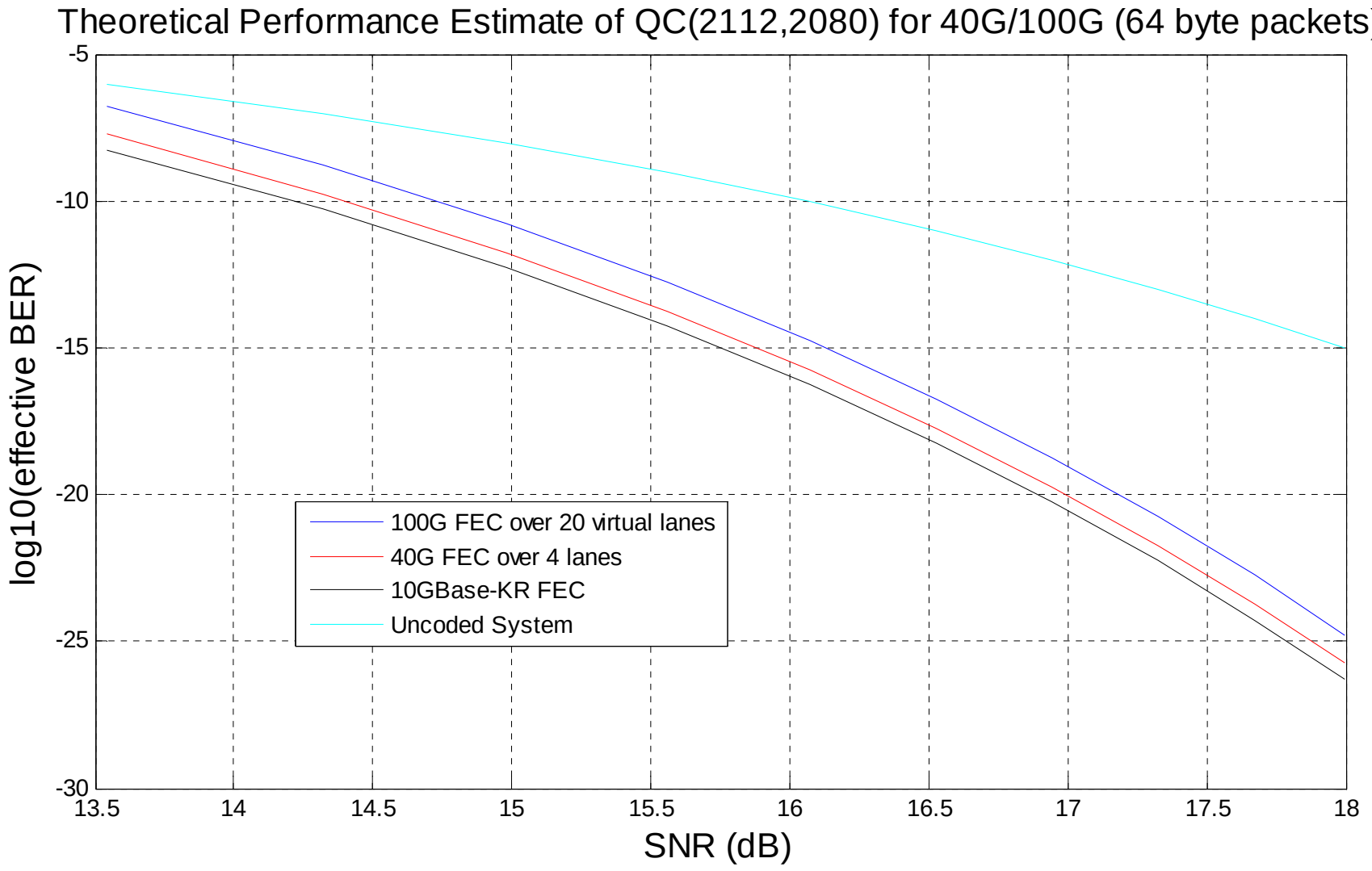
Burst length	Percent	Burst length	Percent
1	84.8	7	0.05
2	4.0	8	0.05
3	7.4	9	0.025
4	2.7	10	0.025
5	0.64	11	0
6	0.28	>11	0

- Clause 74 FEC can correct up to 11-bit error bursts
- Only 15 % of the errors propagated beyond 1 bit

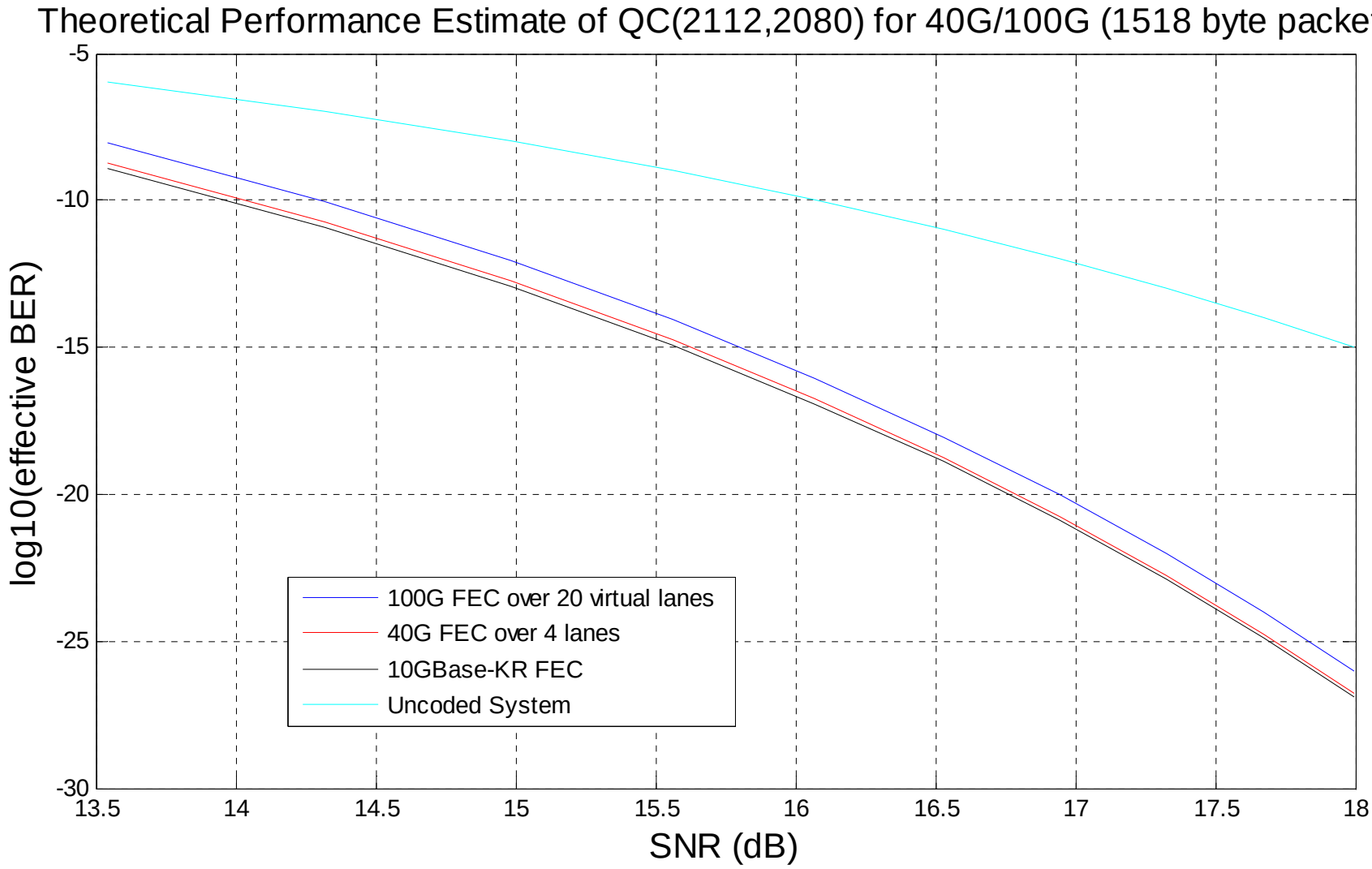
Theoretical Performance Estimate

- Assumptions:
  - Assume memory-less Binary Symmetric Channel (BSC), but with finite error propagation (to model DFE effects)
  - Probability of first error in a burst based on Gaussian noise model
  - 25% of errors are propagated beyond 1 bit
  - DFE does not propagate errors beyond decoder's capability
    - Optimistic for channels with significant error propagation or other error mechanisms
  - Uncorrected errors caused by 2 error events in the same FEC block
  - Uncorrected errors are detected and entire code block is rejected
  - Rejected block causes multiple packets to be lost due to block interleave at PCS and striping
- Method:
  - Estimate Ethernet Packet Error Rate for each SNR using probabilities
  - Translate Packet Error Rate to "Effective BER" of ideal memory-less BSC with Gaussian noise with no error propagation

Results with 64 byte packets



Results with 1518 byte packets



Coding Gain Results

Cases	64 byte Packets		1518 byte Packets	
	(dB)	BER for 1e-12 input	(dB)	BER for 1e-12 input
100G over 20 VLs	1.65	1.2e-19	2.02	6.6e-21
40G over 4 VLs	1.89	1.3e-20	2.21	1.3e-21
10GBase-KR	2.05	4e-21	2.26	9e-22

Analysis

- Reduced coding gain due to multiple packet loss when an FEC block error occurs with
  - smaller packets
  - more virtual lanes
- Coding gain reduces marginally with bit interleaving at the striping layer because of double error events
- For small packets, relative to 10GBase-KR
  - For 40G with 4 virtual lanes ~ 3.3x worse BER improvement
  - For 100G over 20 virtual lanes ~ 23x worse BER improvement
  - Can still improve BER by > 4 orders of magnitude
    - 1e-12 to 1e-19, provided error burst length is limited
  - Similar MTTFPA improvements can be achieved
    - **www.ieee802.org/802_tutorials/july06/10GBASE-KR_FEC_Tutorial_1407.pdf**

What about latency

- **At what value does latency become a concern?**
- **Just looking at the FEC block time (and not processing time):**
  - **10GE backplane, 2112 bits = 205nsec**
  - **40GE backplane (4 VLs, 4 lanes), 2112 bits = 205nsec**
  - **100GE copper (20 VLs, 10 lanes), 2112 x 2 = 410nsec**
- **Today's .ap spec is: 6144 UI of delay (tx and rx)**
- **So for 40GE we do not reduce the possible latency, even though we are going at 4x the speed**
- **For 100GE, if we use FEC, we double the intrinsic latency when compared to 10GE, but the processing time can be the same**
- **Summarizing, total FEC latency constraints can be**
  - **40 GE: 6144*4 bit times = 596ns**
  - **100 GE: (6144 + 2112)* 10 bit times = 801ns**

Conclusions

- Clause 74 FEC's objectives can be met with MLD
  - BER can still be improved by > 4 orders of magnitude
  - MTTFPA can still be improved by > 4 orders of magnitude
- On copper cable assembly channels, Clause 74 FEC can deliver similar performance to KR channels