

# Properties of interleaved PRBS31

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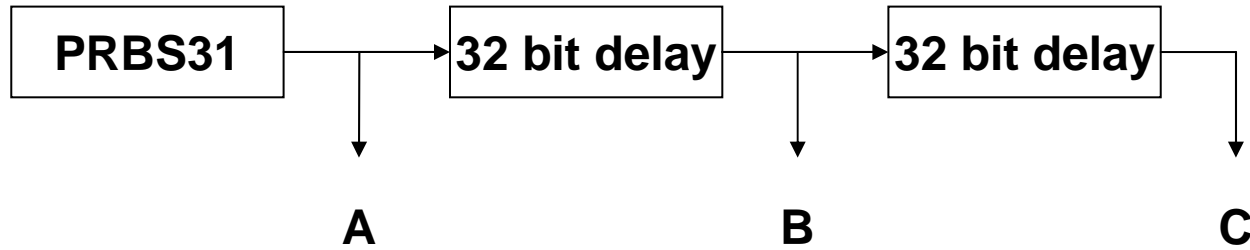
IEEE P802.3ba, San Francisco, July 2009

# Introduction

Comment 33 against D 2.1 proposes to do PRBS31 error checking on a per PCS lane basis so that PRBS31 bit streams which traverse a pair of gearboxes can still be checked.

This contribution analyses the properties of PRBS31 bit streams after they have been bit interleaved by the first gearbox.

# Bit stream

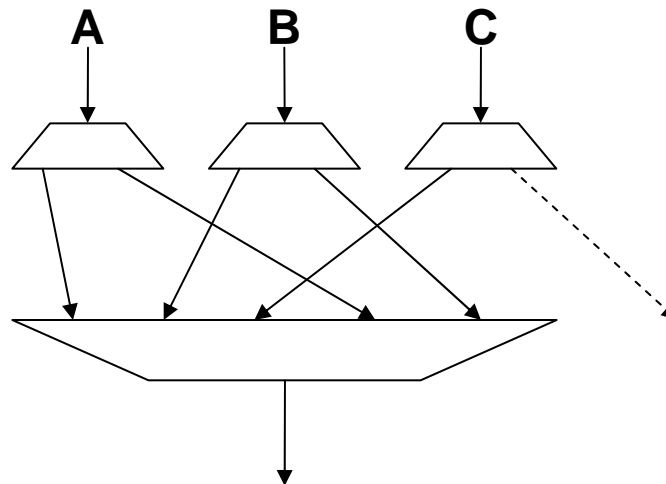


Simulated sequence:

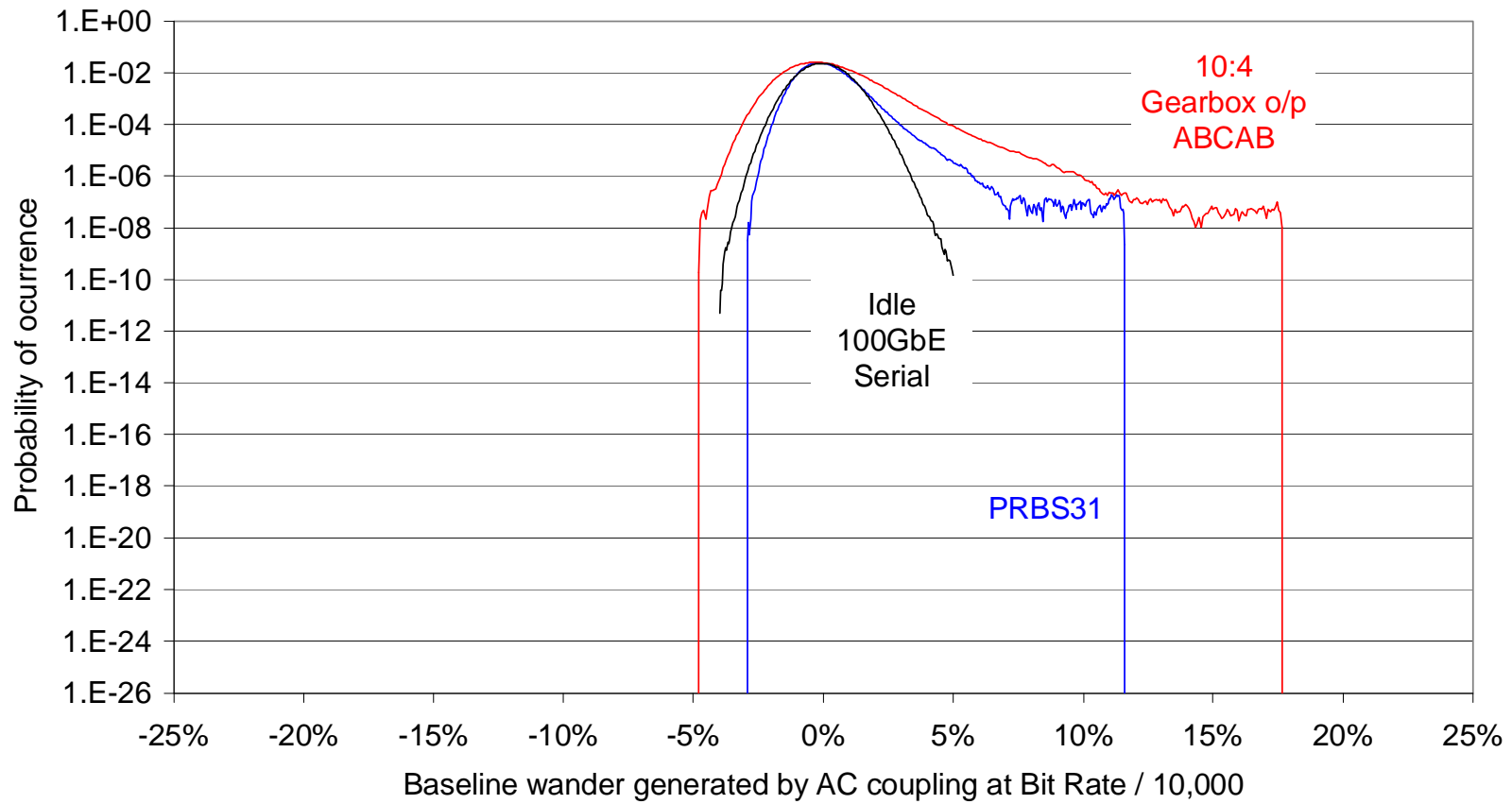
ABCAB ABCAB ...

With every other bit from sequence C dropped

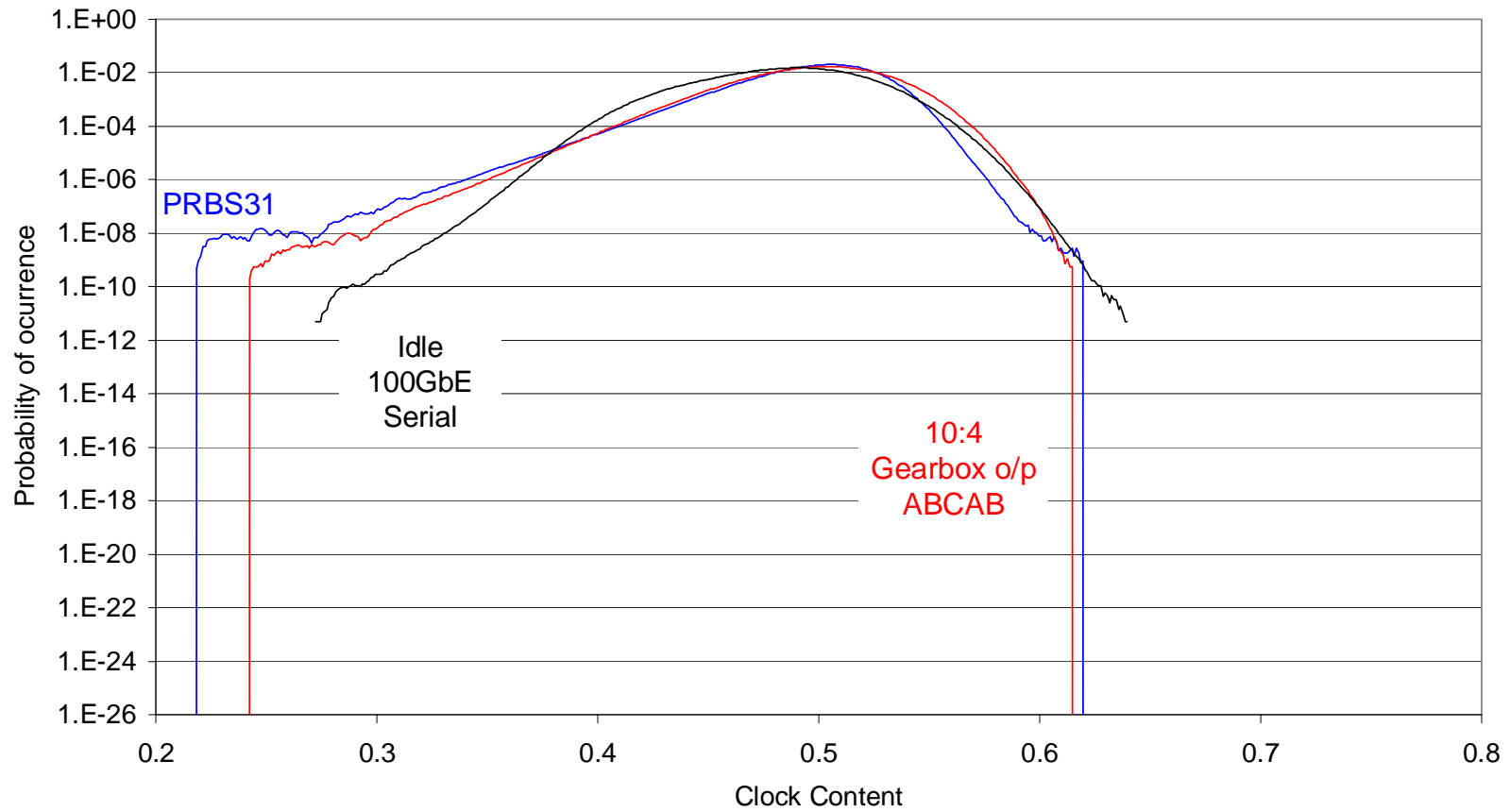
Equivalent to mux structure below



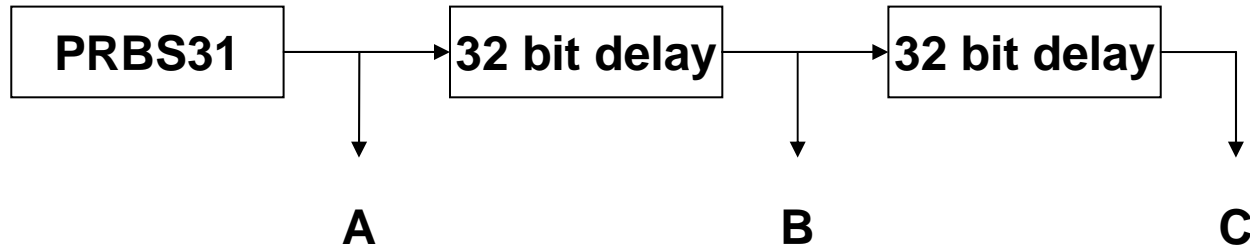
# Baseline wander



# Clock content



# Bit stream 2

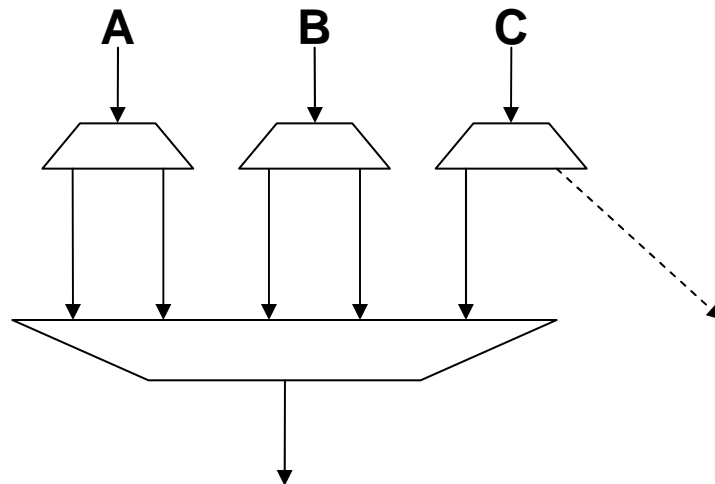


Simulated sequence:

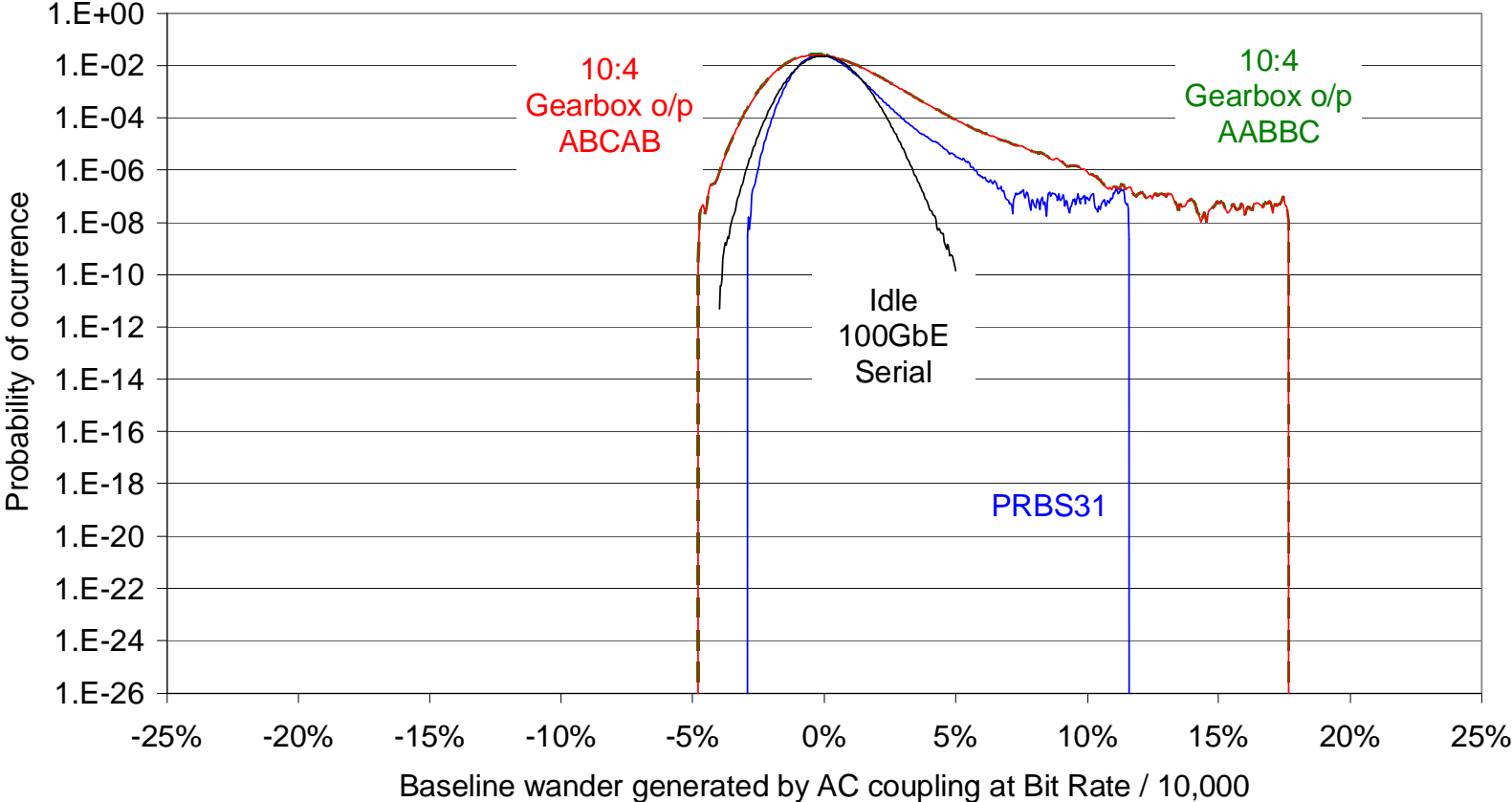
AABBC AABBC ...

With every other bit from sequence C dropped

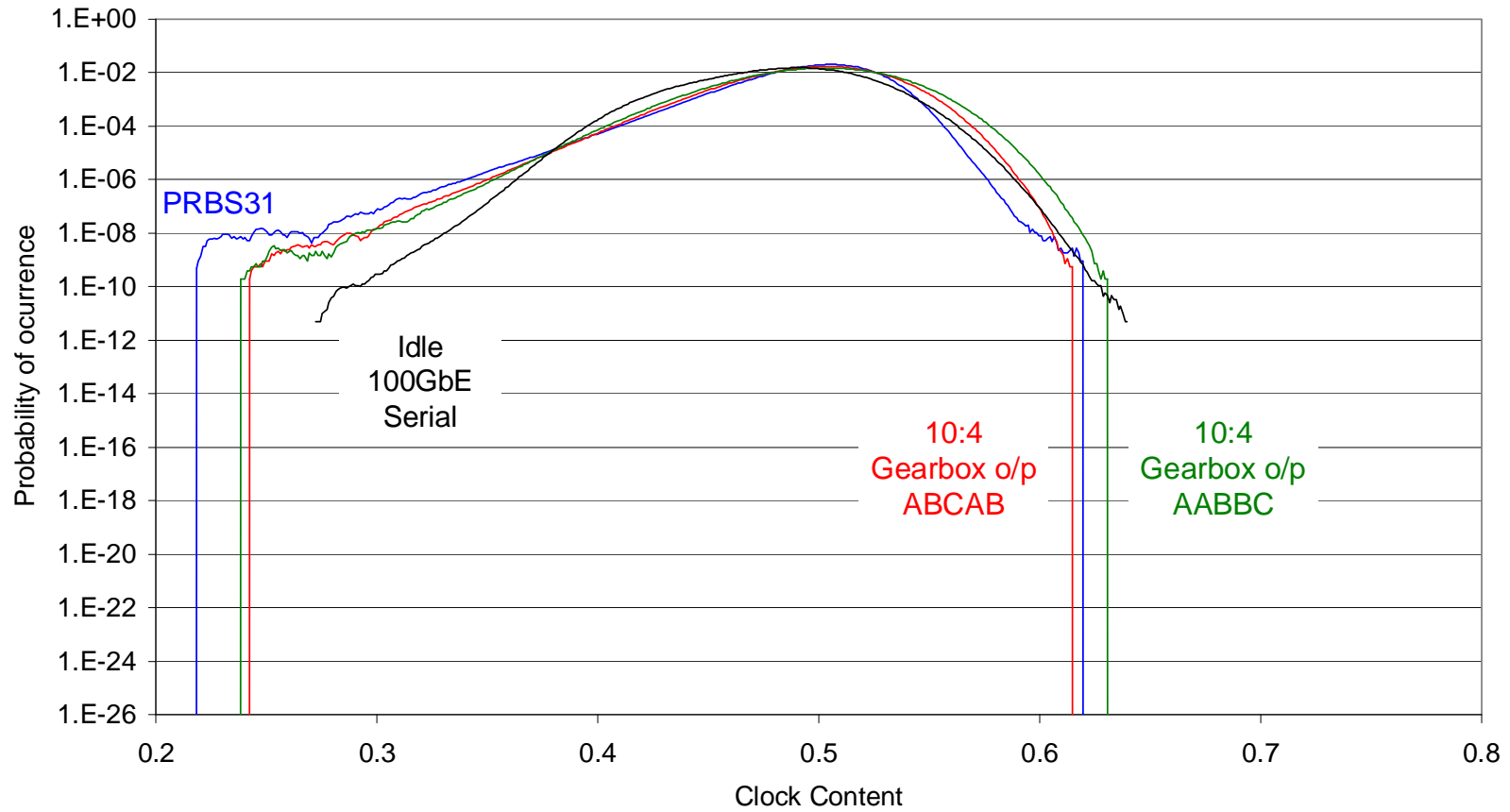
Equivalent to mux structure below



# Baseline wander

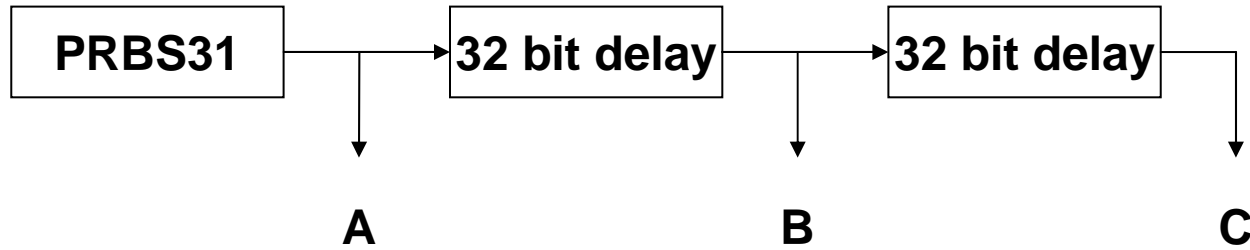


# Clock content





# Bit stream 3

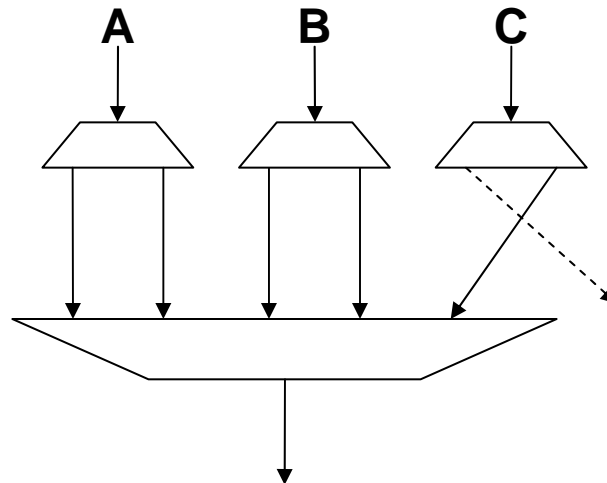


Simulated sequence:

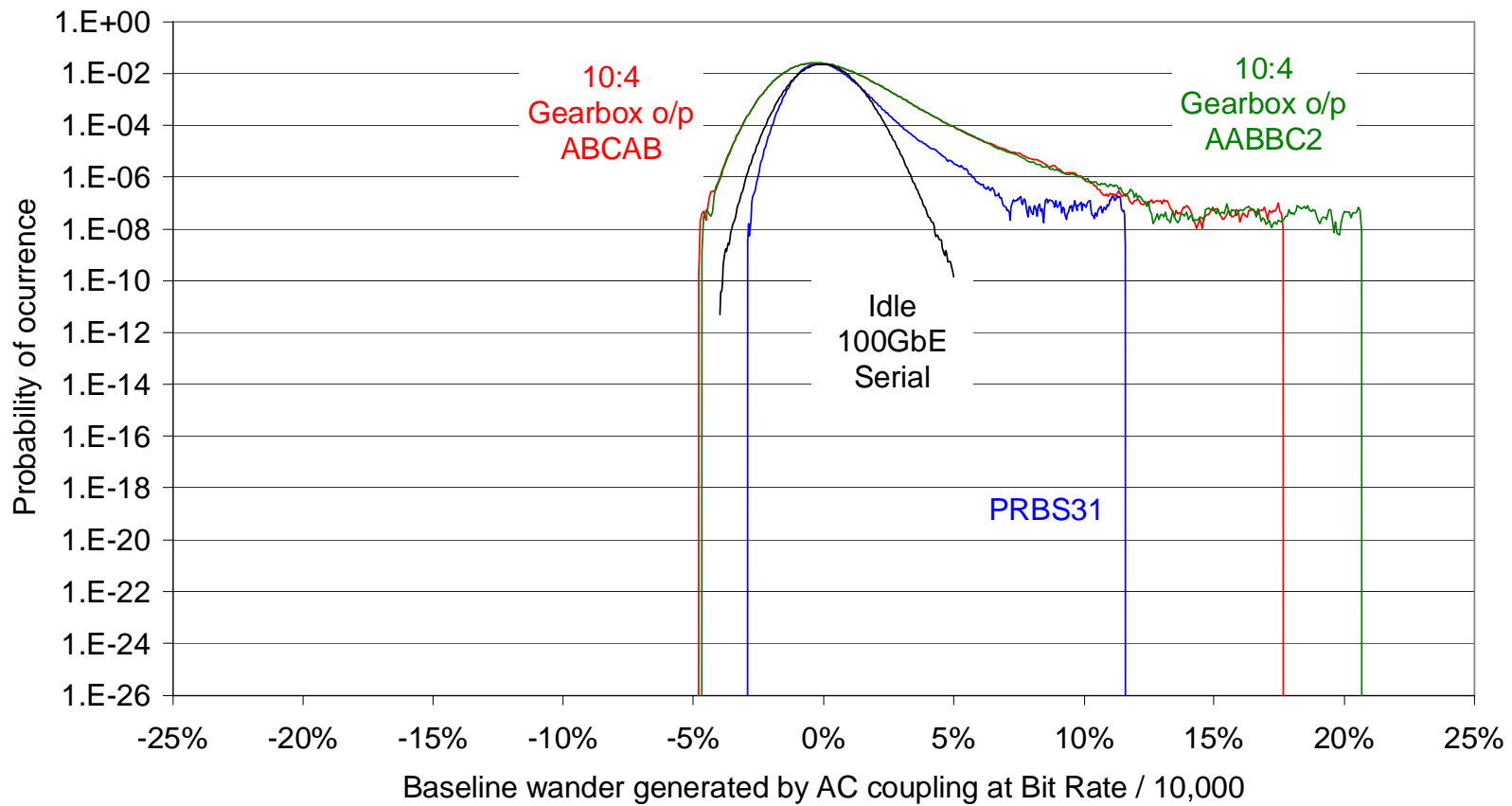
AABBC AABBC ...

With every other bit from sequence C dropped

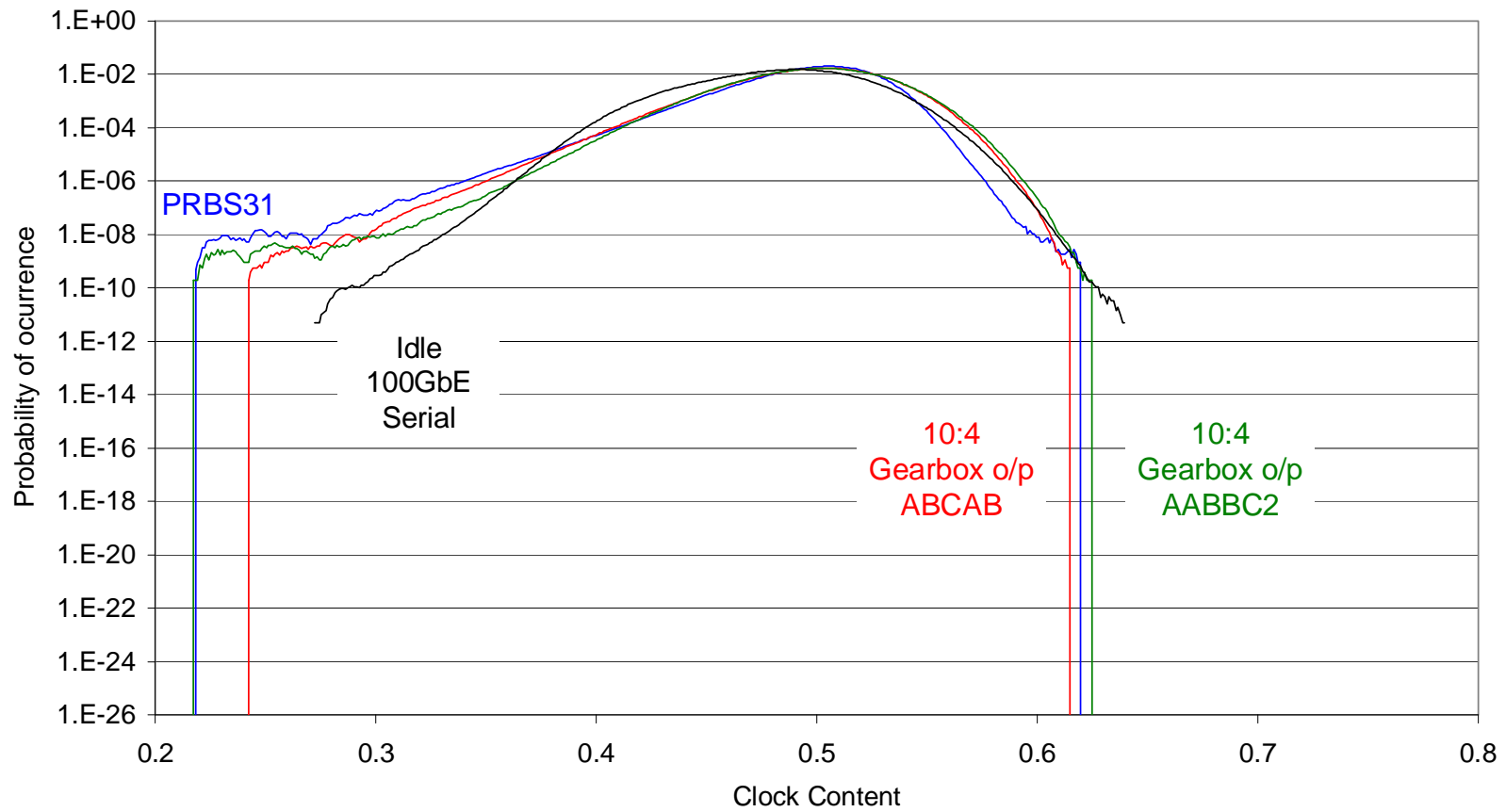
Equivalent to mux structure below



# Baseline wander



# Clock content



Thanks!