

Synchronizing Transmitter Jitter Testing with Receiver Jitter Tolerance

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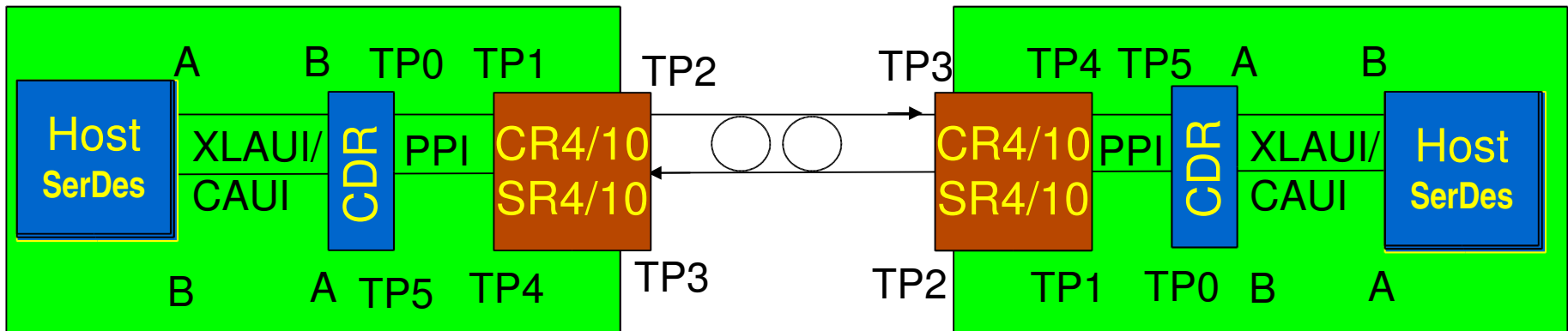
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Problem Statement

- **Clause 52**
 - Transmitter output measured with 4 MHz (CRU) high pass filter
 - Receiver test with worst case allowed transmitter allowed
- **Clause 85**
 - Transmitter output measured with 4 MHz (CRU) high pass filter
 - Receiver interference tolerance does not test the receiver under worst case transmitter allowed low frequency jitter
- **Clause 86**
 - Transmitter output measured with 4 MHz (CRU) high pass filter
 - Receiver jitter tolerance is applied with no other stress an just 2 point where the CDR could be optimized
- **Clause 83A/B**
 - Transmitter output measured with 4 MHz (CRU) high pass filter
 - 83A receiver is test with worst case allowed transmitter, 83B is no clear!
- **CL85/86 credit the transmitter for low frequency jitter but the receiver not tested with the same jitter!**

XLPPPI/CPPI Interfacing to PPI

- The receiving host must operate with jitter accumulation from 2 upstream CDR's
 - The problem is simplified if the local transmit CDR operates in CMU mode
- Non-uniform jitter tolerance applications could make down stream link segment to fail!

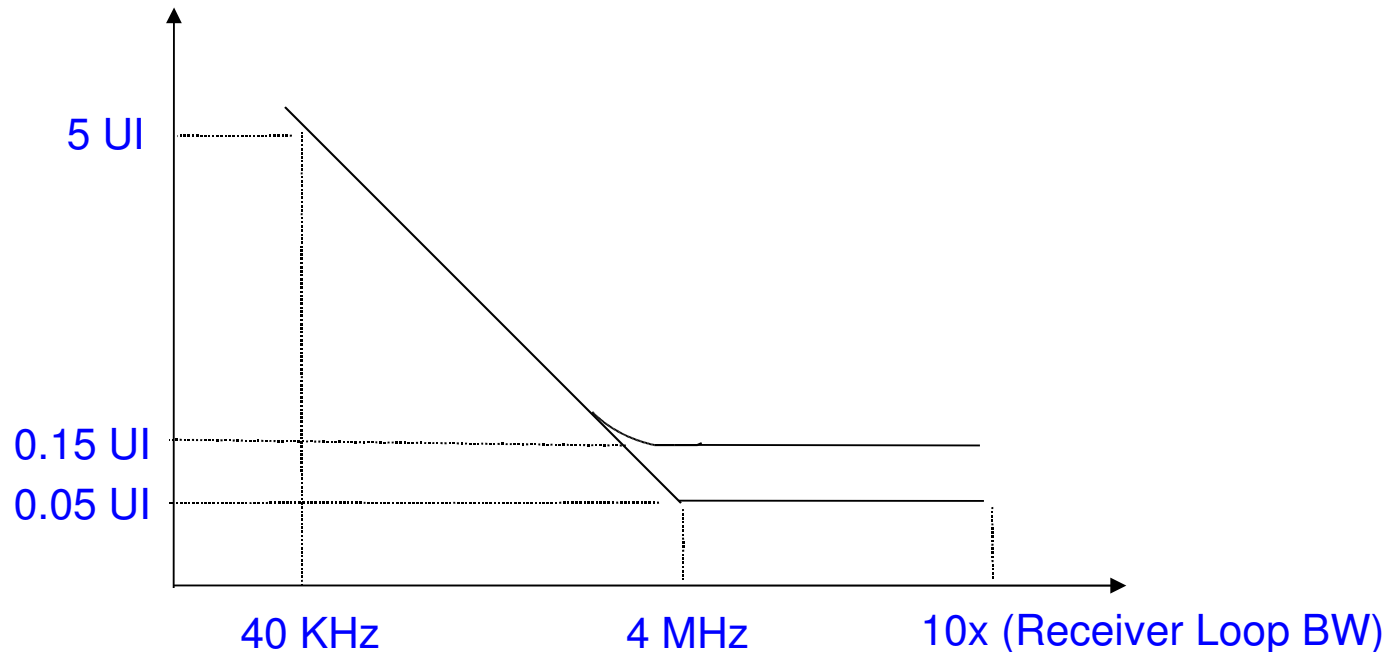


Could There be a Potential Interoperability?

- **What is the function of 4 MHz CRU in CL85/86/83A/83B**
 - Jitter content <4 MHz will be tracked with -20 dB/dec slope
 - The CRU is effectively a high pass jitter filter with 4 MHz BW
 - DC-DC converter, PLL low frequency phase noise, and other low frequency jitter component will be filtered by the CRU
- **Transmitter jitter components filtered by the CRU are always present in the link during operation!**
- **If the receiver is not tested with the same amount of low frequency SJ then the real link may not meet the BER objective**
- **The trend not to test receiver SJ for the credited transmitter SJ started with LRM and KR due to complexity of receiver and the associated burden of tracking low frequency SJ**
- **The best option to move forward is to reduce the CRU BW to 2 MHz but not allow double dipping at the host penalty.**

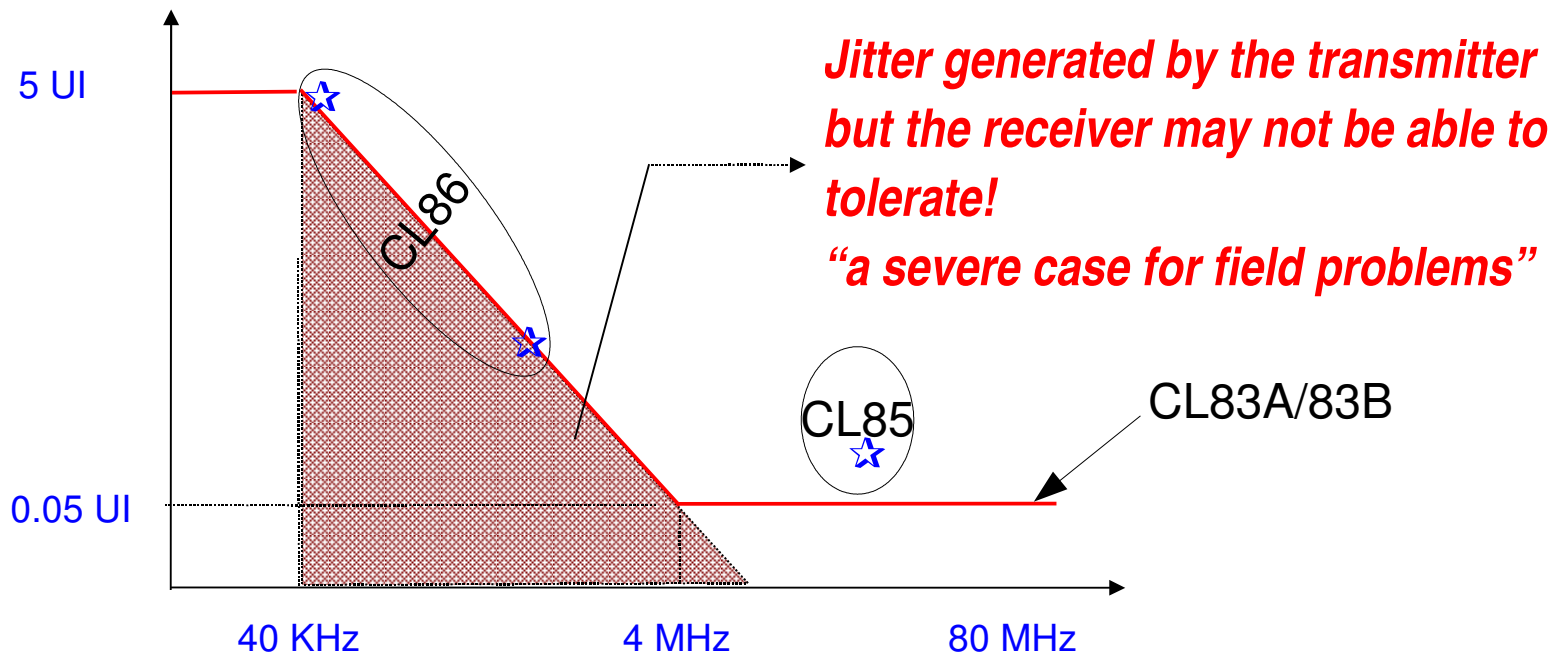
CL52, 83A, 83B Jitter Tolerance Mask

- Jitter corner frequency is 4 MHz
 - CL52 allow SJ to be adjusted from 0.05 to 0.15 UI during calibration
 - 83A/83B has fixed SJ amount is 0.05 UI at 4 MHz



Jitter Tolerance Mask

- Complete lack of commonality on the receiver test but all 3 clauses do take credit for transmitter jitter!
 - CL86 jitter tolerance test is test under no stress!



XLPP/CPPI CDR Specifications

- CDR max BW could be cut by half in order to reduce host jitter tolerance impact

Table 22 XFP Datacom Module Transmitter Requirement

<i>Module Transmitter B'</i>	<i>Symbol</i>	<i>Conditions</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>
Jitter Transfer Bandwidth	BW	PRBS 2 ³¹ -1 Data or Scrambled 64B/66B, see 1			8	MHz
Jitter Peaking		Frequency >50 KHz			1	dB
1. Based on IEEE 802.3ae Clause 52 Sinusoidal Jitter Tolerance Mask Figure 52-4.						

Table 23 XFP Datacom Module Receiver Requirement

<i>Module Transmitter C'</i>	<i>Symbol</i>	<i>Conditions</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>
Jitter Transfer Bandwidth	BW	PRBS 2 ³¹ -1 Data or Scrambled 64B/66B, see 1			8	MHz
Jitter Peaking		Frequency >50 KHz			1	dB
1. Based on IEEE 802.3ae Clause 52 Sinusoidal Jitter Tolerance Mask Figure 52-4.						

Ref <http://www.xfpmsa.org> Rev 4.5

XLPP/CPPI Transmitter Jitter Tolerance

- Transmitter jitter tolerance is the same as chip to chip jitter tolerance

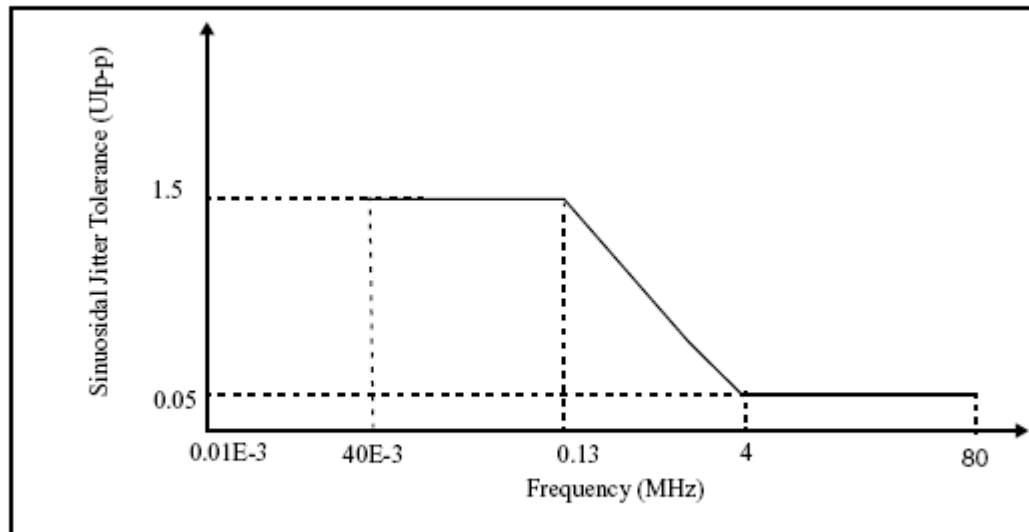


Figure 17 XFI Module Transmitter Input Datacom Margin Mask
Ref <http://www.xfpmsa.org> Rev 4.5

XLPP/CPPI Host Jitter Tolerance

- Include the effect of cascaded CDR's, CDR BW, and jitter peaking
- Reducing the corner frequency from 4 to 2 MHz will help the aggregated CDR's penalty on the host

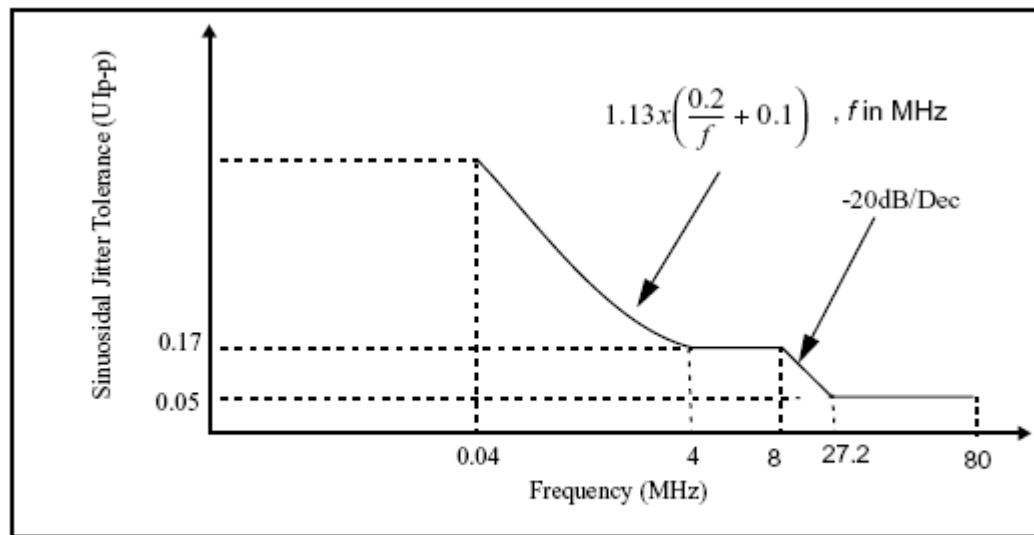


Figure 14 XFI Host Receiver Input Datacom Sinusoidal Jitter Tolerance

Ref <http://www.xfpmsa.org> Rev 4.5

Summary

- **CL85/CL86 either should not take credit for the transmit low frequency jitter or the jitter tolerance must include the credited transmitter low frequency jitter**
- **XLPP/CPPI must deal with the effect of CDR jitter peaking and transfer**
- **To allow bolting XLPP/CPPI to nPP jitter transfer and tolerance must be consistent**
- **A compromise solution would be to make CRU and CDR BW 2 MHz instead of 4 MHz, then require jitter tolerance for CL85/CL86/CL83A/CL83B.**