Insertion loss budget for 40/100GBASE-CR4/10

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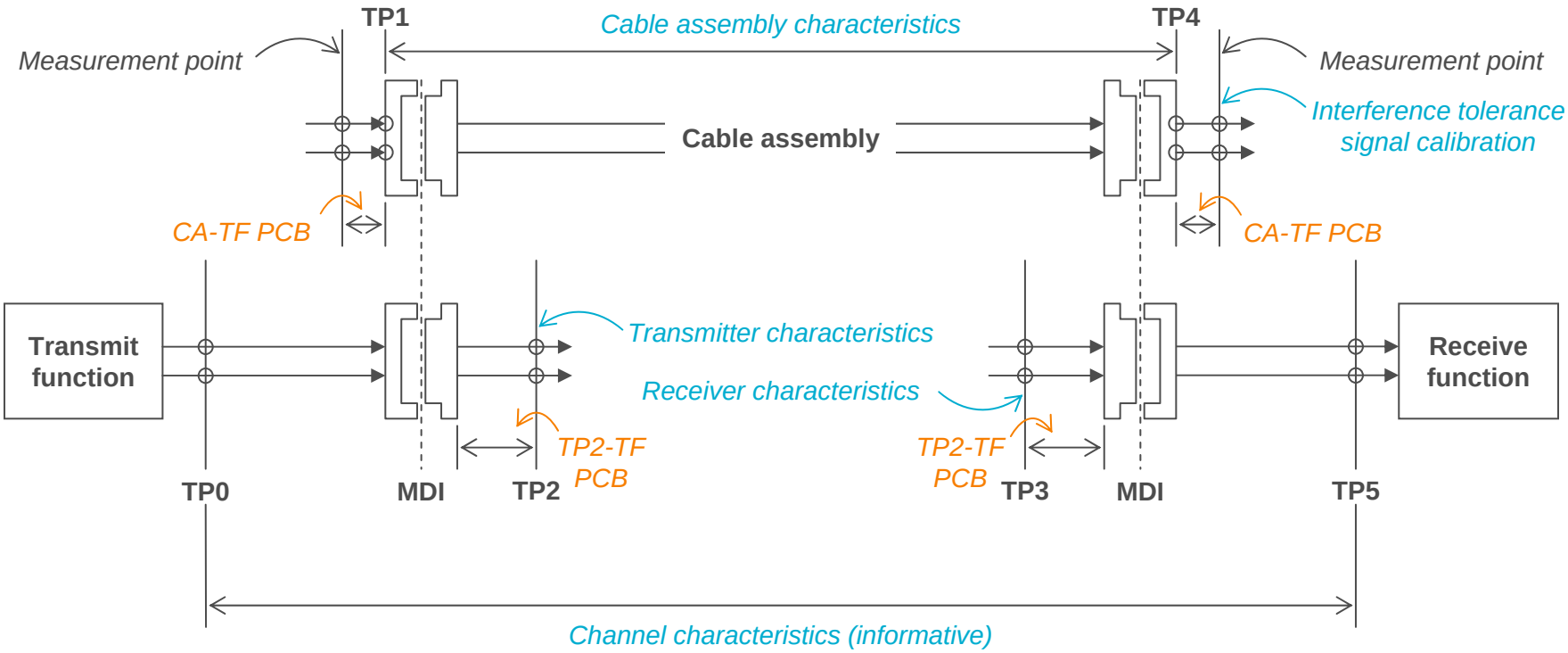
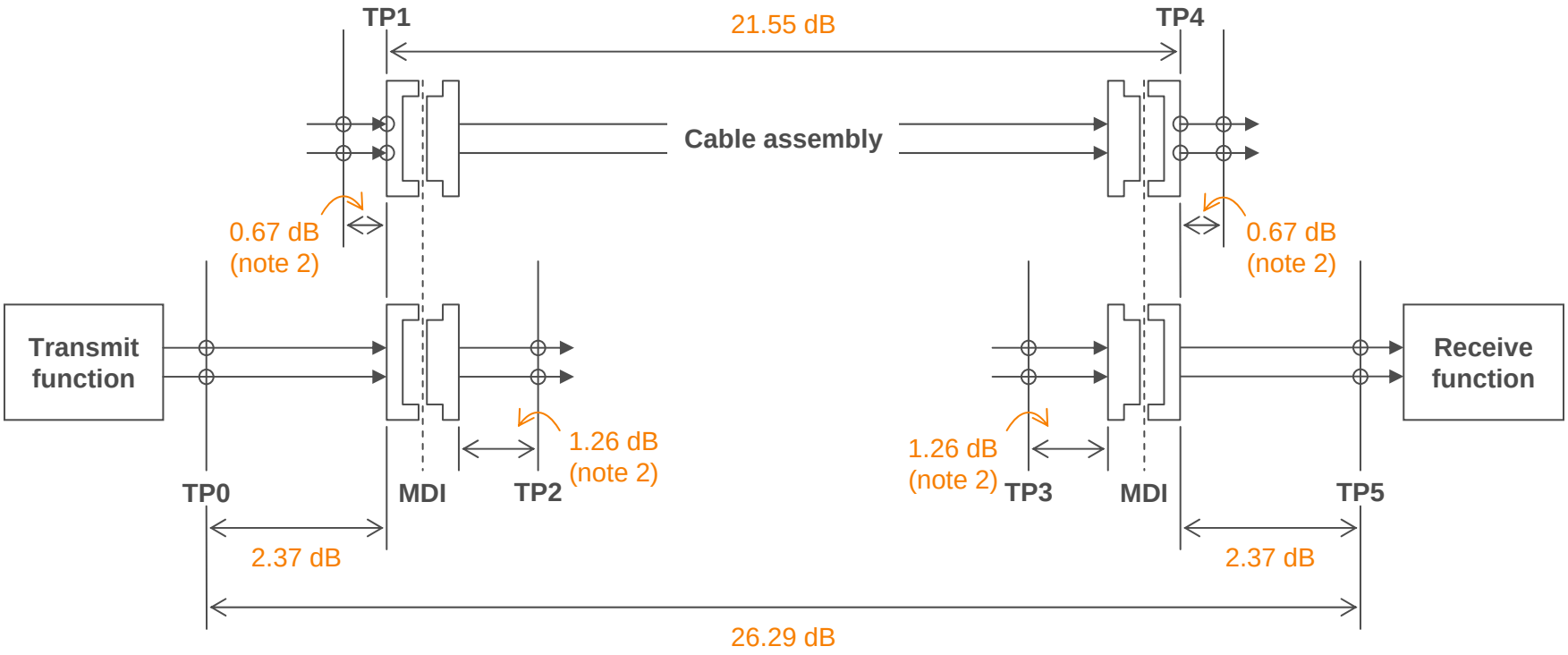
Test points and fixtures – Draft 2.1



Note 1 – 40/100GBASE-CR4/10 TP0 corresponds to 10/40GBASE-KR/4 TP1
Note 2 – 40/100GBASE-CR4/10 TP5 corresponds to 10/40GBASE-KR/4 TP4
Note 3 – Test point 2 test fixture (TP2-TF) corresponds to the host compliance board (HCB) defined in Clause 86
Note 4 – Cable assembly test fixture (CA-TF) corresponds to the module compliance board (MCB) defined in Clause 86
Note 5 – CA-TF PCB is de-embedded from insertion loss measurements

Loss budget – Draft 2.1



NOTE 1 – Quoted insertion loss allowances apply at 5.15625 GHz
NOTE 2 – Intended values; equations in Draft 2.1 are in error

- Compare the loss budget from TP0 to TP5 to the 10GBASE-KR 23.36 dB budget (based on value of A_{max} at 5.15625 GHz)

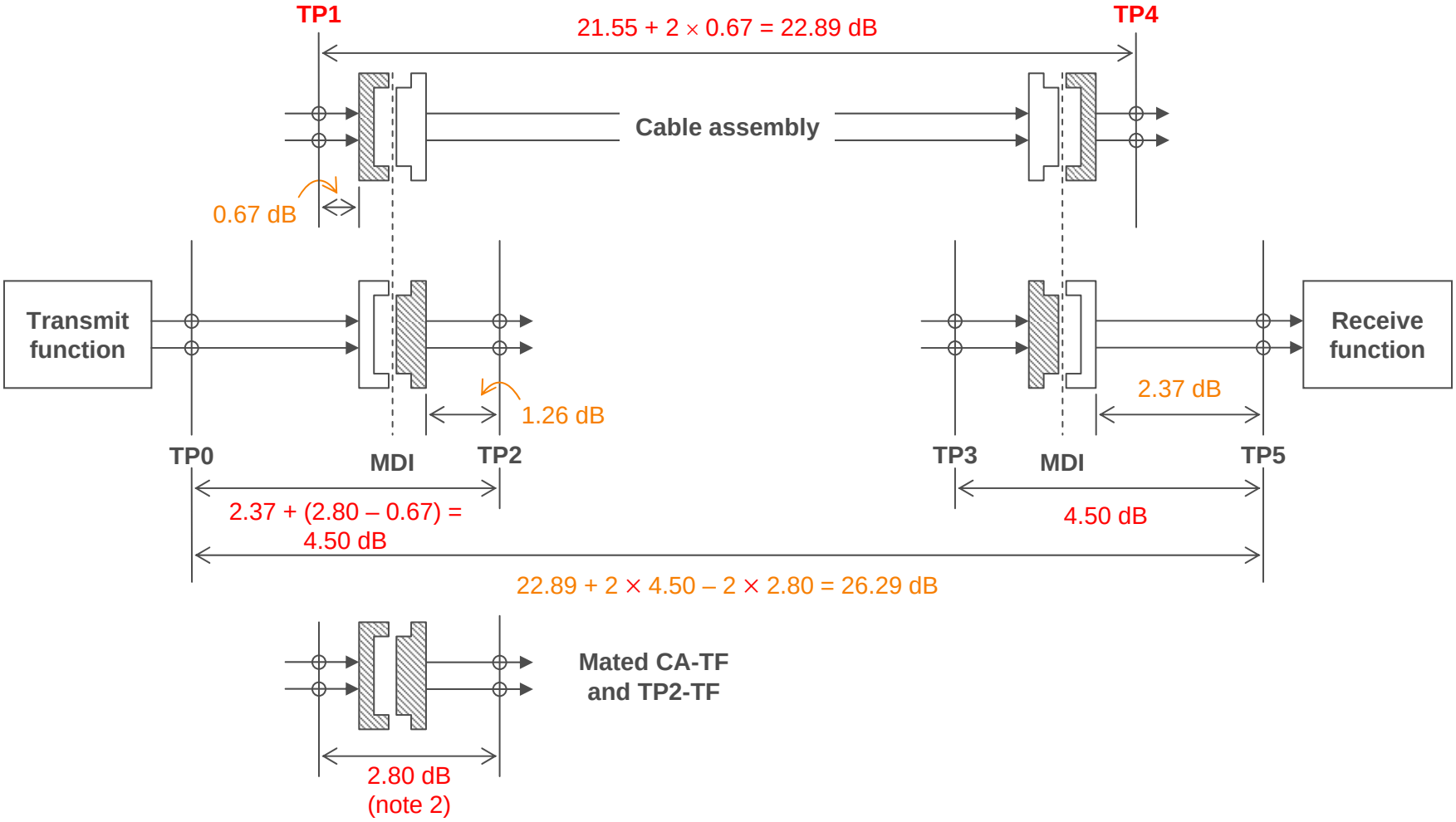
Clarification of test points and fixtures – Comment #114

- Propose to move TP1 and TP4; increase the allowance for cable assembly plus test fixtures accordingly

- Propose to define recommended host channel insertion loss from TP0 to TP2 (and TP3 to TP5)
  - Similar to 86A.6

- Propose to specify normative mated TP2-TF and CA-TF characteristics
  - Similar to 86A.6

Illustration of recommendations

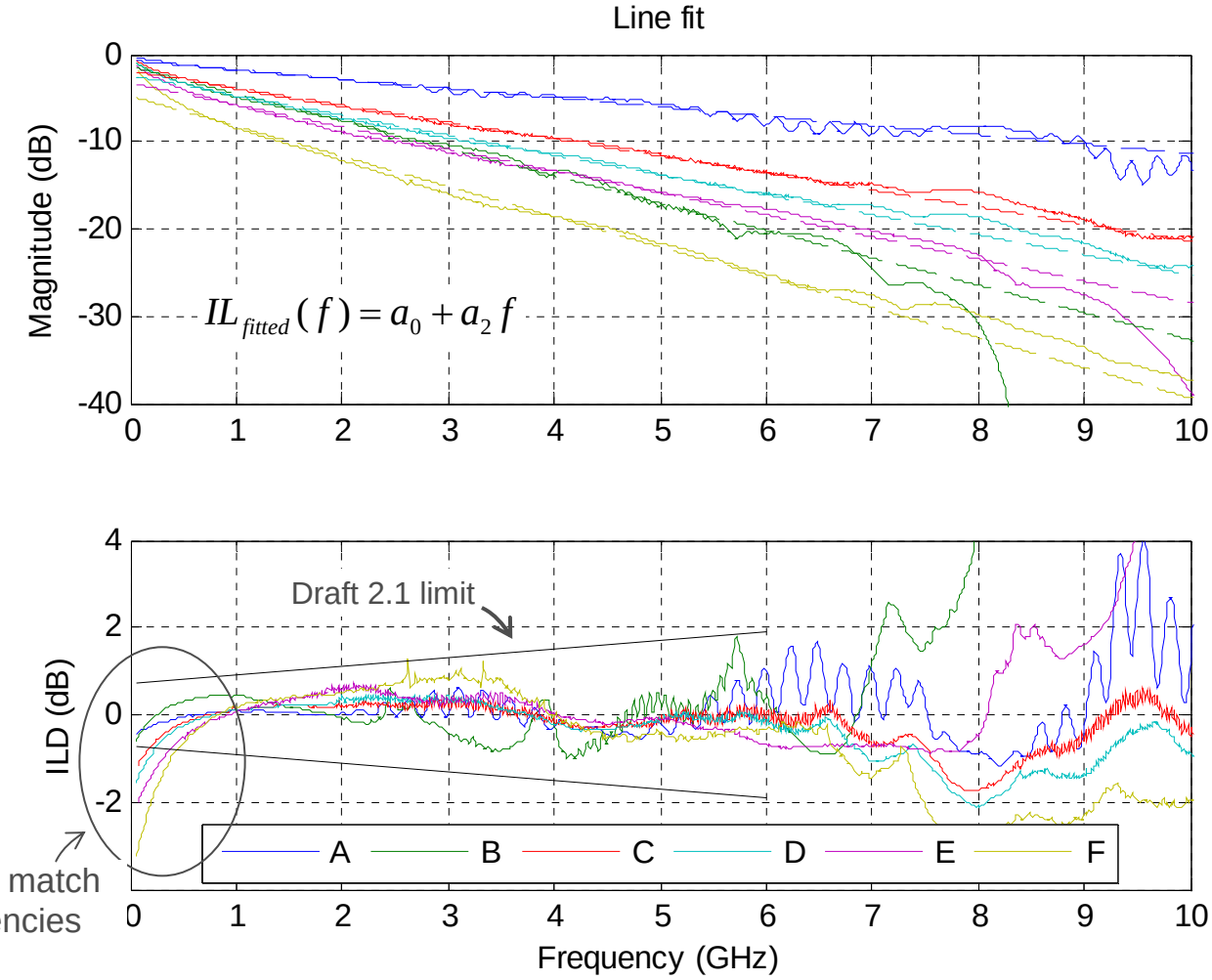


NOTE 1 – Quoted insertion loss allowances apply at 5.15625 GHz
NOTE 2 – From 86A.5.1.1.2, not currently defined in Clause 85

Comments #139, #292 – Fitted insertion loss

- The fitted insertion loss, IL_{fitted}, is defined to be a least mean squares fit of the measured insertion loss, *IL*, to a linear function of frequency
  - This fit is calculated over a frequency range spanning 50 MHz to 6 GHz
- The line fit method is also employed by 10GBASE-KR but that fit is calculated over a frequency range spanning 1 GHz to 6 GHz, where dielectric loss is expected to dominate
- The characteristics of the cable assembly (and channel) are better controlled by expanding the frequency range of the fit but the fitting function must consider "skin effect" losses that are evident at lower frequencies, especially in cable assemblies
- A polynomial in the square root of *f* is a good model for the cable assembly (and channel) insertion loss

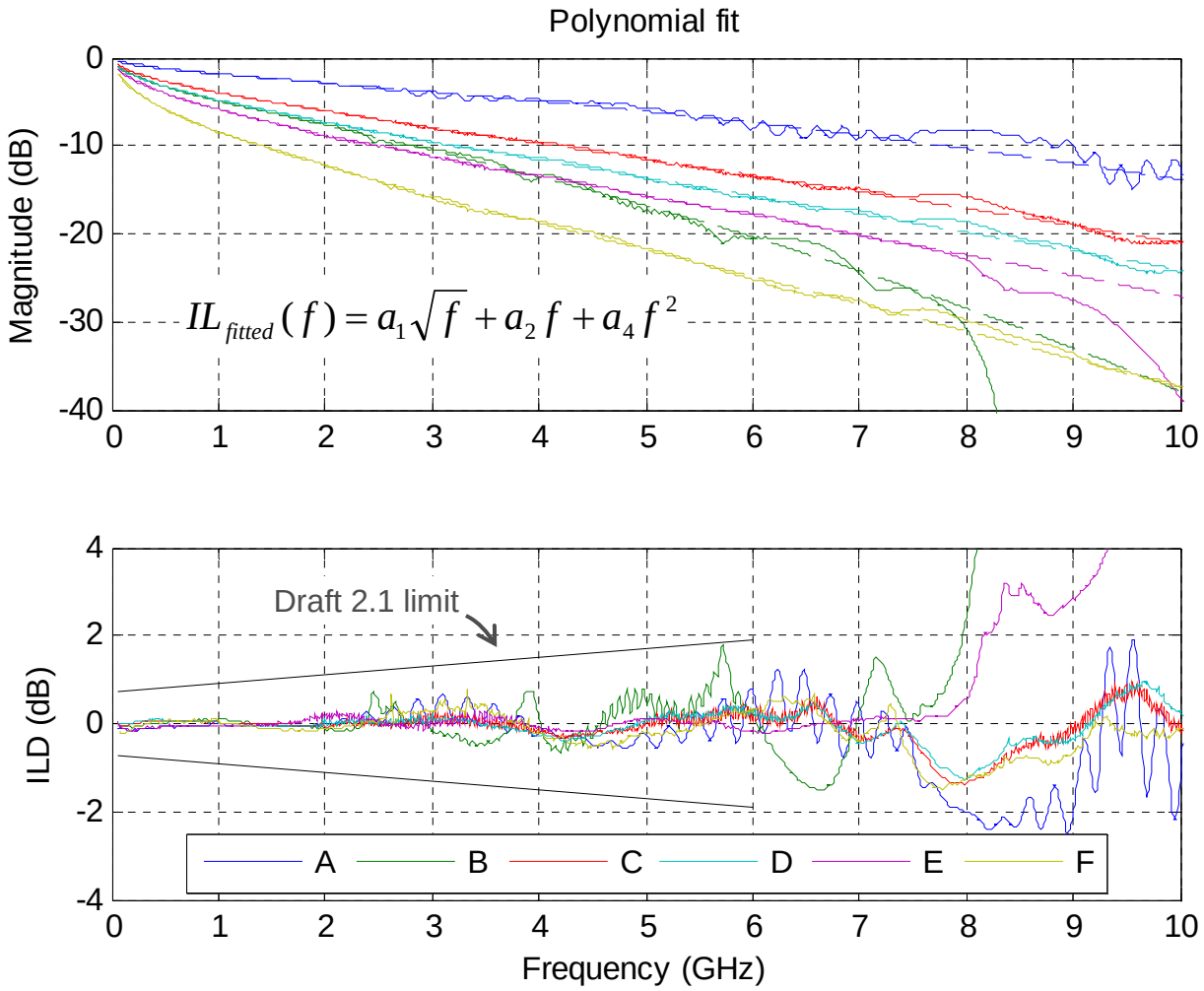
Draft 2.1 – Line fit, 50 MHz to 6 GHz



Line fit is a poor match at lower frequencies

NOTE 1 – Sample A corresponds to a 0.5 m QSFP cable assembly (refer to http://ieee802.org/3/ba/public/channel.html)
NOTE 2 – Sample B corresponds to a 3 m cable assembly with Style 2 MDI (refer to http://ieee802.org/3/ba/public/channel.html)
NOTE 3 – Sample F corresponds to a 10 m QSFP cable assembly (refer to http://ieee802.org/3/ba/public/channel.html)

Proposal – Polynomial fit, 50 MHz to 7.5 GHz



Polynomial fit is a good match across a broad range of frequencies

Comment #139 – Proposal summary

- Replace the line fit method described in 85.10.3 with a polynomial fit
- Constrain the coefficients of the polynomial fit and the insertion loss deviation rather than the insertion loss function itself
  - Delete 85.10.2
  - Bound coefficients of the polynomial fit in accordance with the agreed loss budget
  - Revisit insertion loss deviation requirements in light of the improved fit performance
- Replace test channel requirements of 85.8.4.2 with requirements based on a polynomial fit and associated insertion loss deviation

Comment #200 – Time domain response

- Concerns have been expressed that there are no requirements placed on the cable assembly (or channel) phase response hence the time domain response is not adequately constrained
  - Also refer to Draft 2.0 unresolved comment #75

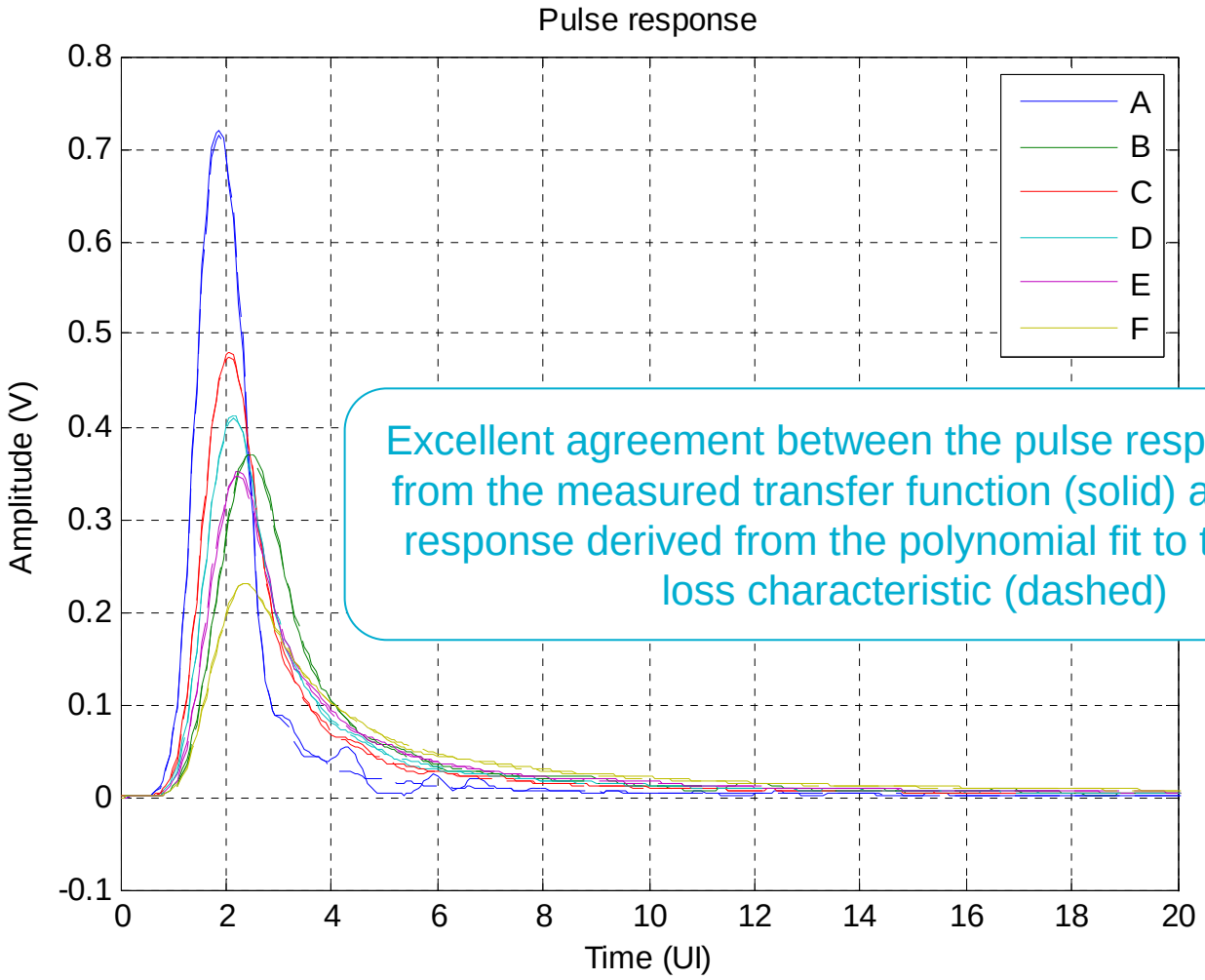
- It can be shown that, for a minimum phase system (linear, causal, stable), there exists a relationship between the phase response of the system and the logarithm of its magnitude response (note 1)

- It has been shown that the insertion loss of the cable assembly and channel is effectively modeled as a polynomial in the square-root of frequency

- It follows that phase response, and therefore the time domain response, may be derived from the polynomial model of the cable assembly (channel) insertion loss

NOTE 1 – Oppenheim, A. V. and R. W. Schafer, *Discrete-Time Signal Processing*, Englewood Cliffs, NJ, Prentice-Hall, 1989.

Pulse response comparison



Excellent agreement between the pulse response derived from the measured transfer function (solid) and the pulse response derived from the polynomial fit to the insertion loss characteristic (dashed)

Comment #200 – Conclusion

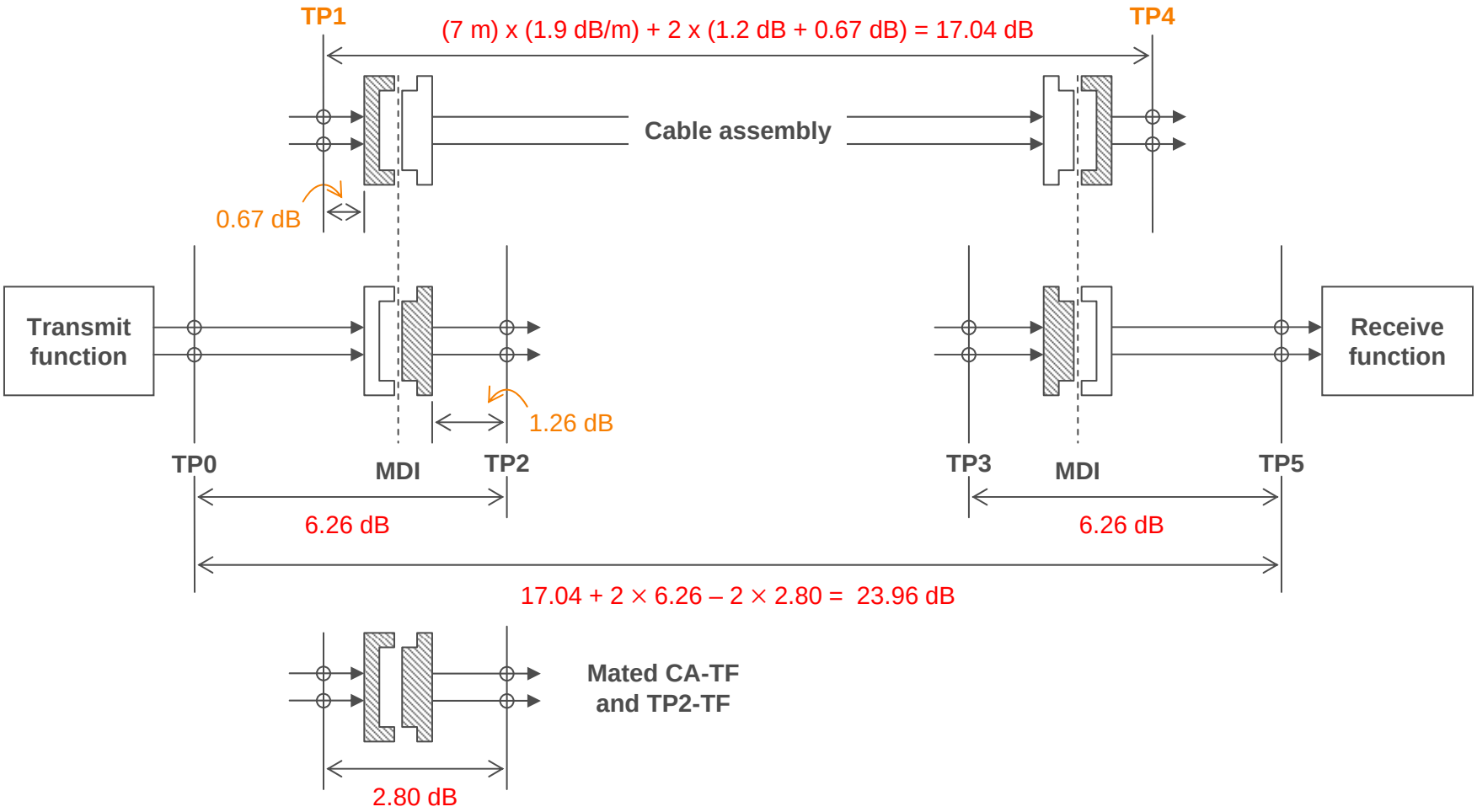
- Constraints on the least mean squares fit polynomial coefficients and the insertion loss deviation are sufficient to constrain the time domain response of the cable assembly (channel)

Host insertion loss allowance – Comments #96, #165

- Comment #96 suggests that the host printed circuit board (PCB) and connector insertion loss allowance be increased
  - 5.0 dB at 5.15625 GHz for the PCB trace, connector, and other impairments
  - 3.5 dB for the PCB trace only
  - This implies that the TP0 to TP2 (and TP3 to TP5) insertion loss allowance is 6.26 dB
  - To maintain a consistent loss budget. the commenter recommends that the cable assembly reach objective be reduced to 7 m

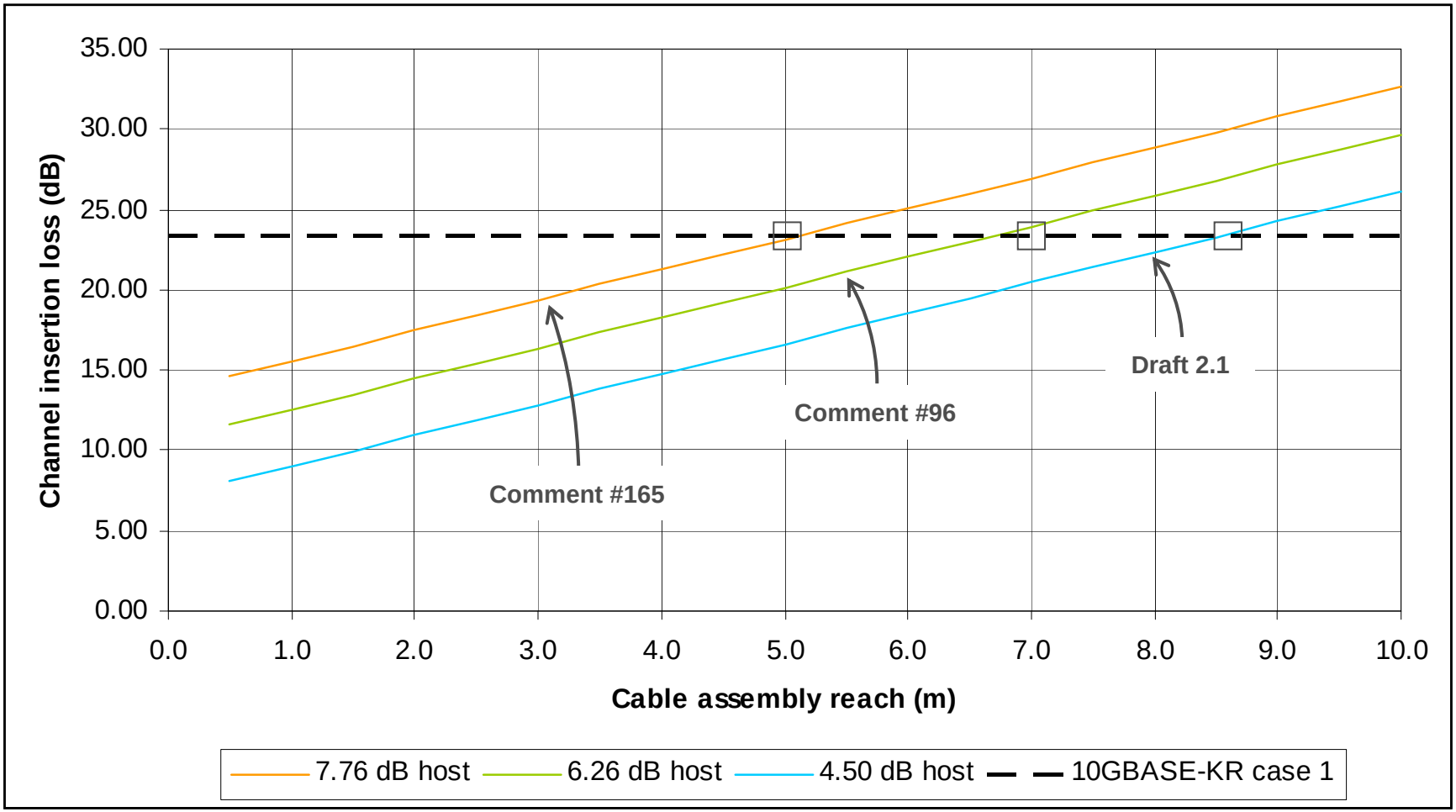
- Comment #165 suggests that the allowance for the host PCB trace alone be increased to 5.0 dB
  - Assume that this translates to a TP0 to TP2 (and TP3 to TP5) insertion loss allowance of 7.76 dB

Loss budget – 7 m, 6.26 dB host insertion loss



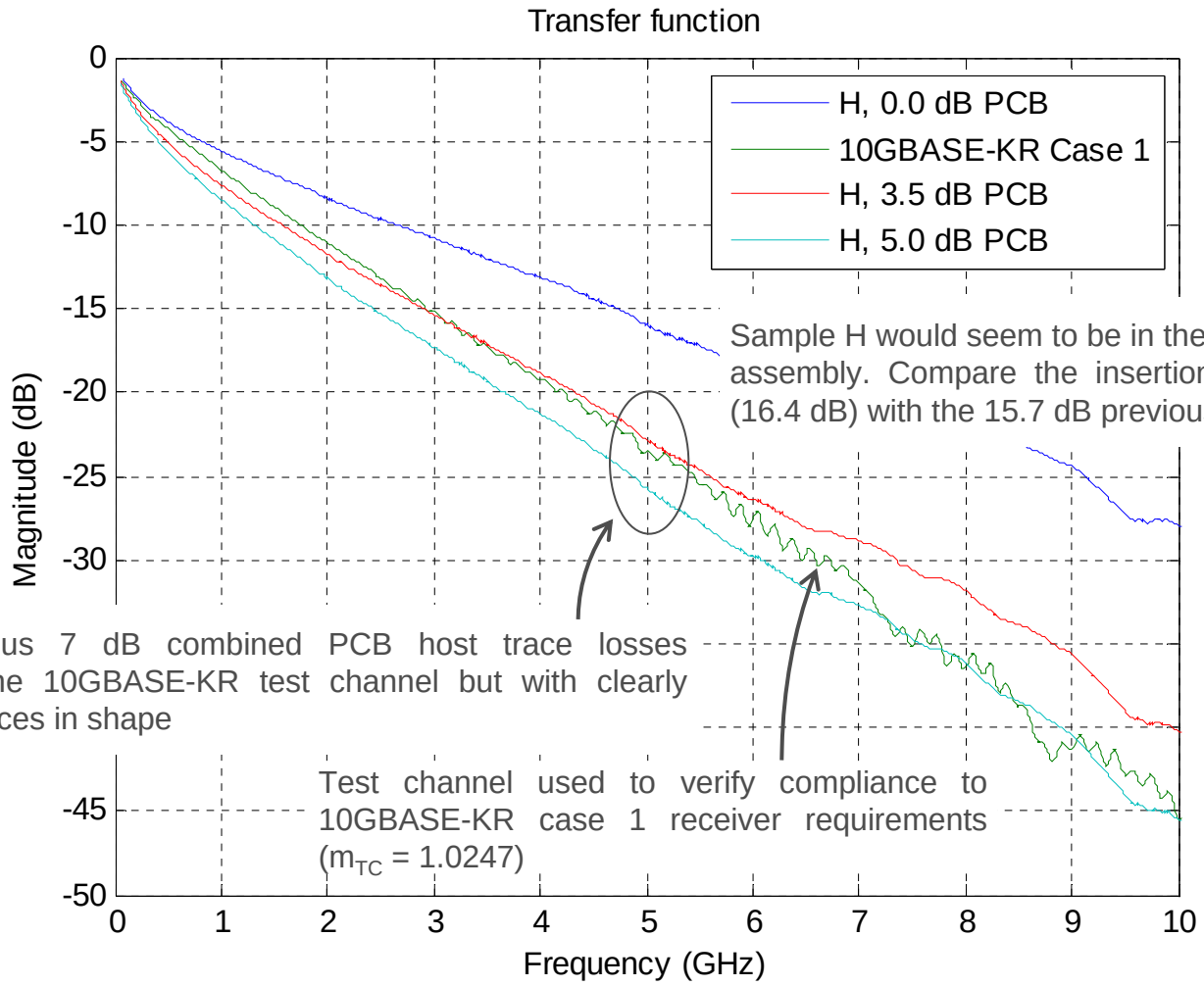
NOTE – Cable assembly insertion loss based on 1.2 dB per host receptacle and cable plug and 1.9 dB/m for 4-pair 24AWG bulk cable. This implies an insertion loss of 15.70 dB for a 7 m cable assembly.

Loss budget scenarios



NOTE 1 – Cable assembly insertion loss based on 1.2 dB per host receptacle and cable plug and 1.9 dB/m for 4-pair 24AWG bulk cable.
NOTE 2 – Host insertion loss includes printed circuit board trace, connector, and TP2 test fixture.

Loss budget investigation – Transfer functions



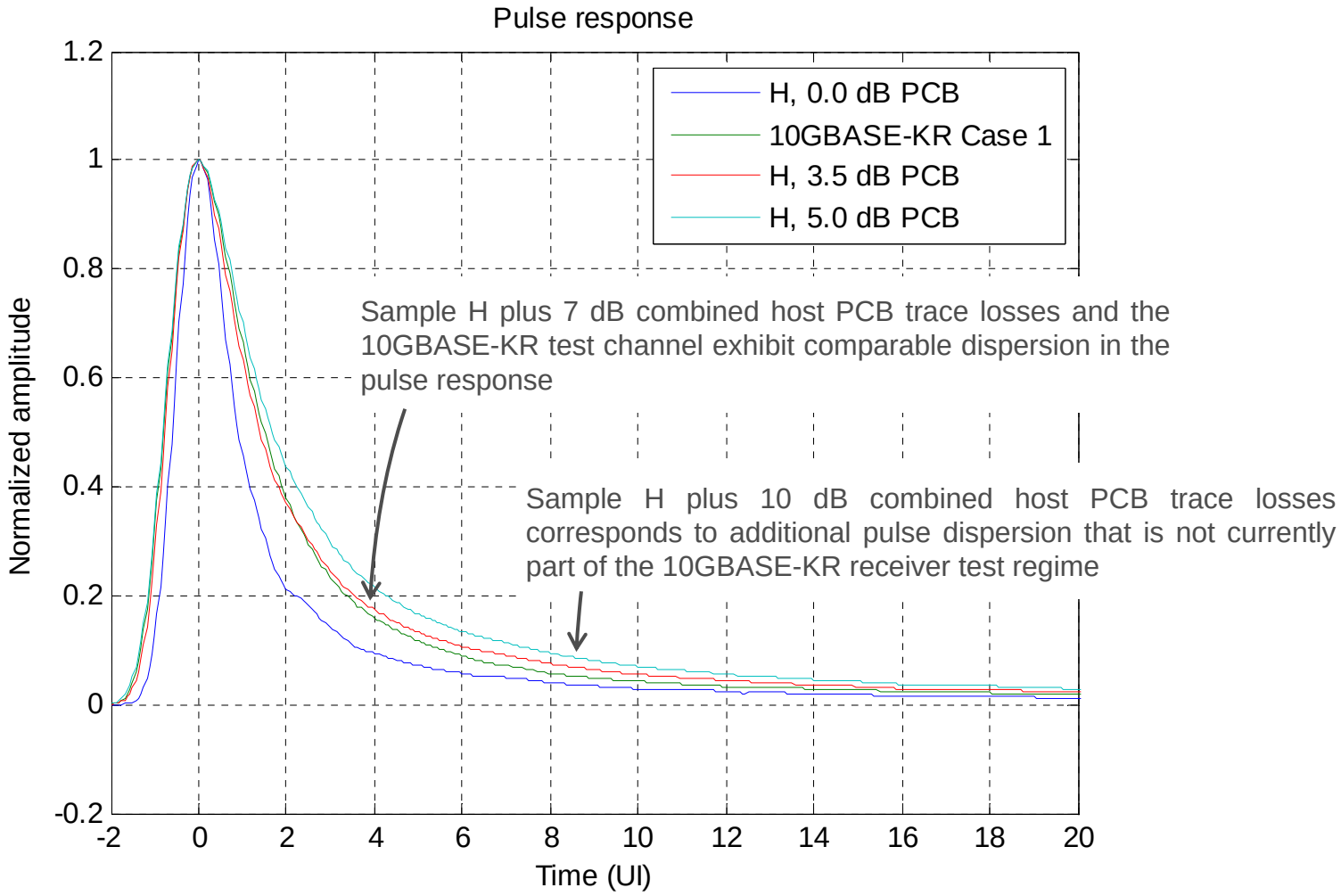
Sample H would seem to be in the ballpark for a 7 m cable assembly. Compare the insertion loss at 5.15625 GHz (16.4 dB) with the 15.7 dB previously calculated

Sample H plus 7 dB combined PCB host trace losses comparable the 10GBASE-KR test channel but with clearly visible differences in shape

Test channel used to verify compliance to 10GBASE-KR case 1 receiver requirements (m_{TC} = 1.0247)

NOTE – 10GBASE-KR case 1 transfer function compensated for b_{TC}.

Loss budget investigation – Pulse responses



Observations

- 10GBASE-KR compliant solutions may be expected to support a 7 m cable assembly with host transmitter and receiver printed circuit board traces each exhibiting an insertion loss of 3.5 dB at 5.15625 GHz

- The insertion loss for a channel that includes 5.0 dB of printed circuit board trace loss at both the transmitter and receiver exceeds what is currently required for 10GBASE-KR receiver testing
  - Existing solutions may support this operating point but no general statements may be made based on the 10GBASE-KR specifications alone

- Note that comment #38 suggests that the mean time to false packet acceptance (MTTFPA) analysis for 40/100GBASE-CR4/10 may not be valid
  - It employs 10GBASE-KR error propagation statistics while 40/100GBASE-CR4/10 links exhibit more dispersion
  - Presumably, working within the 10GBASE-KR loss budget would alleviate this concern

Interference tolerance test channel – Comment #138

- Propose to define the test channel based on a polynomial fit similar to what has been recommend for the cable assembly and TP0 to TP5 channel
  - Specify values for the polynomial coefficients
  - Constrain the insertion loss deviation relative to the fit

- Proposed to define the test channel to include the transmitter printed circuit board allowance, cable assembly insertion loss allowance, and a cable assembly test fixture allowance
  - Do not included the receiver printed circuit board allowance since this is integrated into the receiver under test