Proposed update to BIP-8 mechanism
D2.1 Comment 270

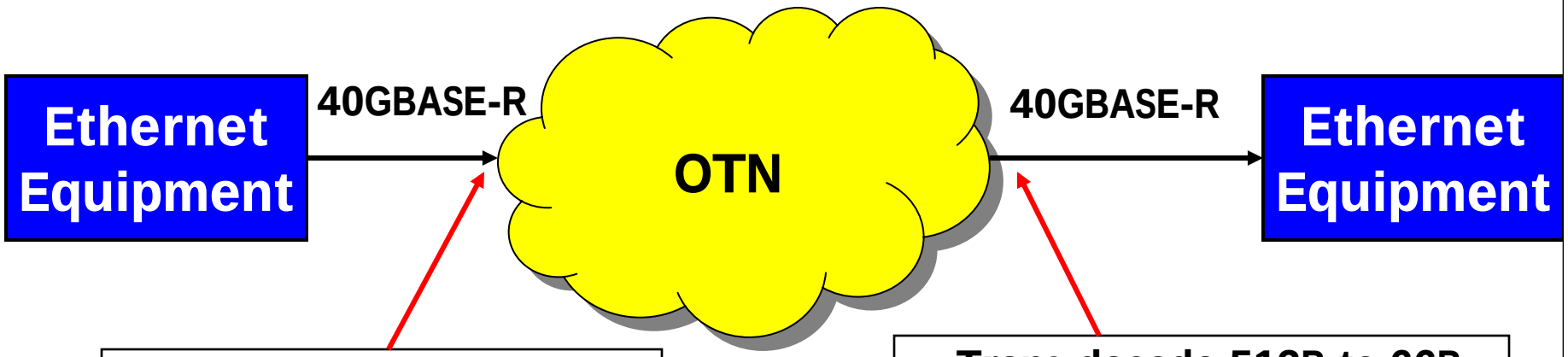
Stephen J. Trowbridge
Alcatel-Lucent

BIP-8 background

- BIP-8 added to lane alignment markers at New Orleans meeting (Jan 2009)
- BIP-8 as compared with SONET/SDH or OTN BIP:
  - Transport technology BIP tends to be calculated inside the scrambler while P802.3ba D2.1 calculates it outside the scrambler. There are some good reasons for this (e.g., the error multiplication effect of the Ethernet scrambler and the order of operations performed in the PCS), but this has been problematic for 40GBASE-R transcoding over OTN
  - Block size differences:
    - OTN BIP counts one error if the BIP-8 does not match for the entire frame (3808×4 bytes, 121'856 bits
    - STM-256/OC-768 B1 counts one error if the BIP-8 does not match for the entire frame (270×9×256 bytes, 4'976'640 bits)
    - STM-256/OC768 B2 is 256 bytes (2048 bits) long, each bit covering a block of 2430 bits. One error counted for each of the 2048 bits that is incorrect.
    - Current 40/100GBASE-R BIP, six bits are calculated as parity over 131'072 bits, and two bits are calculated as parity over 147'456 bits
    - Proposed update: Calculate 40/100GBASE-R BIP like SONET/SDH B1 or OTN BIP, and count one error if the BIP-8 value does not match over 16'384×66=1'081'344 bits

40GBASE-R over OTN with Transcoding

How is end-to-end error monitoring supported by the OTN mapping?



- XOR expected BIP with received BIP to create error mask
- Descramble
- Calculate OTN-PCS lane BIP on descrambled 66B
- Transcode 66B to 513B code blocks

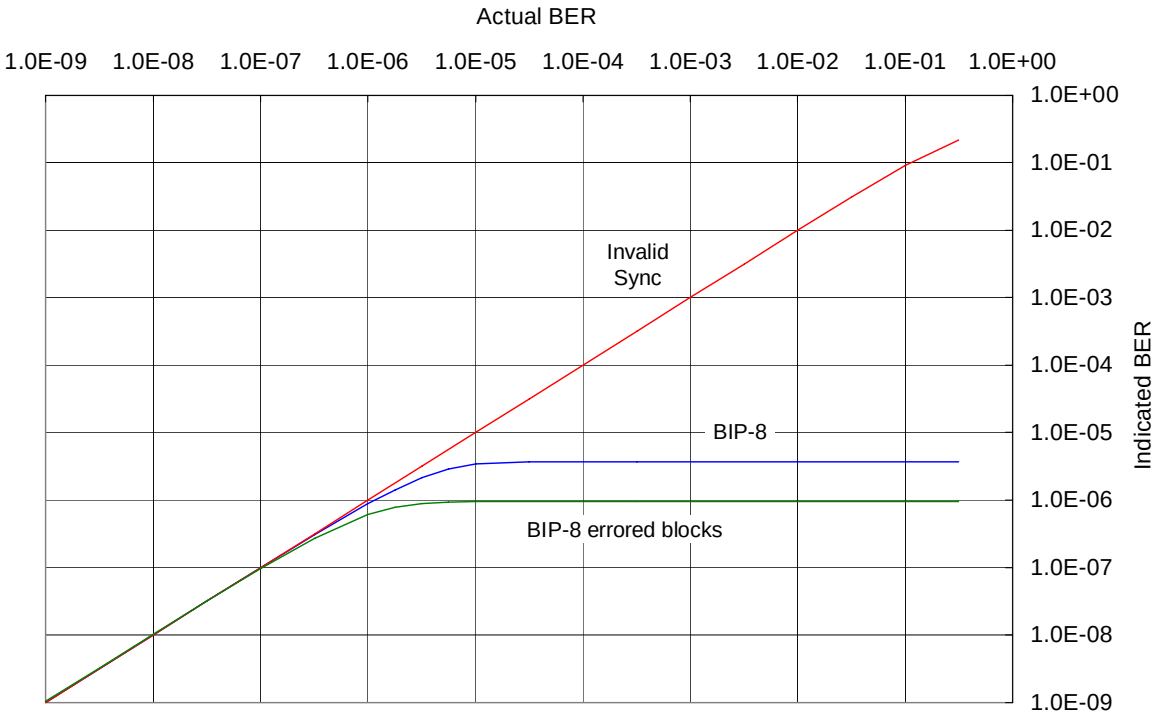
- Trans-decode 513B to 66B code blocks
- XOR expected OTN-PCS lane BIP with received OTN-PCS lane BIP to calculate OTN-PCS lane error mask
- Rescramble 66B
- Calculate new BIP-8 per PCS lane
- XOR with ingress and OTN-PCS lane error masks

Error counting with 40GBASE-R transcoding

- Bit errors from the OTN egress to the Ethernet Rx create an accurate indication in the BIP-8 seen by the Ethernet Rx
- Bit errors in the OTN, if they result in a non trans-decodable 513B code block, will result in replacement of the entire code block with eight 66B error control blocks (SH=10, 0x1e, 8×/E/). A bit error in one PCS lane could result in errors being observed on all PCS lanes, but this only occurs if the error is in a part of the link where all PCS lanes are carried together over a single OPU3. Note that this is the least likely place for errors to occur since OTN (especially at 40G) is nearly always protected by FEC
- Bit errors from the Ethernet Tx to the OTN ingress, if they hit a SH or control block type, will result in the entire 66B block being replaced by an error control block (SH=10, 0x1e, 8×/E/) before transcoding. If errors are counted on a bit-basis, this could replace a single bit error with an average of 4 observed bit errors. The bits that are vulnerable to this range from ~2/66 (3%) for a fully occupied link (mostly data blocks) to 10/66 (~15%) for a fully idle link.

Proposed Remedy

- Count errors like OTN or SDH/SONET B1 (count one error for each incorrect BIP-8 value)
- Generally will give the same error count even when bit errors hit the SH or control block type between the Ethernet Tx and OTN ingress (missing only 1/256 of the cases where by accident the error control block makes a good BIP)
- Saturates a factor of 4 lower (green line added to chart from nicholl_01_0109), but the mechanism is being used to verify 10^{-12}, not 10^{-5} or 10^{-6}. Within the range of interest, the count is the same



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Specific text proposal

Page 179, lines 12-13

Replace:

"As part of the alignment marker removal process, the BIP3 field is compared to the calculated BIP value for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register is incremented for each BIP bit in error (registers 3.90 through 3.99)."

With:

"As part of the alignment marker removal process, the BIP3 field is compared to the calculated BIP value for each PCS lane. If a Clause 45 MDIO is implemented, then the appropriate BIP error counter register is incremented for each 8-bit BIP value in error (registers 3.90 through 3.99)."