Interface classifications

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Supporters

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- Gary Nicholl – Cisco
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- Brad Booth – AMCC
- Shimon Muller – Sun Microsystems

Interface classifications

- Abstract:
  - Service primitives (function calls, pseudo code)
  - Clause 2 (MAC service interface), Clause 6 (MAC/PLS service interface)
- Logical:
  - Signals, code-points, syntax, sequences, true/false
  - Clauses 22 (MII), 35 (GMII), 46 (XGMII), etc
- Electrical:
  - AC/DC parameters
  - Clauses 22 (MII), 54 (CX4)
- Optical:
  - Active output/active input parameters
  - Clauses 38, 52, 58-60, etc
- Physical:
  - Mechanical inter-matebility
  - Clause 38 (by reference to duplex SC in 38.11.3)
  - Clause 54 (by reference to 61076-3-113 in 54.8.1)

Abstract interfaces

- Formally defined using service primitives
  - MA_DATA.request (DA, SA, MSDU, FCS)
  - MA_DATA.indication (DA, SA, MSDU, FCS, Status)
- May be defined in pseudo-code
  - TransmitBit, ReceiveBit, Wait, transmitting, receiveDataValid, carrierSense
- Described from the perspective of the subordinate layer (or sub-layer)

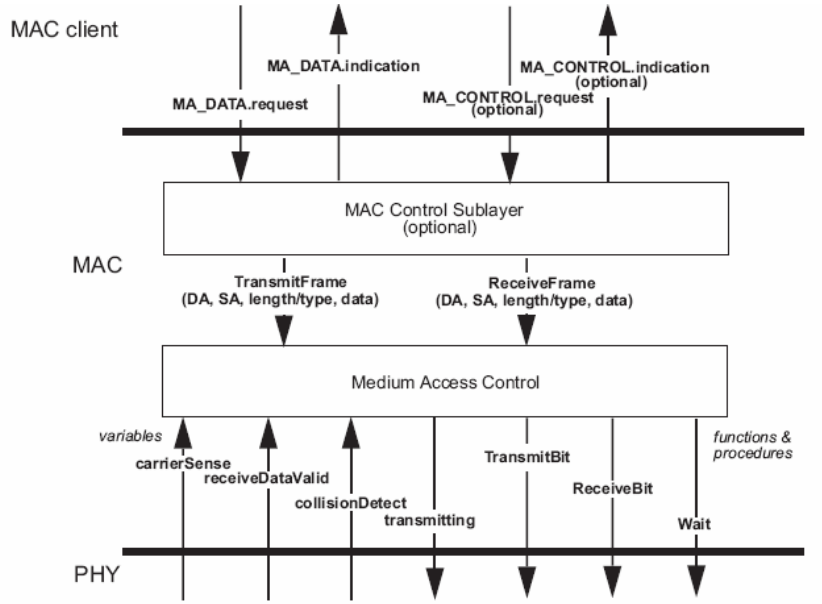


Figure 2–1—Service specification primitive relationships (optional MAC control sublayer implemented)

Abstract interfaces

- Can be mapped to logical interfaces
    - MAC/PLS service interface mapped to MII, GMII, XGMII in Clauses 22, 35, 46
- Provides consistent behavior across many generations of implementation

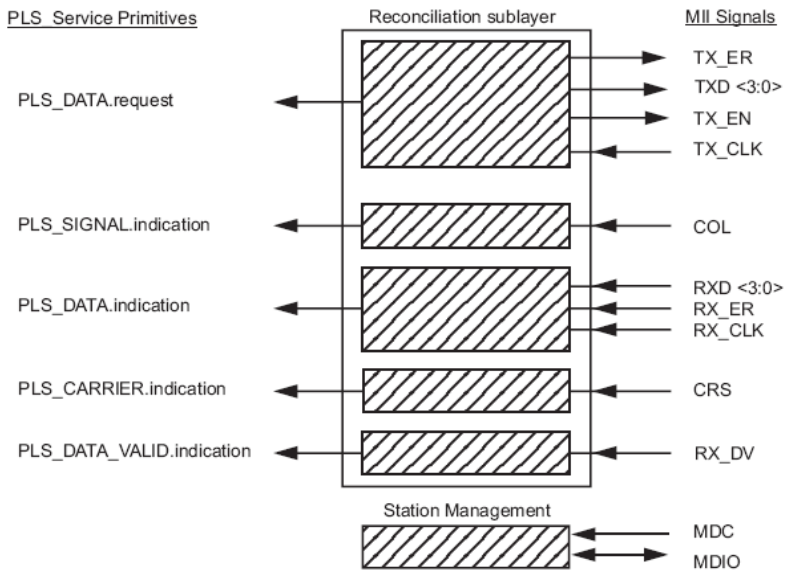


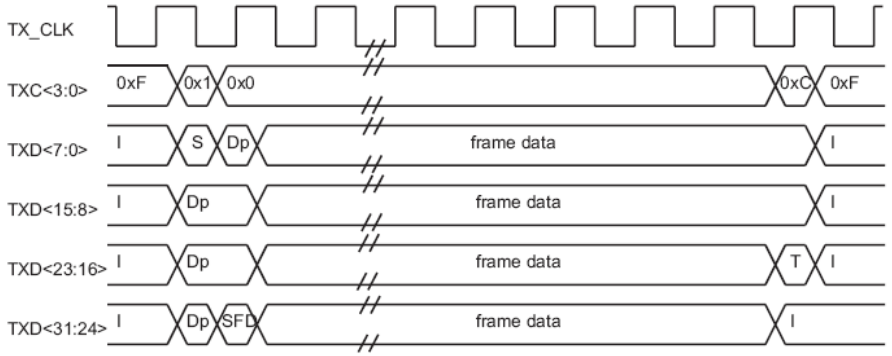
Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII

Abstract interfaces

- Advantages
  - implementation independent
  - long-lived
  - brief specification
- Disadvantages
  - intangible
  - do not ensure interoperability
    - no conformance test points

Logical interfaces

- The behavioral specification of an abstract interface, plus
- Signals, code-points, syntax, sequences, etc
  - TXD<31:0>, RXD<31:0>, TXC<3:0>, RXC<3:0>, TX_CLK, RX_CLK



I: Idle control character, S: Start control character, Dp: preamble Data octet, T: Terminate control character

Figure 46–5—Normal frame transmission

Logical interfaces

- Advantages
  - easy to map to Register Transfer Level (RTL) hardware descriptive languages (HDL)
  - more rigorous than abstract interfaces
- Disadvantages
  - do not ensure interoperability
    - since there is no definition of the logic levels
  - take longer to specify than abstract interfaces
  - not as long-lived as abstract interfaces

Electrical interfaces

- The specification of a logical interface, plus
- DC characteristics
  - Voh, Vol, Vih, Vil, Ioh, Iol, Iih, Iil, etc
- AC characteristics
  - Tr, Tf, Tsu, Thd, etc

Table 35–7—DC specifications

Symbol	Parameter	Conditions		Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	V_{CC} = Min	2.10	3.60	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA	V_{CC} = Min	GND	0.50	V
V_{IH}	Input High Voltage			1.70	—	V
V_{IL}	Input Low Voltage			—	0.90	V
I_{IH}	Input High Current	V_{CC} = Max	V_{IN} = 2.1 V	—	40	µA
I_{IL}	Input Low Current	V_{CC} = Max	V_{IN} = 0.5 V	–600	—	µA

Electrical interfaces

- Advantages
  - very rigorous
  - high degree of interoperability
    - since it can be probed and measured
- Disadvantages
  - take longer to specify than logical interfaces
  - not as long-lived as logical or abstract interfaces

Optical interfaces

- Specify transmit characteristics
  - Wavelength, spectral width, launch power, optical modulation amplitude, return loss, etc
- Specify receive characteristics
  - Wavelength, receive sensitivity, overload, etc

Table 59–5—1000BASE-LX10 receive characteristics

Description	Value	Unit
Signaling speed (range)	1.25 ± 100 ppm	GBd
Wavelength (range)	1260 to 1360	nm
Average receive power (max)	–3	dBm
Receive sensitivity (max)	–19.5	dBm
Receiver sensitivity as OMA (max)	–18.7 (13.4)	dBm (μW)
Bit error ratio (max)	10^{-12}	
Receiver reflectance (max)[a]	–12	dB
Stressed receive sensitivity (max)	–15.4	dBm
Stressed receiver sensitivity as OMA (max)	–14.6 (35)	dBm (μW)
Vertical eye-closure penalty (min)	3.6	dB

Optical interfaces

- Advantages
  - most rigorous
  - highest degree of interoperability
- Disadvantages
  - take a looooooooong time to specify
  - specification methods constantly evolve

Physical interfaces

- Specify mechanical inter-matebility
  - dimensions, clearances, etc. usually defined by reference to an IEC standard
- Specify contact assignments

Table 54–7—CX4 lane to MDI connector pin mapping

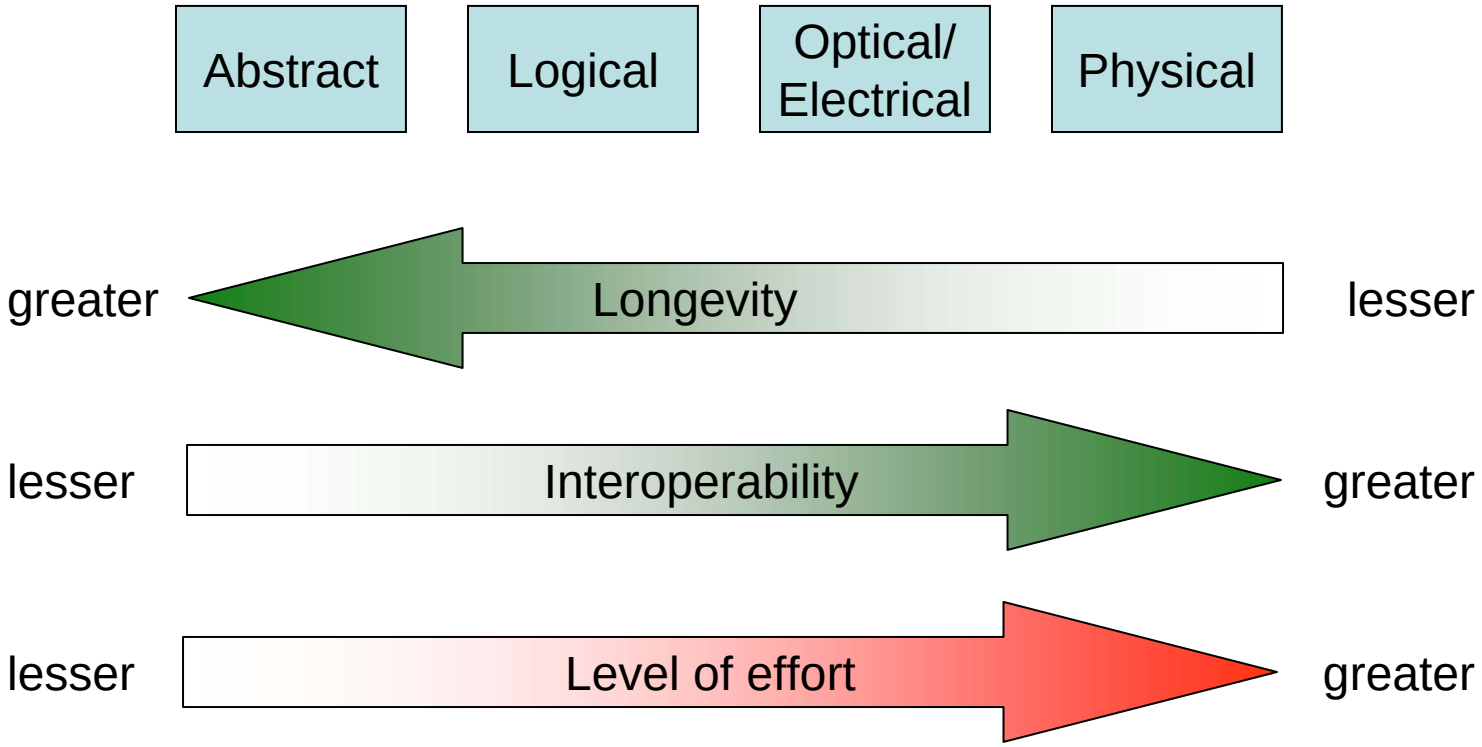
Rx lane	MDI Connector pin	Tx lane	MDI Connector pin
DL0<p>	S1	SL0<p>	S16
DL0<n>	S2	SL0<n>	S15
DL1<p>	S3	SL1<p>	S14
DL1<n>	S4	SL1<n>	S13
DL2<p>	S5	SL2<p>	S12
DL2<n>	S6	SL2<n>	S11
DL3<p>	S7	SL3<p>	S10
DL3<n>	S8	SL3<n>	S9
Signal Shield	G1	Signal Shield	G5
Signal Shield	G2	Signal Shield	G6
Signal Shield	G3	Signal Shield	G7
Signal Shield	G4	Signal Shield	G8
—	—	Link Shield	G9

Physical interfaces

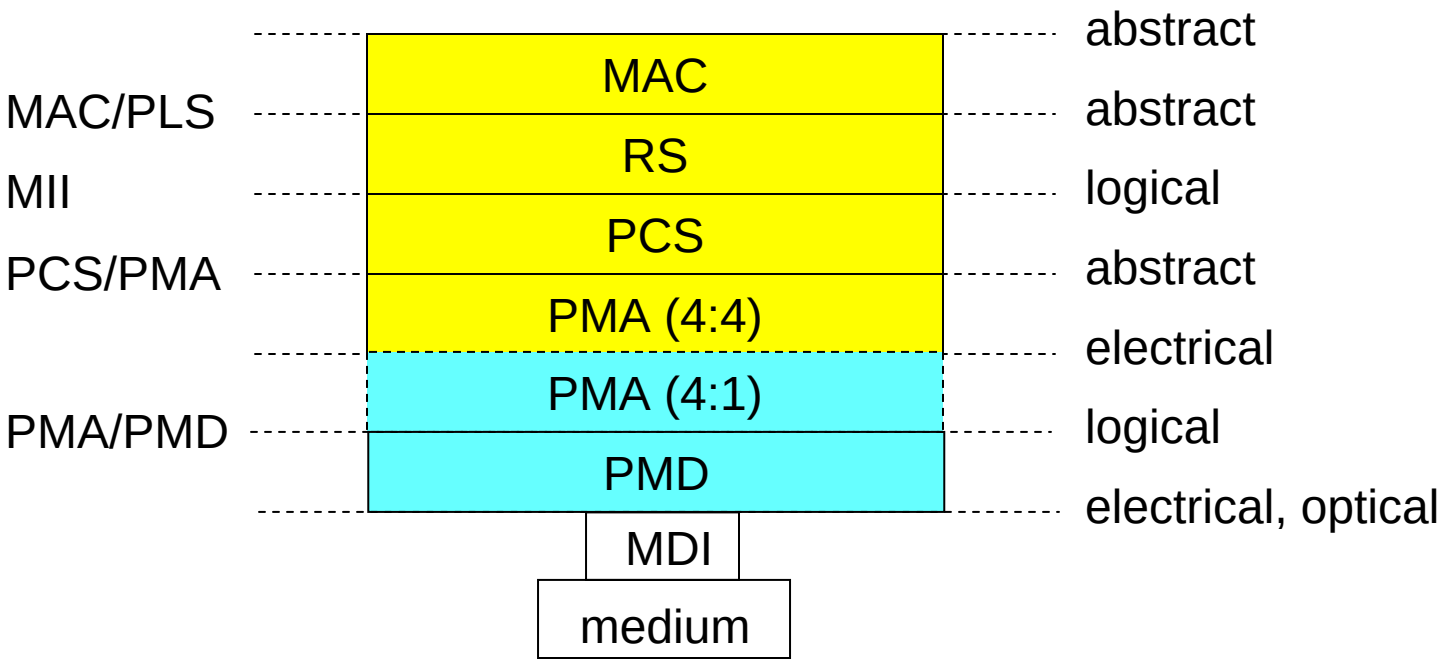
- Advantages
  - most rigorous
  - highest degree of interoperability
  - free food!
- Disadvantages
  - connector wars!

Proposal for 40G and 100G interface classes

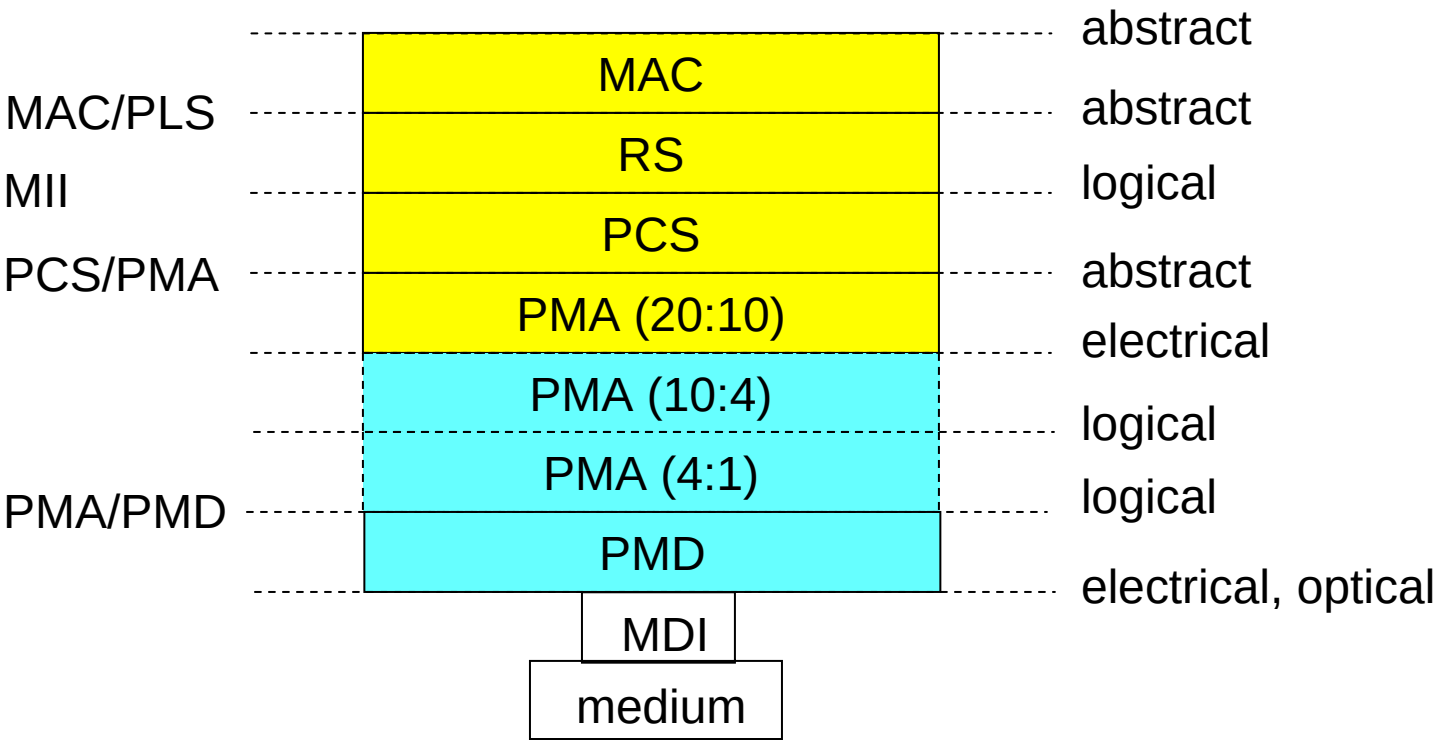
Comparison


Abstract
Logical
Optical/ Electrical
Physical
greater
Longevity
lesser
lesser
Interoperability
greater
lesser
Level of effort
greater

40 G sub-layers & interfaces



100 G sub-layers & interfaces



Summary

- There are several different classes of interfaces employed in IEEE 802.3
  - Abstract, Logical, Electrical, Optical, Physical
- Each has advantages and disadvantages
  - Longevity, interoperability, level of effort
- We should strive to minimize the number of interfaces, and strive to obtain the most benefit from the effort