40/100G Architecture and Interfaces proposal

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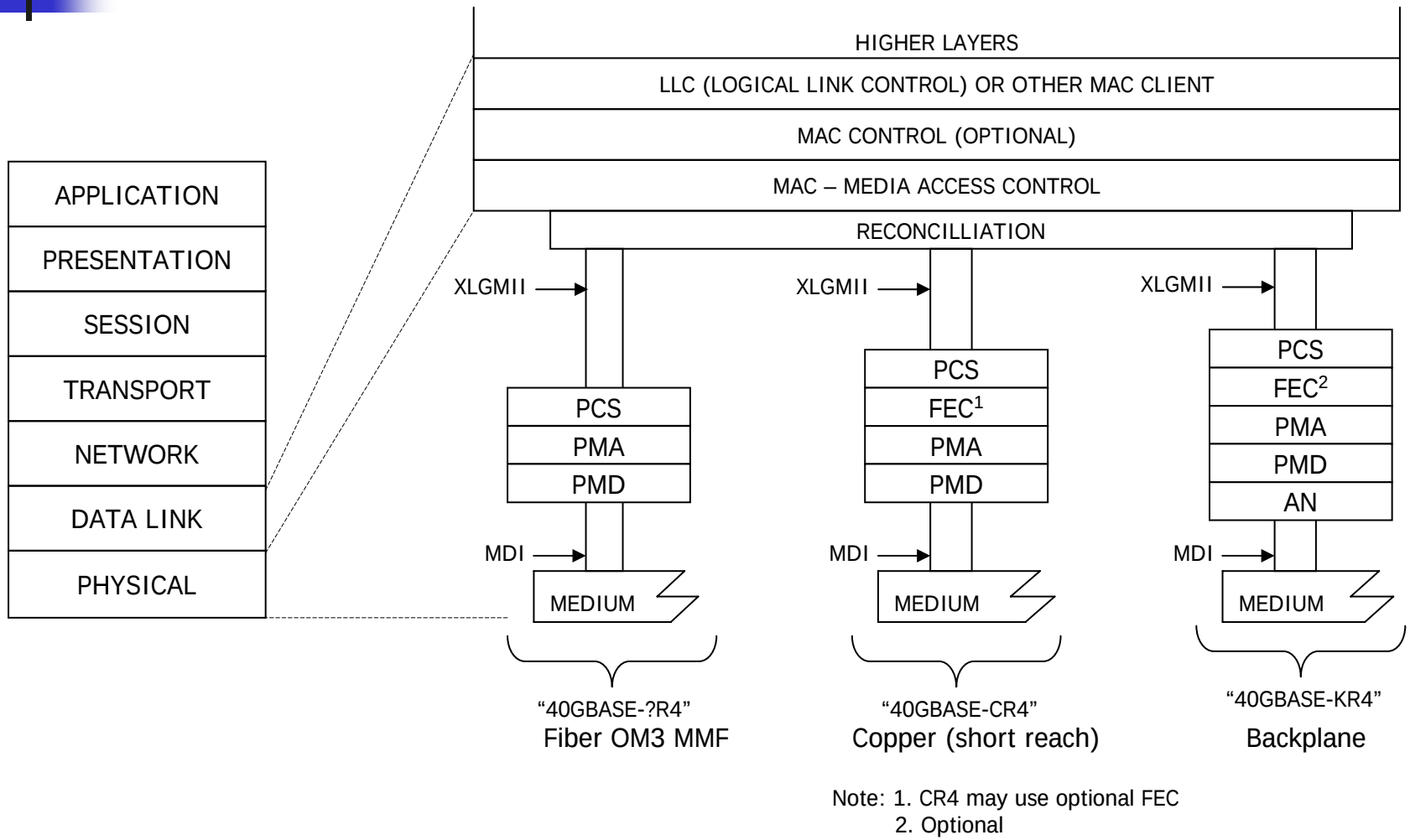
Overview

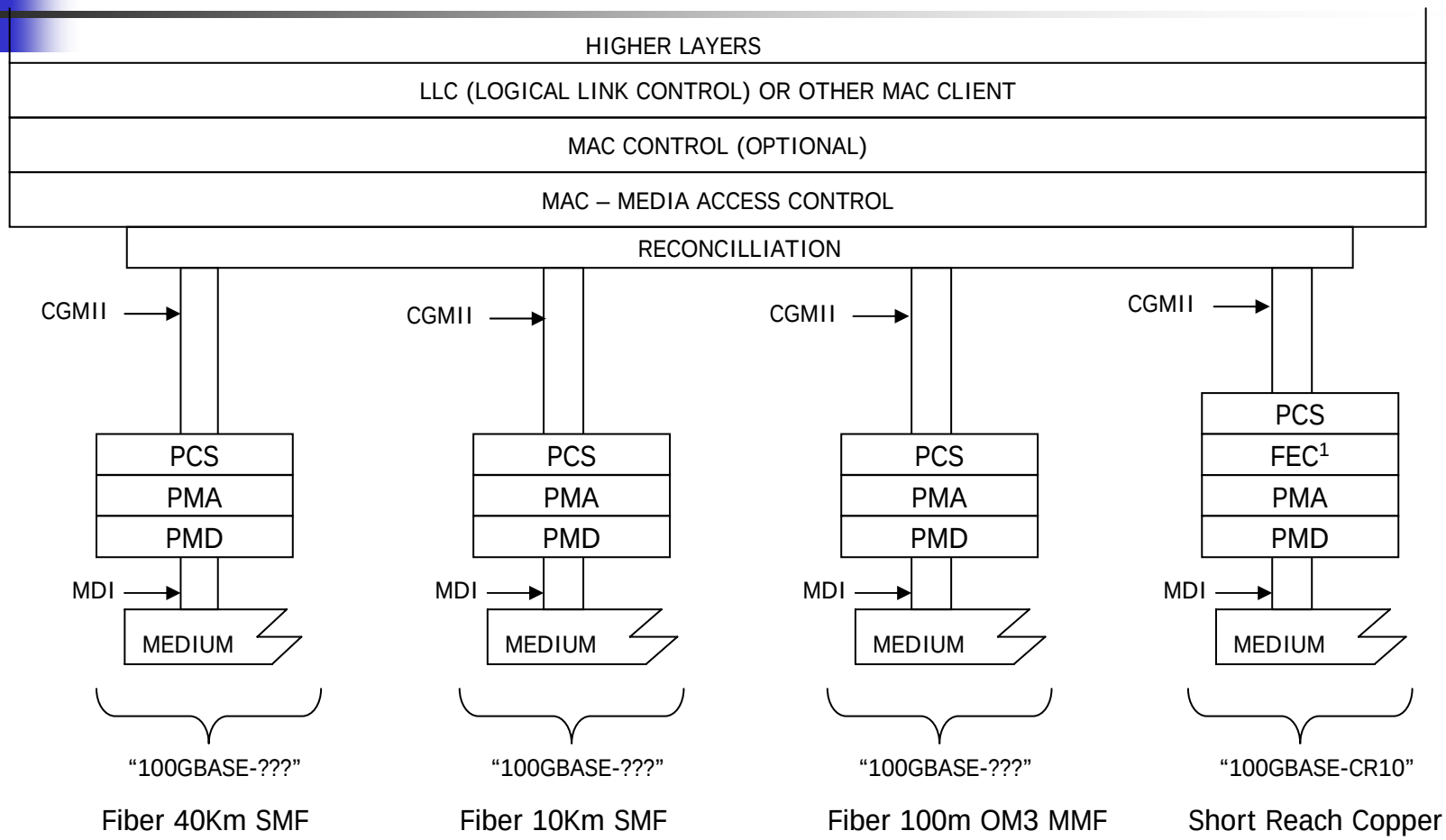
- Proposed layer diagrams for 40Gb/s and 100Gb/s
  - Additional references: ganga_01_1107, ganga_01_0108
- Proposed architectures
  - See frazier_01_0308.pdf for interface definitions
- Possible implementation examples
- Summary

Proposed 40GbE layer model



Note: 1. CR4 may use optional FEC
2. Optional

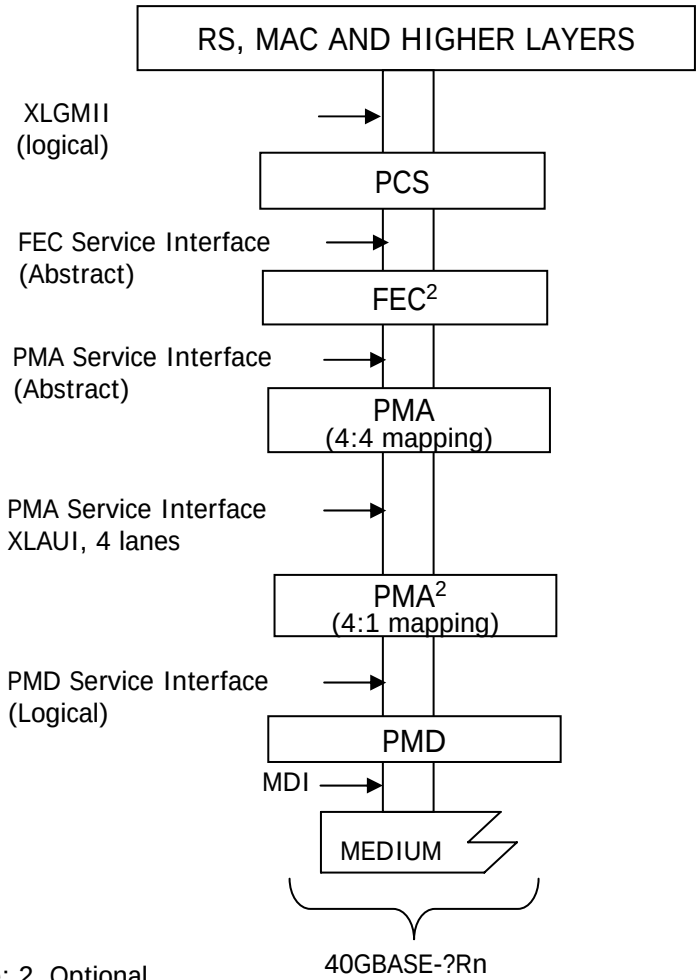
Proposed 100GbE layer model



Note: 1. CR10 may use optional FEC

Proposed 40GbE architecture

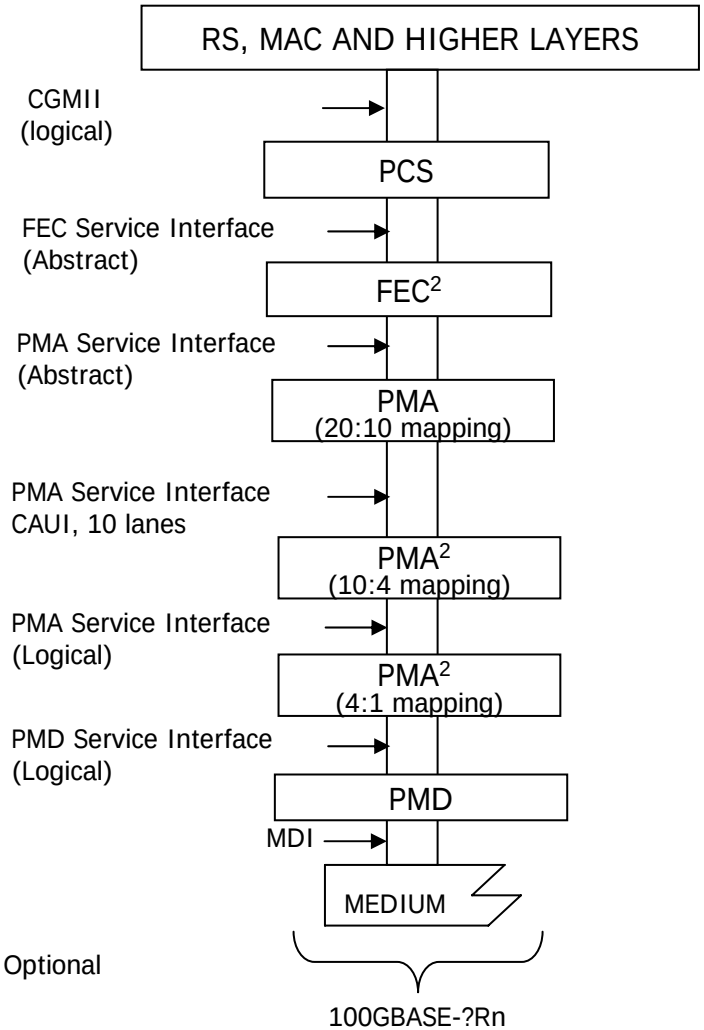
- XLGMII (intra-chip)
  - Logical, define data/control, clock, no electrical specification
- PCS
  - 64B/66B encoding
  - Lane distribution and alignment
- XLAUI (chip-to-chip)
  - n lane x 10 GBaud electrical interface
  - 4 lanes, short reach
- FEC service interface
  - Abstract, can map to XLAUI electrical interface
- PMA Service interface
  - Logical n lanes, maps to XLAUI electrical interface
- PMD Service interface
  - Logical, can map to XLAUI electrical interface



Note: 2. Optional

Proposed 100GbE architecture

- CGMII (intra-chip)
  - Logical, define data/control, clock, no electrical specification
- PCS
  - 64B/66B encoding
  - Lane distribution and alignment
- CAUI (chip-to-chip)
  - n lane x 10Gbaud electrical interface
  - 10 lanes, short reach
- FEC service interface
  - Abstract, can map to CAUI electrical interface
- PMA Service interface
  - Logical n lanes, maps to CAUI electrical interface
- PMD Service interface
  - Logical, can map to CAUI electrical interface



Note: 2. Optional

Interface description (1)

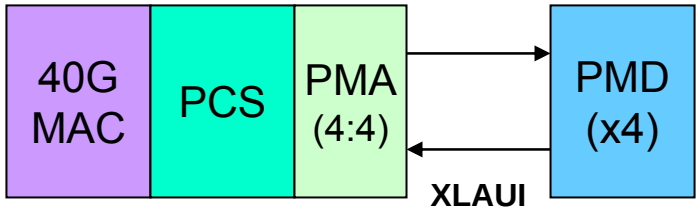
- XLGMII (Forty Gigabit MII) or CGMII (100 Gigabit MII) – PCS interface
  - Interface between MAC and PHY layers needed for intra-chip connectivity
  - Need for Compatibility interface
    - Multiple vendors develop IP blocks for system on chip implementations
    - Provides a point of interoperability for multi vendor implementations
  - Logical definition, data width, control, clock frequency, no electrical specification
  - XLGMII and CGMII can have same logical behavior, different data/control width and/or clock frequency
- XLAUI or CAUI interface (Chip-to-Chip)
  - n lane x 10Gbaud electrical interface
  - Provides a point of interoperability for multi vendor implementations
    - Similar to XAUI, for 10GbE, which is widely used as MAC - PHY interface
  - Low pin count, low power interface, for example PHYs, Switches, LAN controllers
  - Electrical definition, n lane x 10 Gbaud differential signaling
    - Short reach channel: e.g. around 10 inches with 1 pair of connector
    - Lane width: 4 lane for 40G, and 10 lane for 100G;
  - Same electrical definition can be optionally used with multiple Service interfaces (e.g. PMA, FEC, PMD)

Interface description (2)

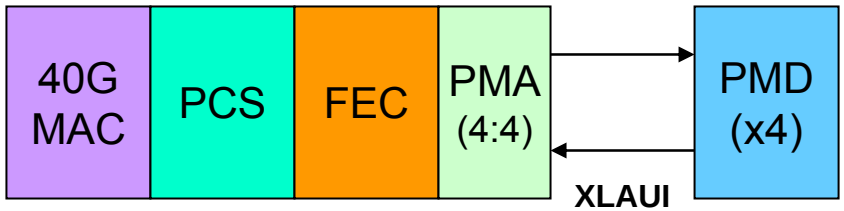
- FEC Service interface
  - Interface between PCS and optional FEC sub-layer
    - Used for backplane PHYs, may be used with other PHY types (e.g. copper cable assy)
  - FEC Service interface is similar to PMA interface
  - Possible implementations: FEC integrated with MAC/PCS, or with PMA/PMD device
  - Abstract definition, with an option to map to XLAUI/CAUI electrical interface
- PMA Service interface
  - Interface between PMA and PCS
  - Logical definition with n Lanes, maps to XLAUI/CAUI electrical interface
- PMD Service interface
  - Interface between PMD and PMA
  - PMA and PMD may be implemented together in the same device
  - Logical definition, with an option to map to XLAUI/CAUI electrical interface

Possible 40GbE implementations

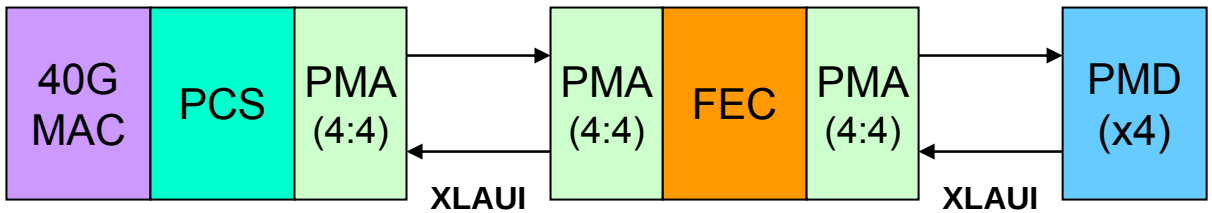
40GBASE-R4
(4 λ or lanes)



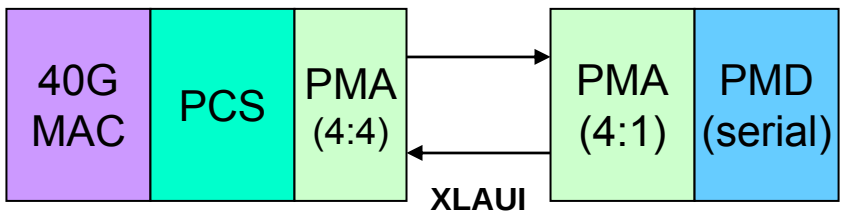
40GBASE-R4
(w/ FEC)



40GBASE-R4
(w/ FEC chip)

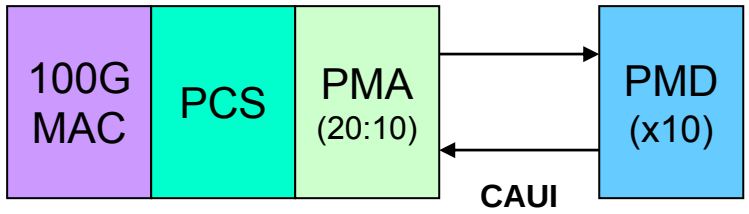


40GBASE-R
(serial)

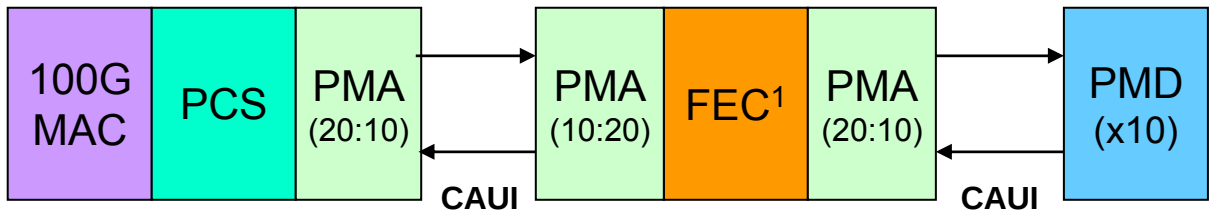


Possible 100GbE implementations

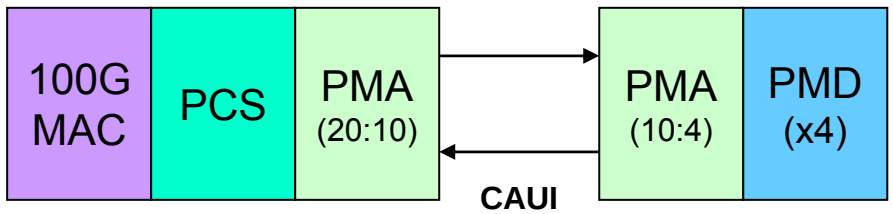
100GBASE-R10
(10 λ or lanes)



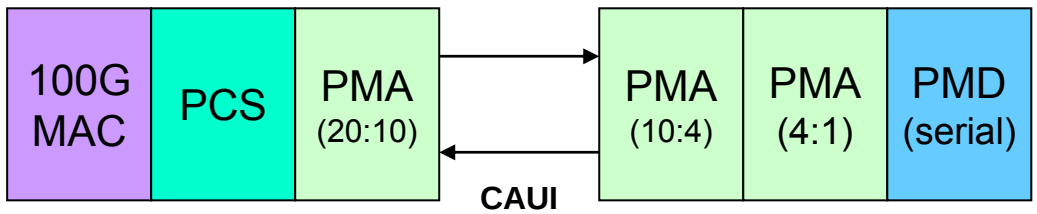
100GBASE-R10
(w/ FEC chip)



100GBASE-R4
(4 λ or lanes)



100GBASE-R
(serial)



Note: 1. CR10 may use optional FEC

Summary

- Proposed 40/100G high level architecture
  - Provides a common framework for both 40G and 100G
  - Supports project objectives
- Provide an interface for multi-vendor interoperability
  - XLGMII/CGMII for intra-chip connectivity
  - XLAUI/CAUI for inter-chip connectivity