100GE and 40GE skew

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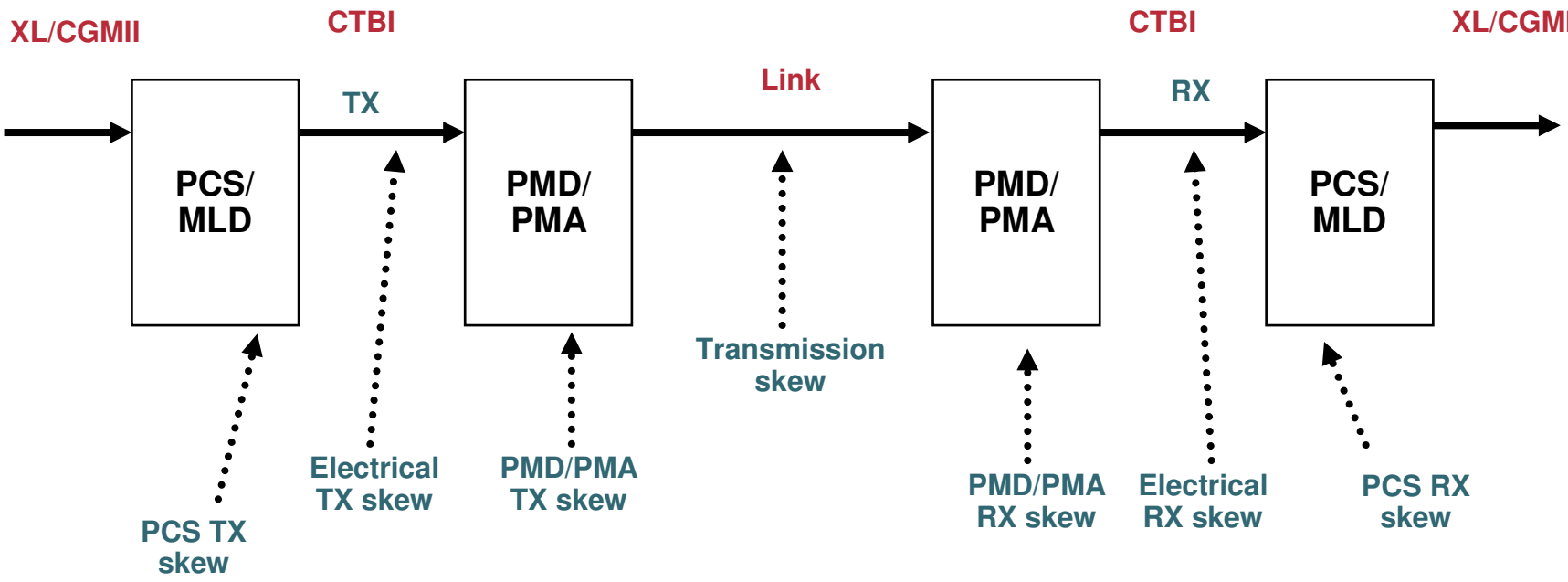
System architecture (one direction shown)



Total Skew introduced

- **Skew considered in this presentation is static lane-to-lane skew, not P-N skew in a differential pair – no dynamic skew analyzed here**

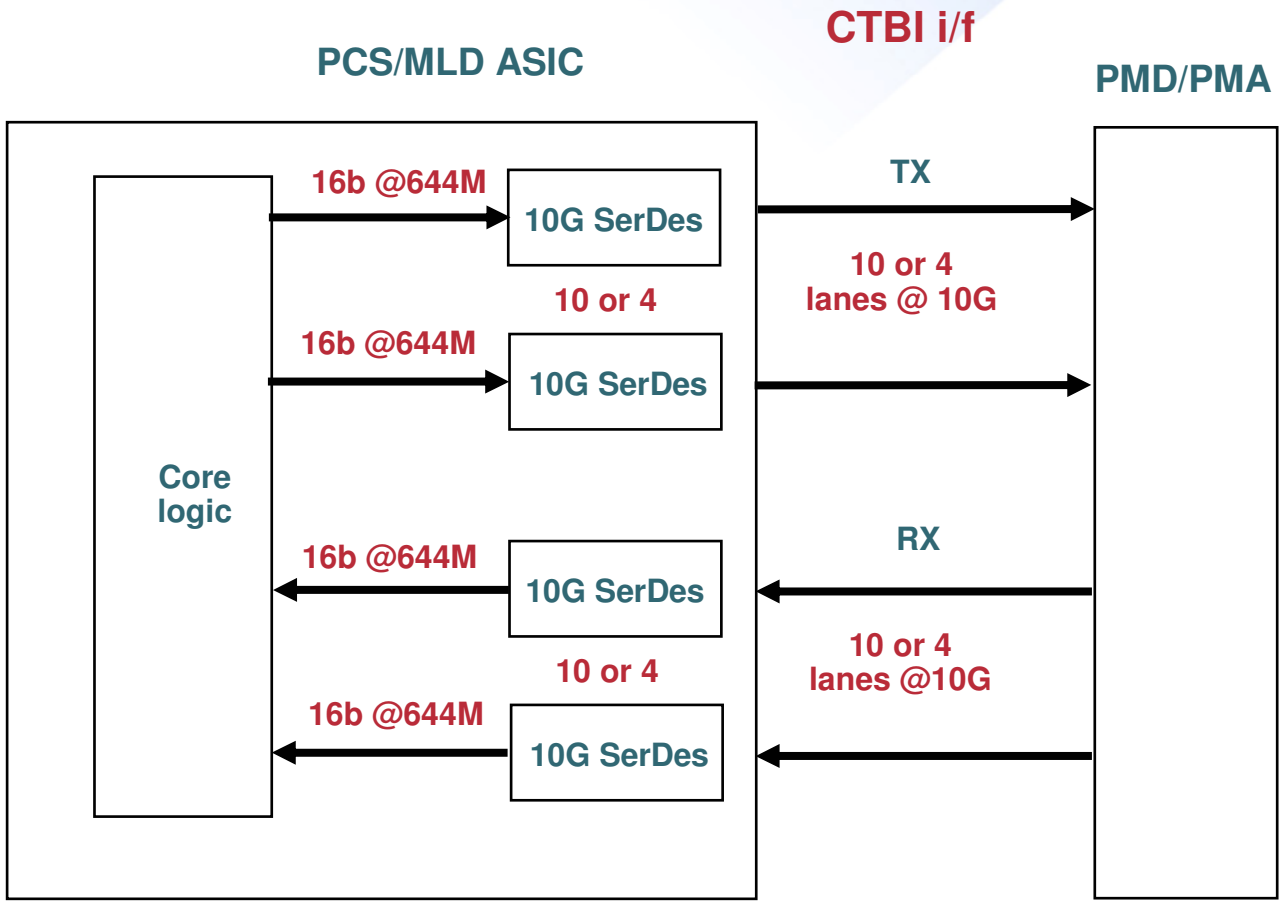
- **We need to add up all of the skew to see how much total skew must be compensated for at the receiver**

- **Skew contributors are PCS/MLD, Electrical interface, PMD/PMA and transmission skew, can be broken further into:**
  - **TX PCS/MLD**
  - **TX Electrical (PCS Layer to PMA)**
  - **TX PMD/PMA**
  - **Transmission (medium)**
  - **RX PMD/PMA**
  - **RX Electrical (PMA to PCS Layer)**
  - **RX PCS/MLD**

PCS/MLD skew (TX and RX)

- **Skew could be introduced due to 10G Tx SerDes FIFOs not aligned, difference in FIFO fill translates into skew**
- **Basically, each SerDes has its own FIFO, all 10 (4) FIFOs should be aligned if possible to reduce skew – essentially "reset" the pointers within some tolerance**
- **Another contributor can be the high speed serializer stage in the SerDes**
- **2 case studies: ASIC or FPGA solution**

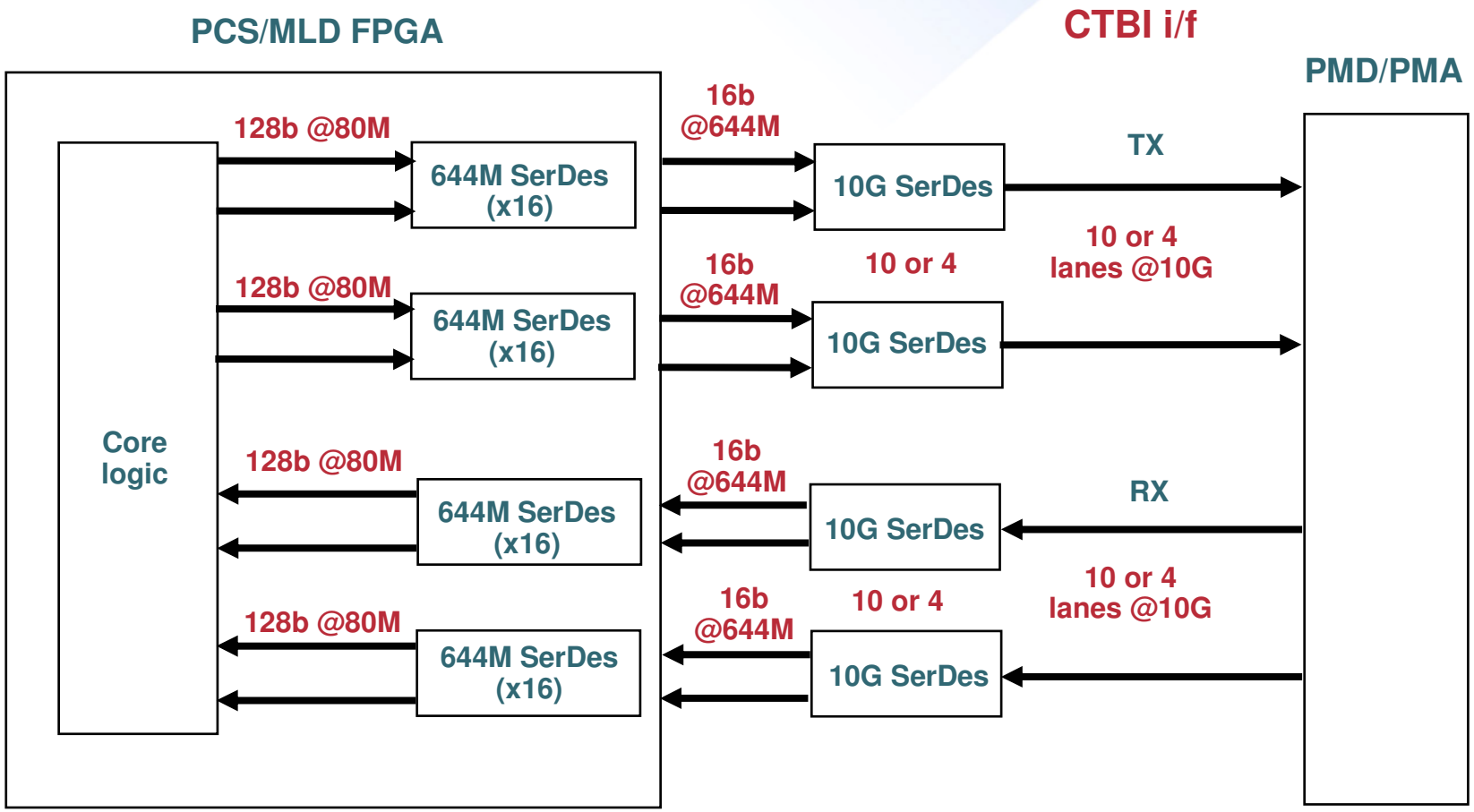
PCS/MLD skew – ASIC case



PCS/MLD skew – ASIC case (cont.)

- **ASIC skew**
  - **should be small in Tx, since the ASICs can integrate 10G SerDes technology. This is assuming all 10 or 4 SerDes in same chip**
  - **This should potentially introduce only a small amount of skew quantified by the uncertainty on the FIFO reset mechanism and serializer-related skew**
  - **There should be no skew in the stages feeding the Tx FIFOs**
  - **Total amount of TX skew should be in the order of 16-18 UI for reset/serializer uncertainty and another 200ps for skew induced from driver/package, total of upto 20 UI**
  - **Numbers for RX side are also in the order of upto 20 UI**

PCS/MLD skew – FPGA case



PCS/MLD skew – FPGA case

- **FPGA solution with external 10G SerDes devices**
  - **Since current FPGA technology does not support 10G links (SerDes), board level solutions need to connect a MAC/PCS FPGA to 10 (or 4) 10G SerDes devices**
  - **Assuming a 16-bit i/f between FPGA and external 10G SerDes: still need internal FPGA SerDes to convert from a wide databus to serial 644 Mb/s (16 of them per 10G) – a 4-bit i/f is an alternative option**
  - **Stages feeding the internal SerDes could introduce upto 128 UI of skew, depending on datapath size choice – need confirmation from FPGA vendors**
  - **Number of pins and internal FPGA SerDes required might prohibit single-FPGA device implementation, but only possible option is partitioning to Tx and Rx, and analysis still holds**

PCS/MLD skew (TX and RX), cont. - FPGA

- **FPGA solution with external 10G SerDes devices (cont.)**
  - **External SerDes devices are difficult to synchronize, so skew can be introduced by different fill levels in their FIFOs, also in the order of a few tens of bits (depending on FIFO size) – with a 16-bit i/f could have a skew of Nx16 UI, this applies to both Tx and Rx**
  - **Do not expect electrical skew in a 16-bit clocked i/f @644M between FPGA and external SerDes**

CTBI Electrical skew (TX and RX)

– Calculation of skew requires modeling using controlled impedance traces on standard FR4 low-cost PCBs

– A good starting point would be the XFI interface for a chip to chip interconnect

- current XFI i/f allows for 9.6dB of loss @5.5GHz
- allows for a range from 1” to 8-10” typically

CTBI Electrical skew (TX and RX) (cont.)

- If we assume a 10” range then the upper bound of skew is 10”, which translates into 10*220ps/in = 2.2ns, so 4.4 ns for TX and RX – Could never happen ☺
- A more realistic scenario would be 1-2” of board skew, 2” translates to 0.88 ns or 9 UI (@10Gb/s)
- Even 1” should be fine with good layout practices (4-5 UI)
- PCB designers could give more accurate skew data, depends on board size, number of layers etc

- Reference Point for Interconnect (XAUI)
- From 802.3ae (Table 47-4)
- 75ps per table (backup slide)x2 = 150ps

PMD/PMA skew (TX and RX), 4x25G

- **MLD supports bit muxing at the CTBI i/f as well as at the line side**
- **PMA is a simple bit MUX/DeMUX**
  - internal skew in the order of 2-4 UI (per chip, per direction), including analog and digital skew
- **PMA to PMD connection**
  - Traces should in any case be carefully laid out
  - Even ½" of electrical skew should be ok
  - In a 4x25G case, ½" translates to 3 UI (per direction)

Transmission skew

- **Dependent on PMD type**
- **For an optical solution, Nortel (P. Anslow) latest data shows a max skew @ 1300 nm of 1.7ns (44.5 UI) for transmission skew (4x25G case) – see next slide**
- **Copper TBD**

Transmission skew (4 x 25G)

- The "Fibre characteristics" spreadsheet gives a skew of:
  - 1.7 ns (44.5 UI) for 10 km CWDM (1271 nm)
  - 0.18 ns (4.7 UI) for 10 km DWDM (800 GHz spacing, 229.6 THz)
  - 0.72 ns (18.6 UI) for 40 km DWDM (800 GHz spacing, 229.6 THz)
- Also, need to account for the skew change (over the lifetime of product) of
  - 0.8 ns (19.7 UI) for 10 km CWDM
  - 43 ps (1.1 UI) for 10 km DWDM
  - 0.17 ns (4.4 UI) for 40 km DWDM

– Max is 1.7ns (44.5 UI) for transmission skew (4x25G)

Source: Pete Anslow, Nortel

Summary Table for static skew

Contributor	Static Skew (UI)
PCS/MLD TX	20 (ASIC) 128+N*16 ? (FPGA solution)
Electrical CTBI TX	9
PMA/PMD TX	7
Transmission	44.5 Optical (4x25G @1300nm) TBD Copper
PMA/PMD RX	7
Electrical CTBI RX	9
PCS/MLD RX	20 (ASIC) 128+N*16 ? (FPGA solution)
TOTAL	**116.5** (ASIC) **332.5 + 2N*16** (FPGA solution)

Comments/Proposals

- Assuming 10-12” for the max distance of a CTBI interface between chips, we propose a 2” board trace skew which results in 9 UI skew per direction

- When architectural decisions are reached, this will clarify all skew scenarios we need to evaluate (chicken and egg problem ? ☺)

Questions

- How should we define min deskew capability in the standard?
  - A. Based on MAX skew introduced by worst case scenarios in the Scope
    - **MAX_skew = Transmission + PCS/MLD + electrical + PMA/PMD skew**
  - B. Based on a MAX skew from case A + extra budget for future technology that might require more de-skew. This will more than cover the needs of what is in the scope
    - **MAX_skew + extra_budget**

Q & A

Thank you !

Backup slides

XAUI skew (from IEEE 802.3 Table 47-4) – for reference

	Loss (dB)[a]	Differential skew (ps_{p-p})	Total jitter (UI_{p-p})[c]	Deterministic jitter (UI_{p-p})[c]
Driver	0	15	0.35	0.17
Interconnect	7.5	60	0.20	0.20
Other[b]	4.5		0.10	0.10
Total	12.0	75	0.65	0.47

- [a] **Budgetary loss in height of eye opening**
- [b] **Includes such effects as crosstalk, noise, and interaction between jitter and eye height**
- [c] **Jitter specifications include all but 10^{-12} of the jitter population**

Fiber characteristics tool

- Fiber characteristics tool (spreadsheet) officially adopted by IEEE and used by P. Anslow to calculate transmission skew is in:

http://www.ieee802.org/3/ba/public/tools/Fibre_characteristics_V_3_0.xls