Technical Feasibility of 100G/40G MLD

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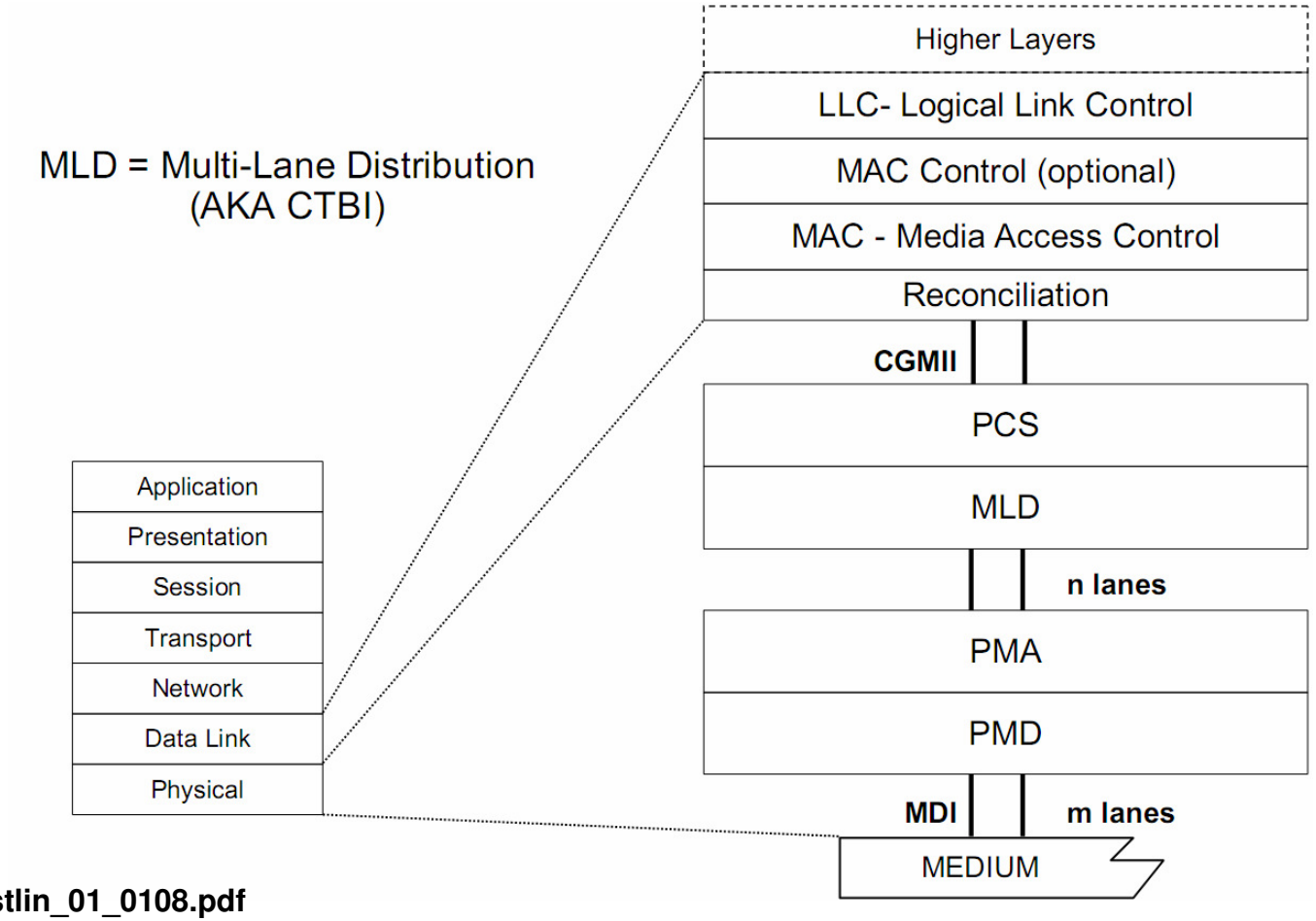
Outline

- Presentation is focused on the implementation of the digital logic

- Agenda:
  - MLD overview
  - 100G implementation and discussion
  - 40G implementation and discussion
  - Conclusions

MLD Overview



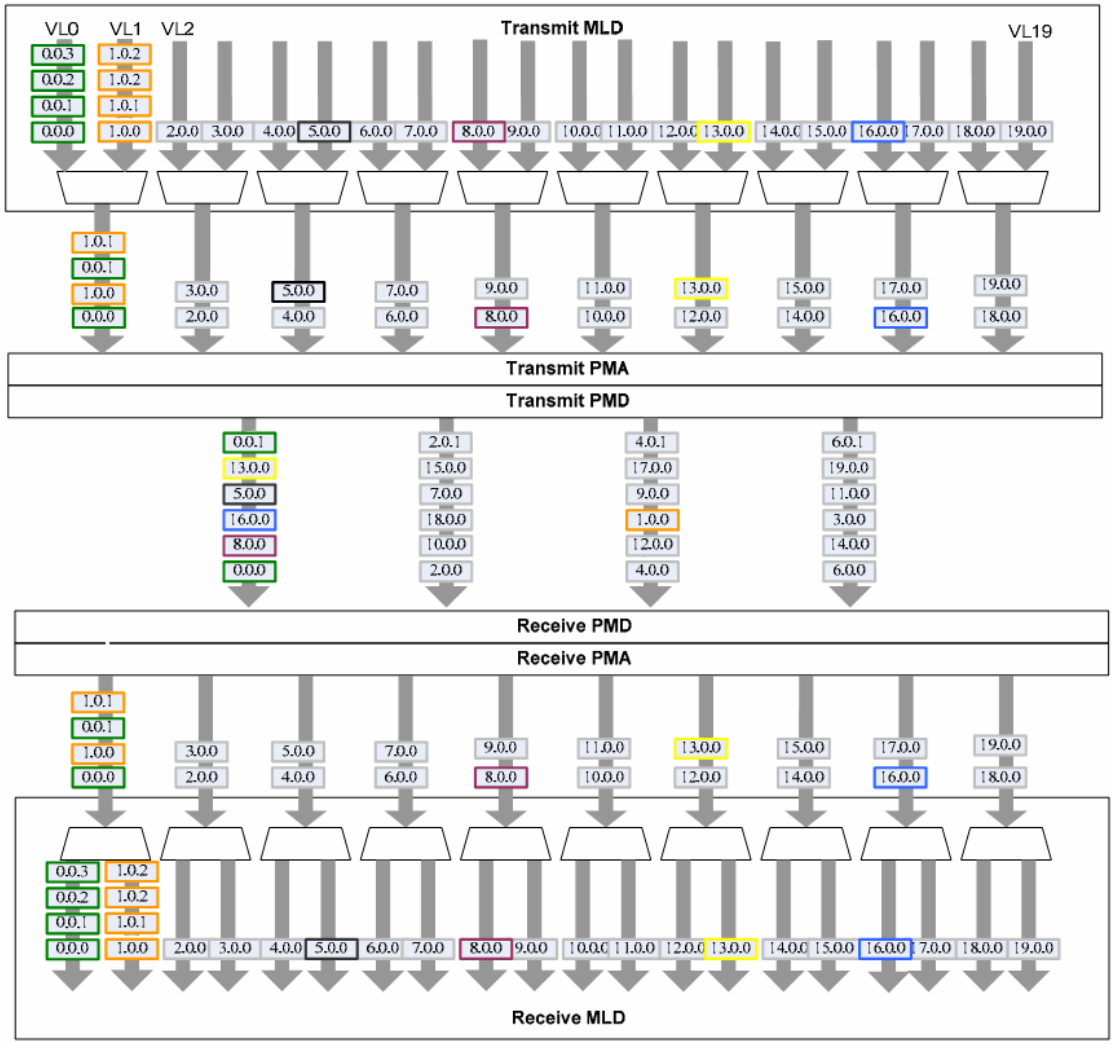
From gustlin_01_0108.pdf

MLD Operation (100G)

- Transmit path:
  - Receive 66B blocks from PCS
  - Stripe the blocks over 20 Virtual Lanes (VLs)
    - Simple round-robin mechanism
  - Add periodic alignment blocks
  - Mux 20 VLs down to "n" electrical PMA lanes
    - Bit muxing

- Receive path:
  - Demux data from "n" electrical lanes to 20 VLs
  - Rebuild 66B from serial stream for each VL
  - Deskew and align the VLs
  - Reorder VLs to compensate for different "n" and "m" ratios

Bit Flow Through MLD

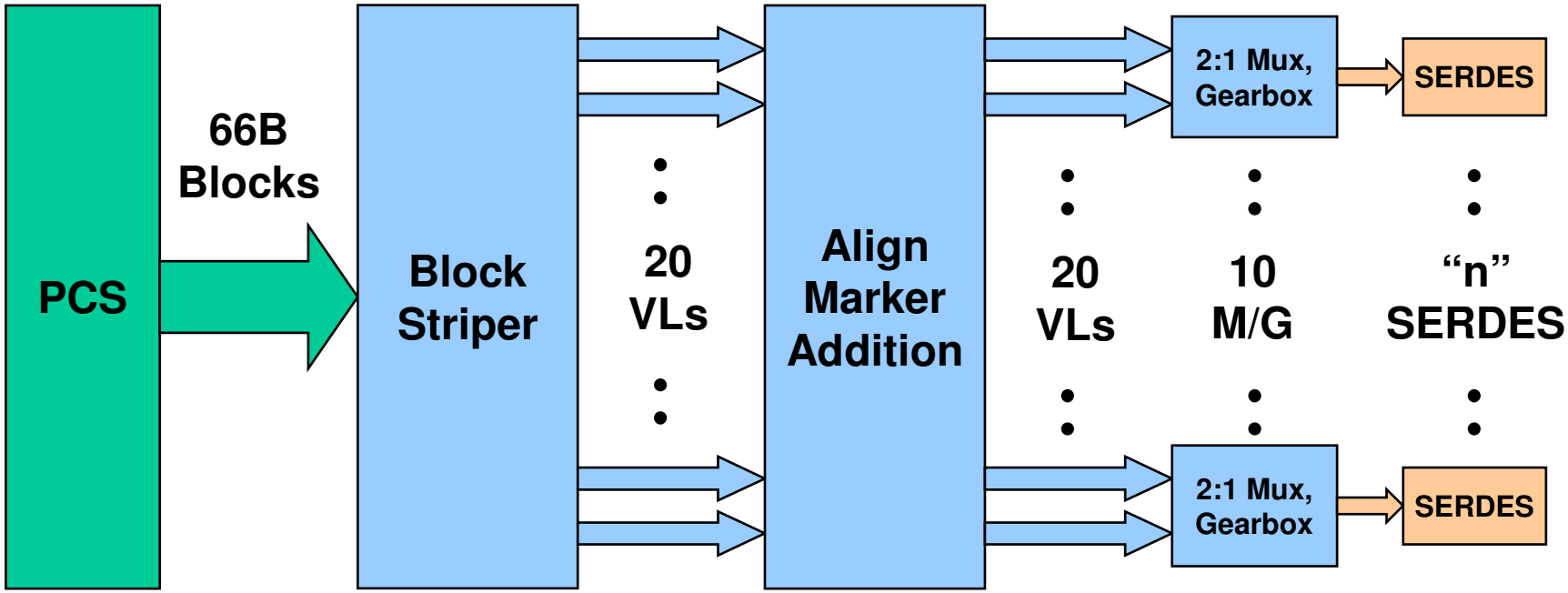


VLs are re-ordered as they go through the PMD and medium

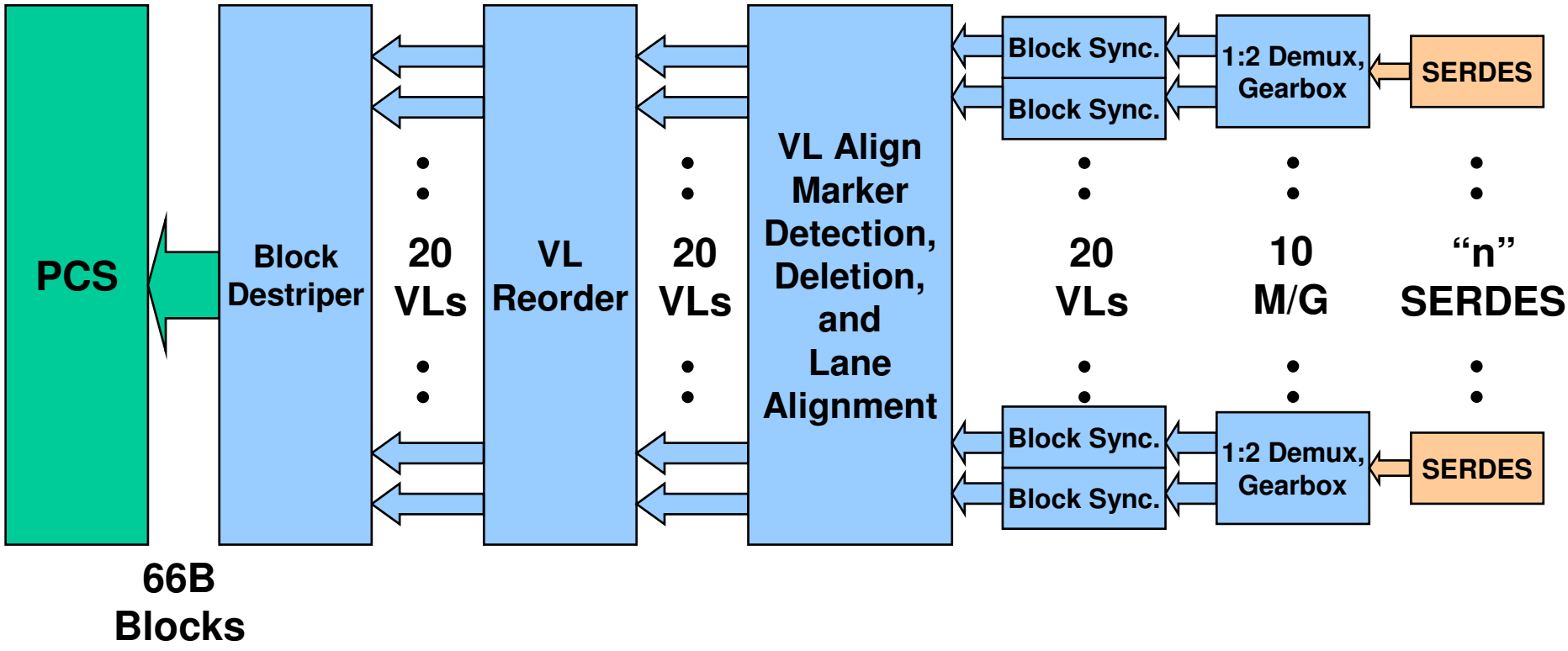
From gustlin_01_0108.pdf

100G Transmit Path

- Simple!
- Note that VL identifier is part of the align marker



100G Receive Path



Receive VL Alignment Discussion

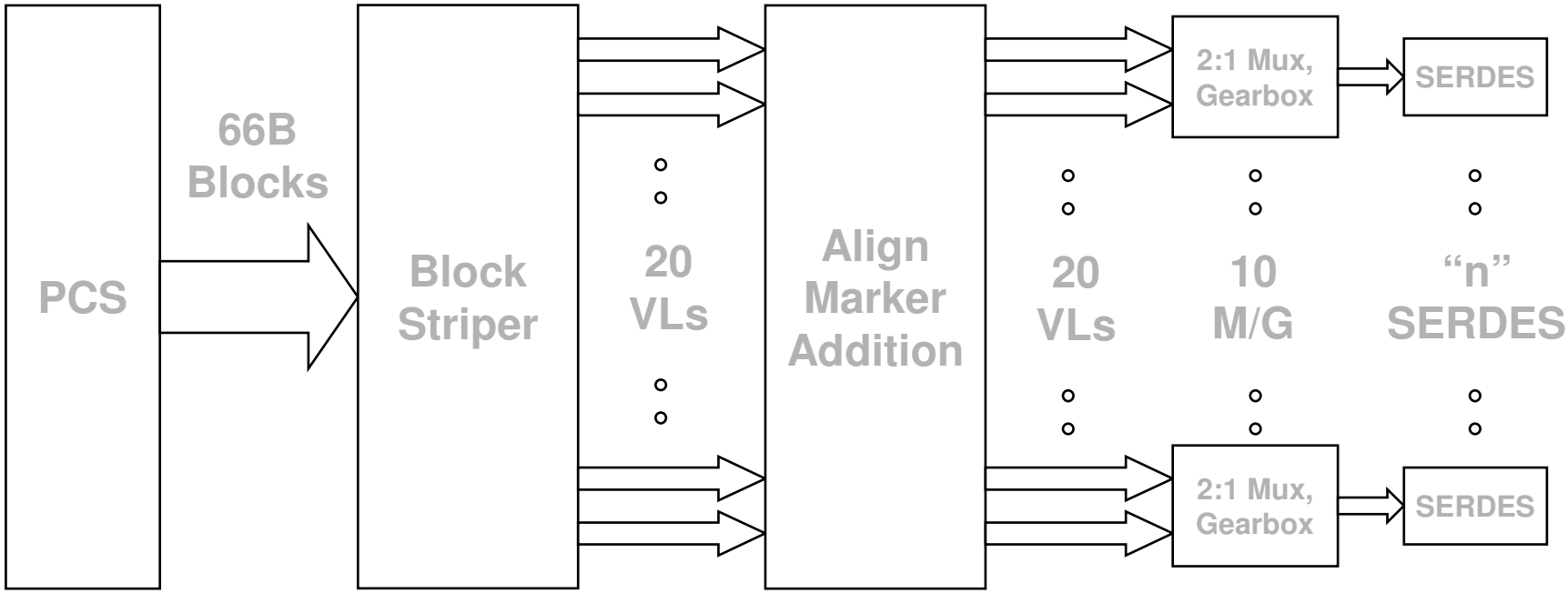
- Alignment control logic is fairly straight forward:
  - Each VL has a FIFO
  - Look for VL align markers and keep track of their position going into each FIFO
  - Adjust each FIFO's read pointer based on the position of it's align maker -> all read data is aligned

- Depth of FIFO determines skew limit:
  - One 64 bit word: 64 bit deskew (a pipeline stage)
  - Two 64 bit words: 128 bit deskew
  - Etc.

Logic complexity is low; Deskew capability can be easily increased or decreased

Implementation Results
Transmit Path

- Implemented in Xilinx Virtex™ 5 FPGA

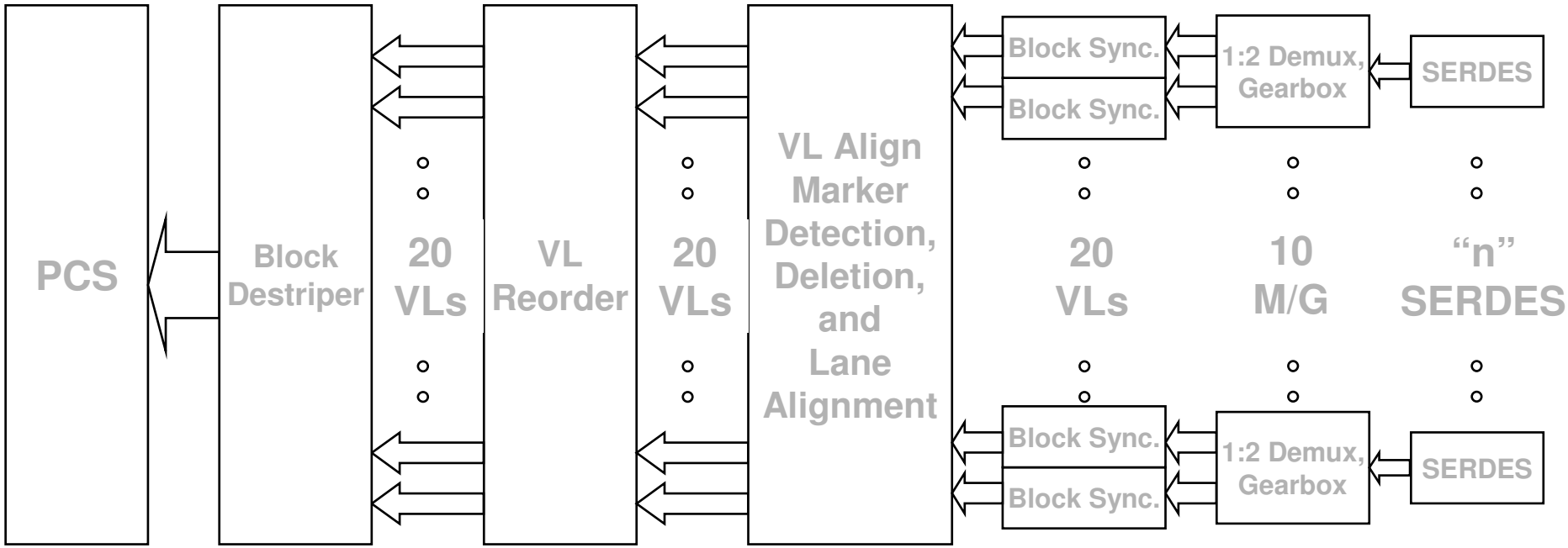


2800 LUTS
1560 Registers
~33.6K ASIC gates

500 LUTS
929 Registers
~6K ASIC gates

3600 LUTS (total)
1280 Registers
~43.2K ASIC gates

Implementation Results
Receive Path



1050 LUTS
1980 Registers
~12.6K ASIC gates

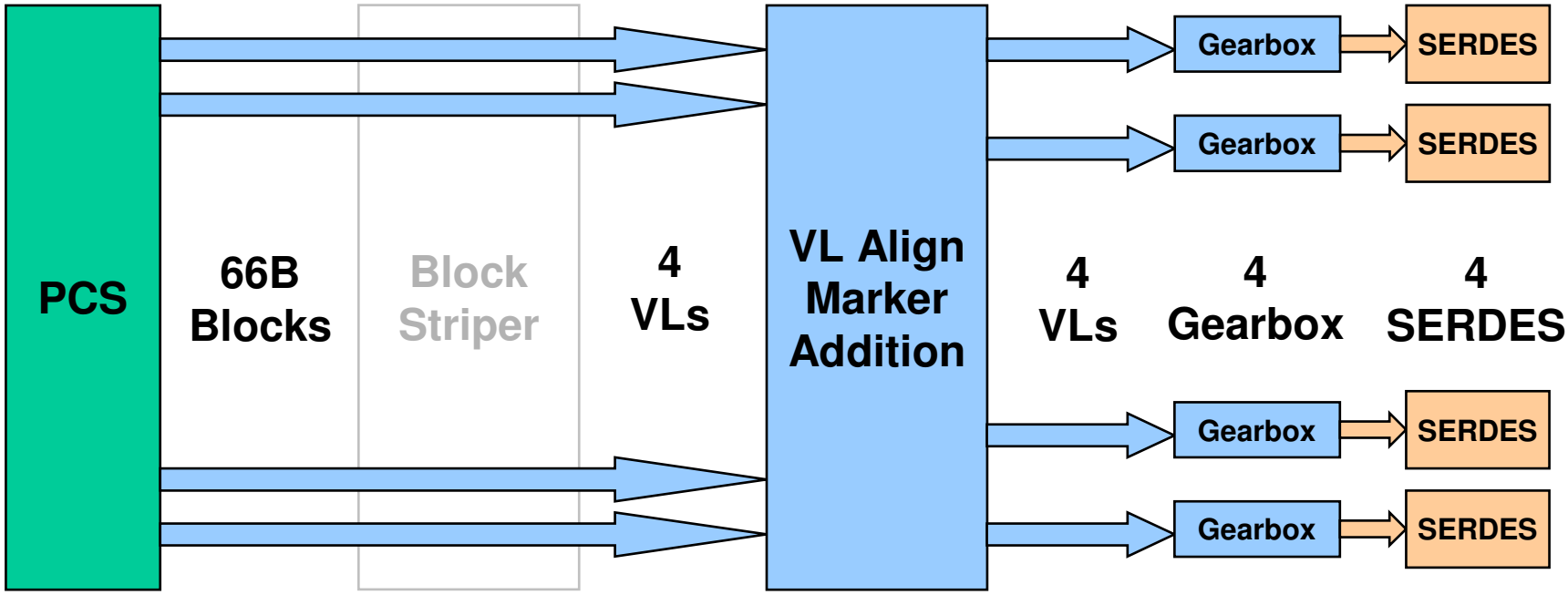
8500 LUTS
720 Registers
~102K ASIC gates

2050 LUTS
3100 Registers
+ FIFO as needed
~24.6K ASIC gates

6900 LUTS (total)
2060 Registers
~82.8K ASIC gates

40G Transmit Path
m=n=4

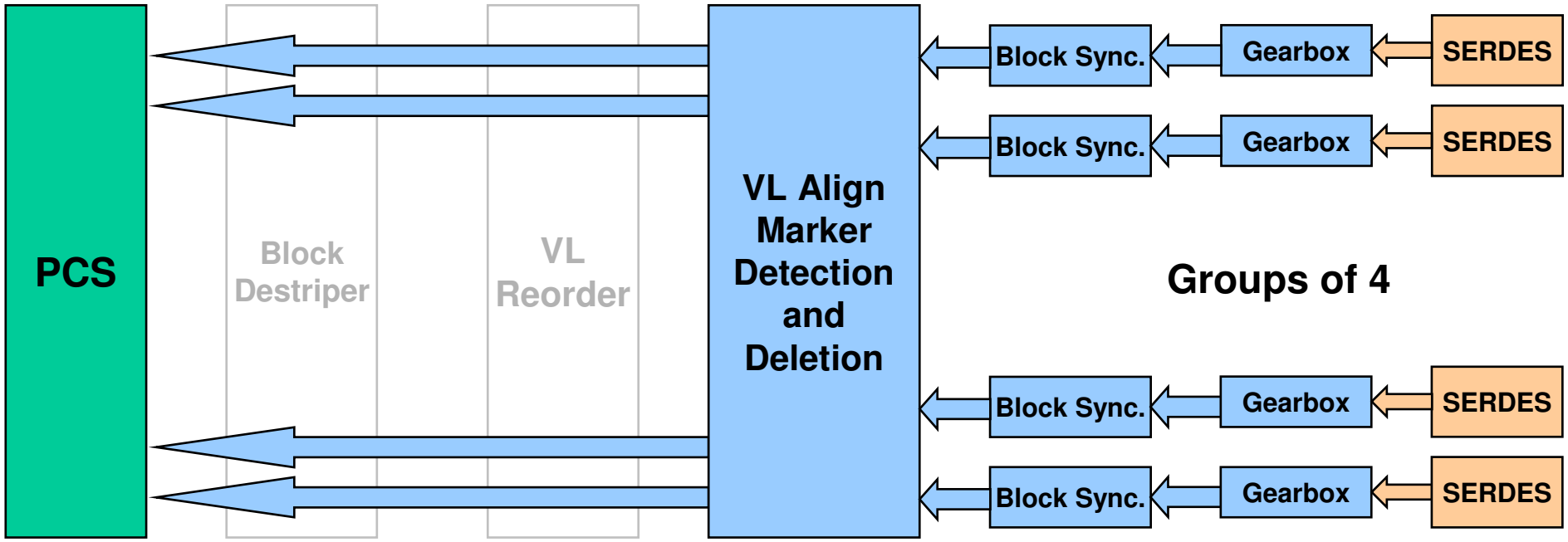
- Even simpler



264 LUTS
276 Registers
~3.2K ASIC gates

720 LUTS (total)
256 Registers
~8.6K ASIC gates

40G Receive Path
m=n=4



66B Blocks

145 LUTS
549 Registers
~1.7K ASIC gates
(includes storage for 128 bit deskew)

1380 LUTS (total)
412 Registers
~16.6K ASIC gates

SARANCE TECHNOLOGIES

VL Align Marker Discussion

- There are no VLs, so VL Align Markers are only used to align the lanes
- Do we need align markers, or can we use the sync bits to align?
  - Using sync bits to align limits the skew to one word (i.e. 32 bits) between all lanes
  - FPGAs have 32-bit buses coming out of SERDES receivers. This may add 32 bits of skew due to serial-to-parallel conversion and another 32 bits of skew due to elastic buffers. Total skew inside the SERDES receiver may be up to 64 bits.
- Cost of using sync bits to align (estimated):
  - Transmit path: no logic is needed
  - Receive path: 400 LUTs and 528 Registers
- Cost of having the VL Align Markers (actual):
  - Transmit path: 264 LUTs and 276 Registers
  - Receive path: 145 LUTs and 549 Registers for 128 bit deskew limit
  - Total logic: 409 LUTs and 825 Registers for 128 bit deskew limit

Additional cost of having VL Align Markers is very minimal and pretty much irrelevant

Do VL Align Markers Add Latency?

- They do:
  - Transmit path: 1 cycle of latency to add VL Align Markers
  - Receive path:
    - 1 cycle of latency for 64 bit deskew
    - 2 cycles of latency for 128 bit deskew
    - Etc.
    - This latency is needed to align lanes and delete VL Align Makers

- Clock cycle for 10G SERDES is most likely 32bits/10Gbps = 3.2ns

Added latency due to MLD is only 6.4ns

Conclusions

- MLD characteristics
  - Logic complexity is low
  - Cost (in terms of area) is low
  - Added latency is small
  - Benefits are high:
    - VL concept can support all reasonable “n”/”m” ratios
    - VL Alignment Markers can deskew any amount of skew without any extra logic complexity and with minimum additional storage
- MLD is possible in today’s FPGA technologies