40/100G CEI Feasibility

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PhyCore Technology

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Outline

1. SNR and Noise Margin
2. Measured Data of Channel & Package Crosstalk [1],[2]
3. Worst Case Scenario
4. Signaling Selection by Salz SNR and Noise Margin
5. Achievable Noise Margin with IC Implementation
6. Summary

[1] http://grouper.ieee.org/groups/802/3/ba/public/tools/ghiaisi_c1_1207.pdf

[2] http://grouper.ieee.org/groups/802/3/ba/public/tools/na_01_1207.pdf

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SNR vs. EYE-Opening

Question: “Is BER OK when EYE is open?”

The answer depends on system impairments.

YES: Chip to chip I/O environment in which high SNR is guaranteed and deterministic ISI is much bigger impairment than random noise source.
→ EYE / LINK Budget

NO: When random (Gaussian) noise sources such as crosstalk, IC electronics noise, and random jitter are major impairments.
(Backplane, Long reach CEI, and Cable applications)
→ SNR / Noise Margin

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Noise Margin

The best method to characterize PHY QOS is "Noise Margin"

"Noise Margin" Definition

Noise Margin = [Achievable SNR] – $SNR_{required}$

$SNR_{required}$ is 17dB for 2PAM-NRZ

24dB for 4PAM (BER = 10-12).**

Target Margin: 3 ~ 6dB

"6dB in theory and 3dB with worst case conditions w IC implementation"

Achievable SNR is determined by Channel, Noise environment, Jitter, and IC Implementation.

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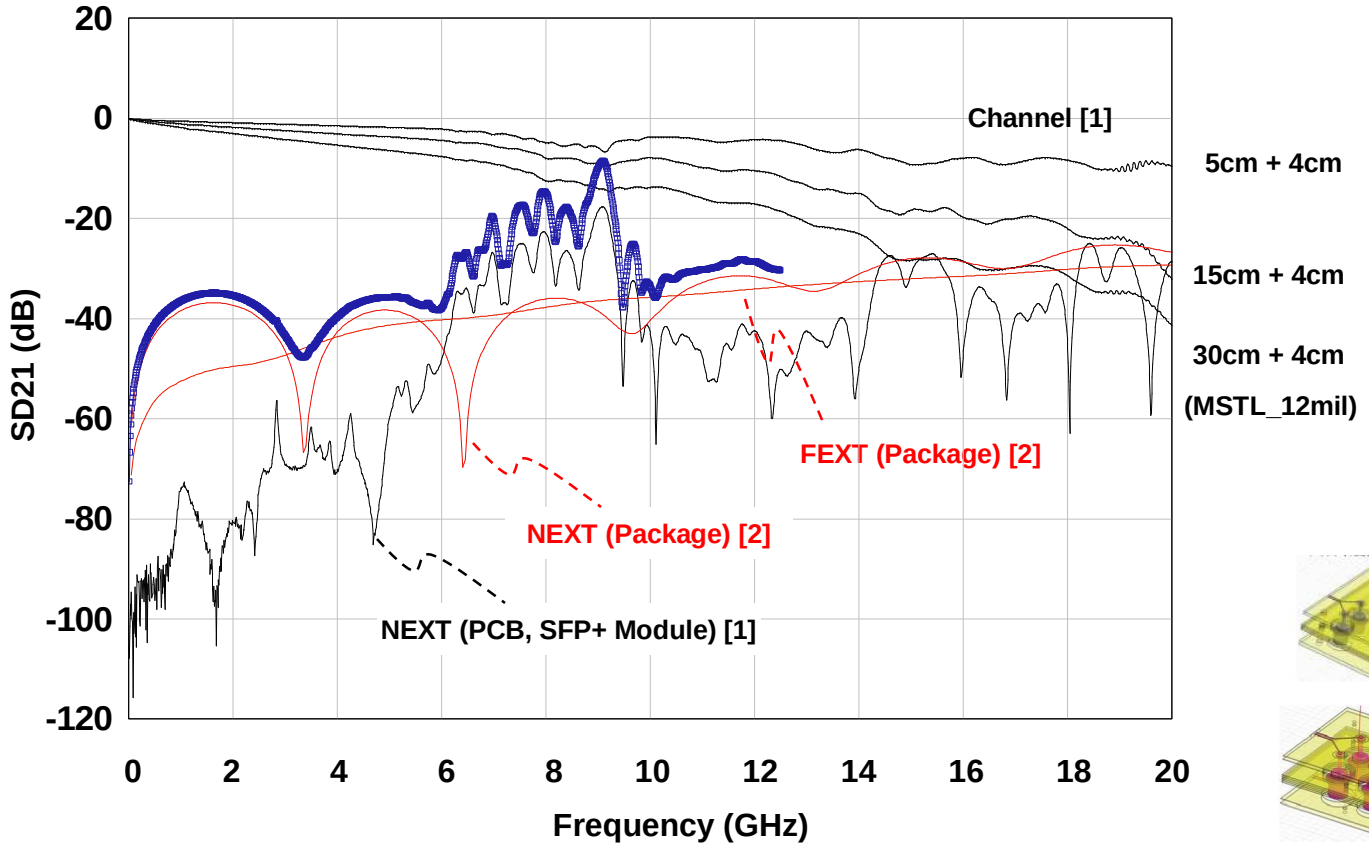
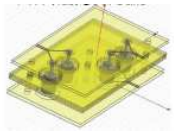
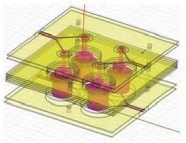
Channel IL and Crosstalk,
SFP+ Module and Package

Measured PCB and SFP+ Module Data [1] and Package Crosstalk [2]





Low Coupling



High Couplig

Blue heavy line: Power sum Crosstalk (One example)

(SFP+[1], Case1 Package[2])

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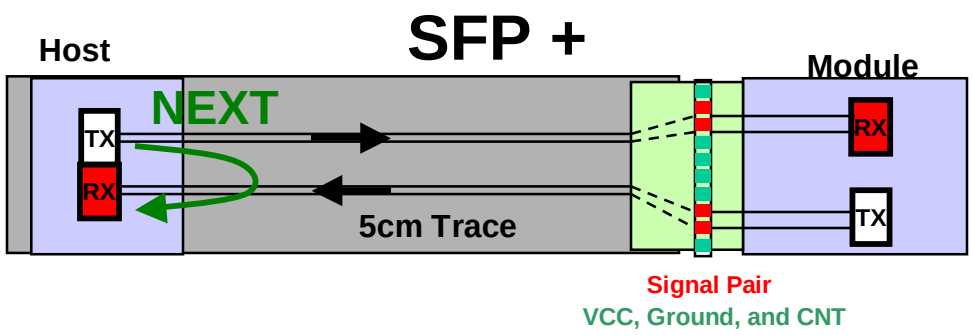
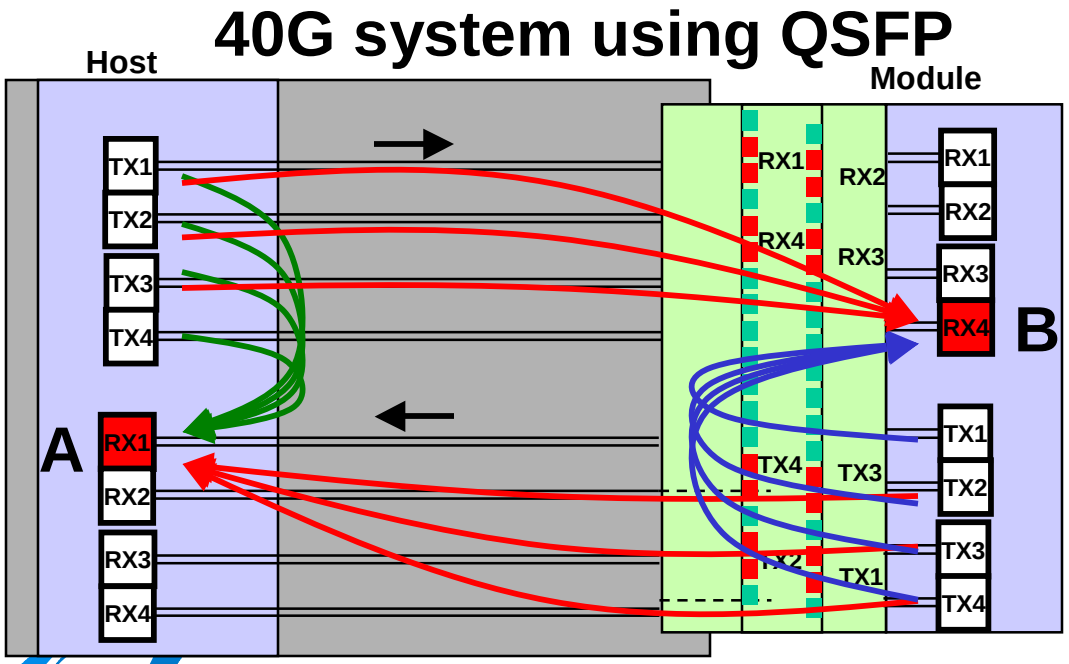
Worst Case Scenario



Data measured for SFP+

From SFP+ and package crosstalk data, the the worst case scenario for 40/100G system is estimated.



Crosstalk Increase

	Increase SFP → QSFP		Package from [2]	
	NEXT	FEXT	NEXT	FEXT
A	0dB (4ch)	+6dB (3ch)	0dB (4ch)	(3ch)
B	+3dB (4ch)		-6dB (4ch)	(3ch)

Assumption: Factor of 2.0 for 10-lane connector

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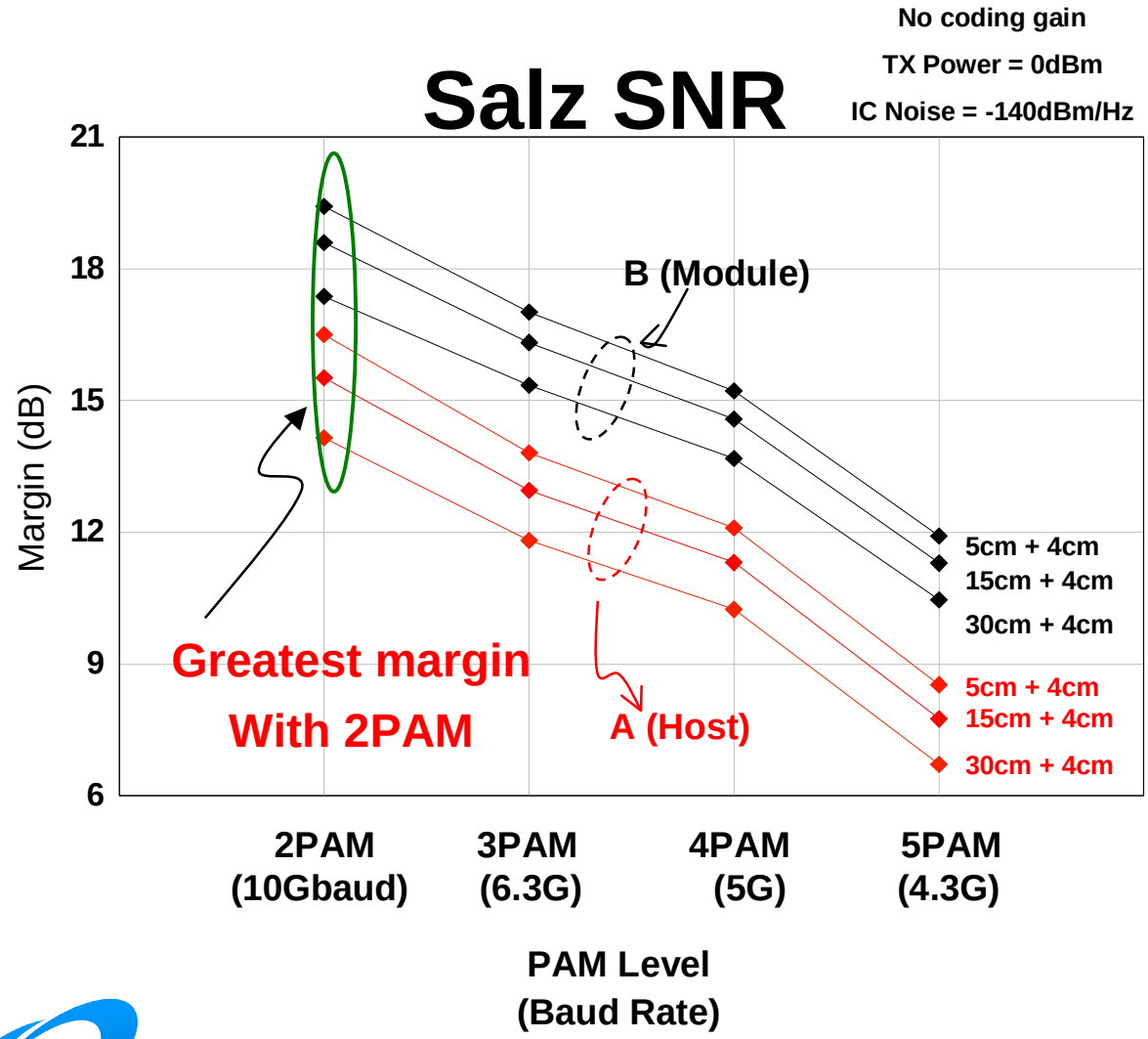
Signaling for 40G (4-lane)



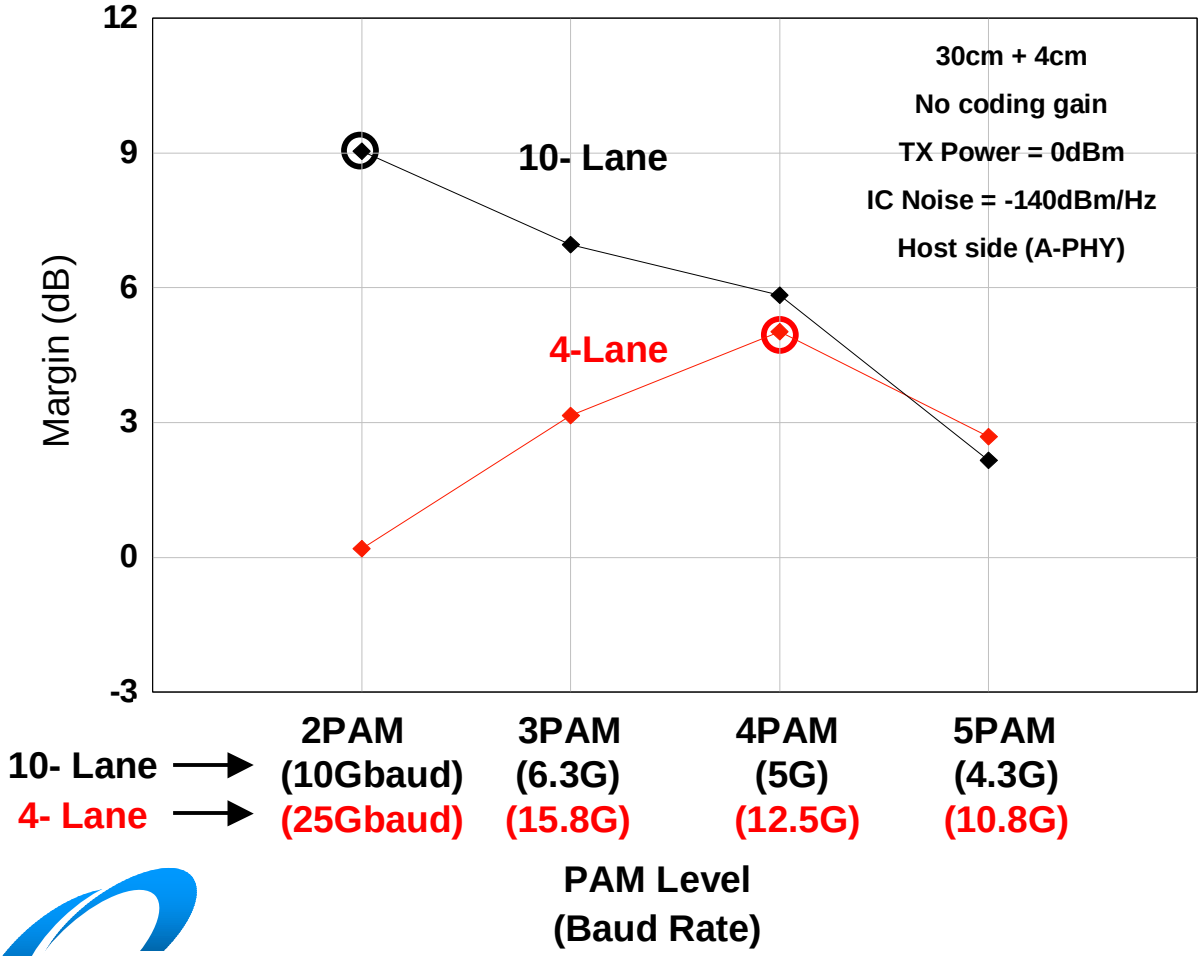
Host PHY (A) is worse than module PHY (B).

2PAM is the best signaling for 40G, 4-lane system.

Margin > 14dB

Signaling for 100G(4 & 10-lane)

Salz SNR



Greatest margin with

2PAM for 10-lane

4PAM for 4-lane

Margin = 9dB (2PAM, 10-Lane)

5dB (4PAM, 4-lane)

2PAM is worse than 4PAM by ~5dB for 4-lane system.

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Behavioral Time Domain Simulation

- How does BER relate to an EYE Diagram?
- Vertical EYE closure by ISI and Noise?
- Horizontal EYE closure by Jitter?
- How do we simulate random noise?
- What is the importance of sampling phase?

Some of these issues ignored and assumed to be ideal by Salz SNR are incorporated by the behavioral time domain simulation with key IC implementation impairments.

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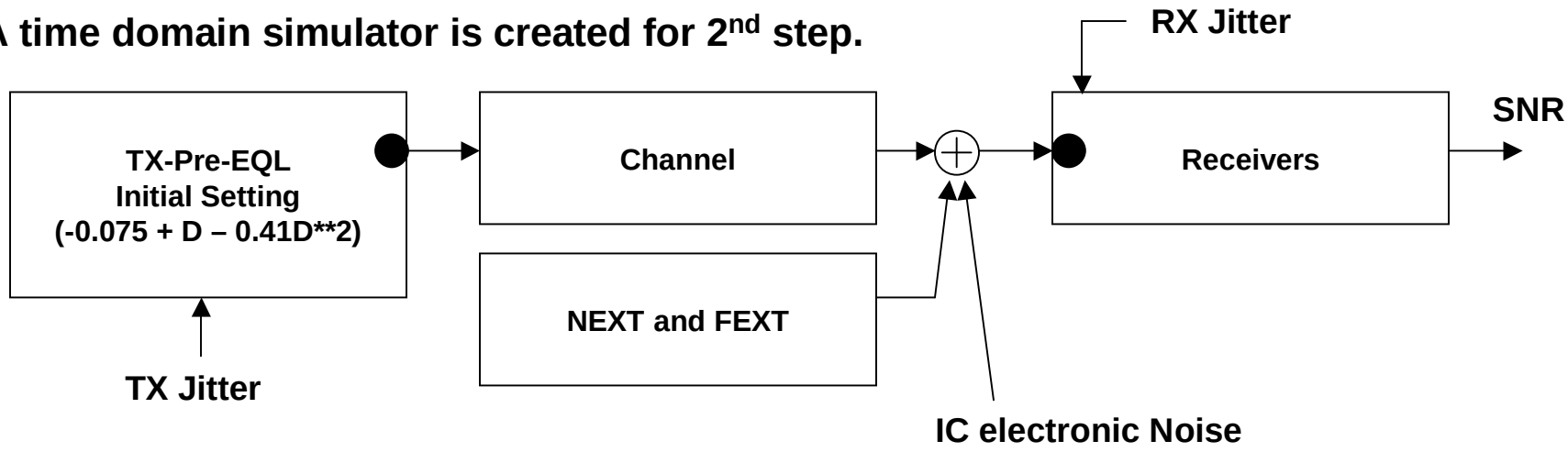
Behavioral Time Domain Simulation

A time domain simulator is created for 2nd step.



TX Jitter	**0.15UIpp jitter**
RX Jitter	**systematic timing recovery jitter**
IC Electronic Noise	**-140dBm/Hz**
FFE	**8 tap**
DFE	**8, 16, 32tap**

Crosstalk Canceller added later as an option

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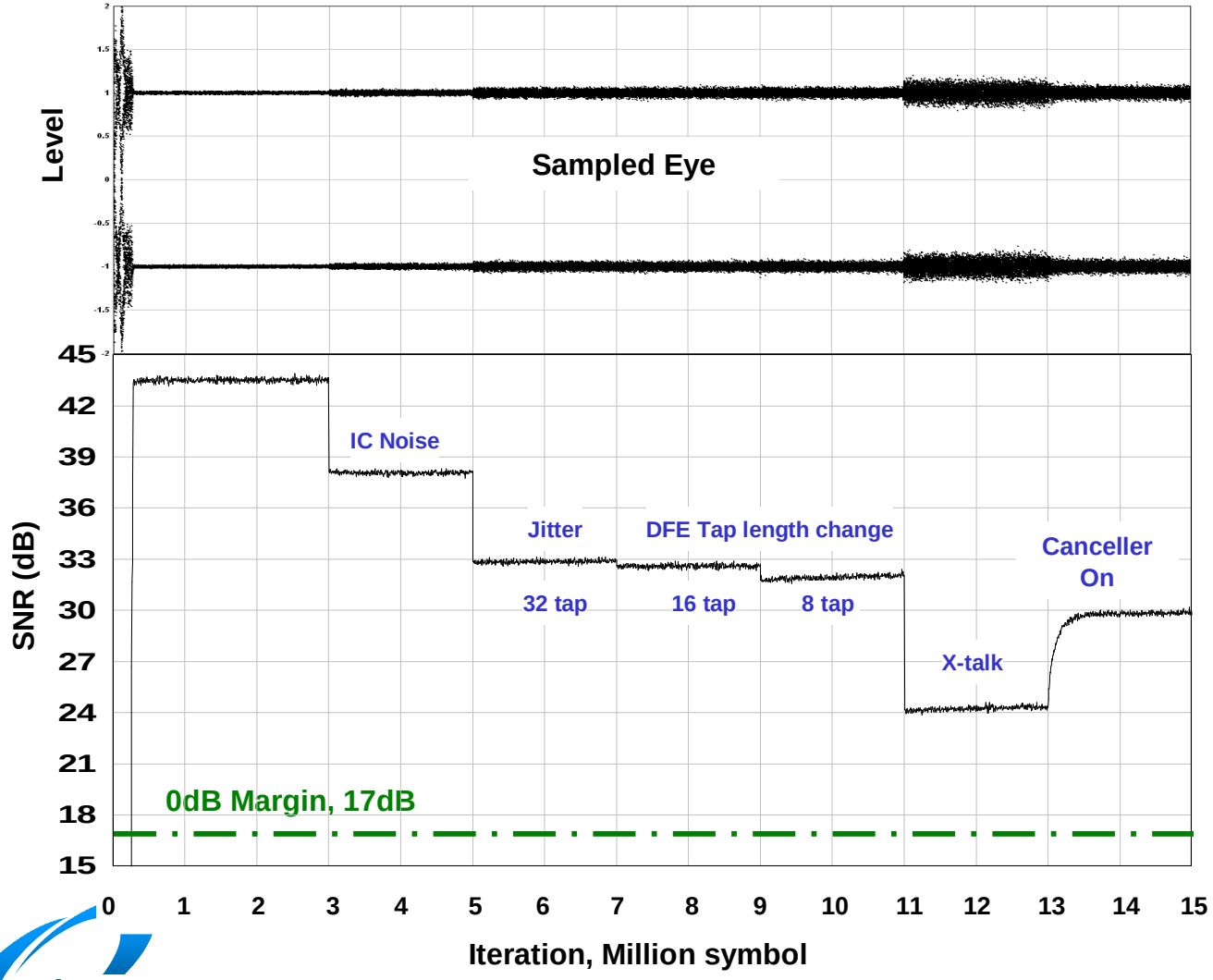
Result-1: 40G, 10G x 4-Lane

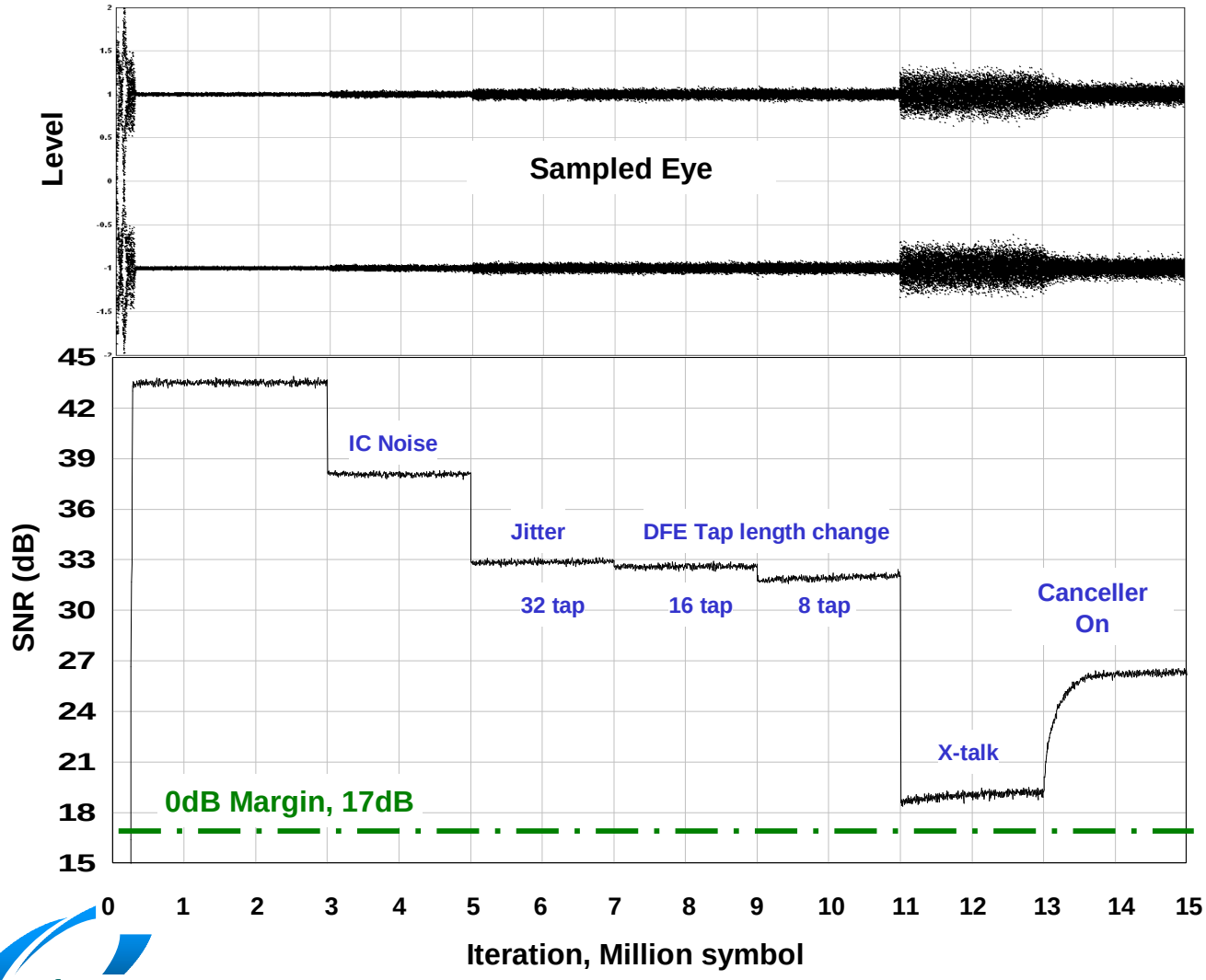


Channel: 30 + 4cm

Noise Margin:
7.5dB
(w/o canceller)

13.0dB
(w canceller)

Result-2: 100G, 10G x 10-Lane



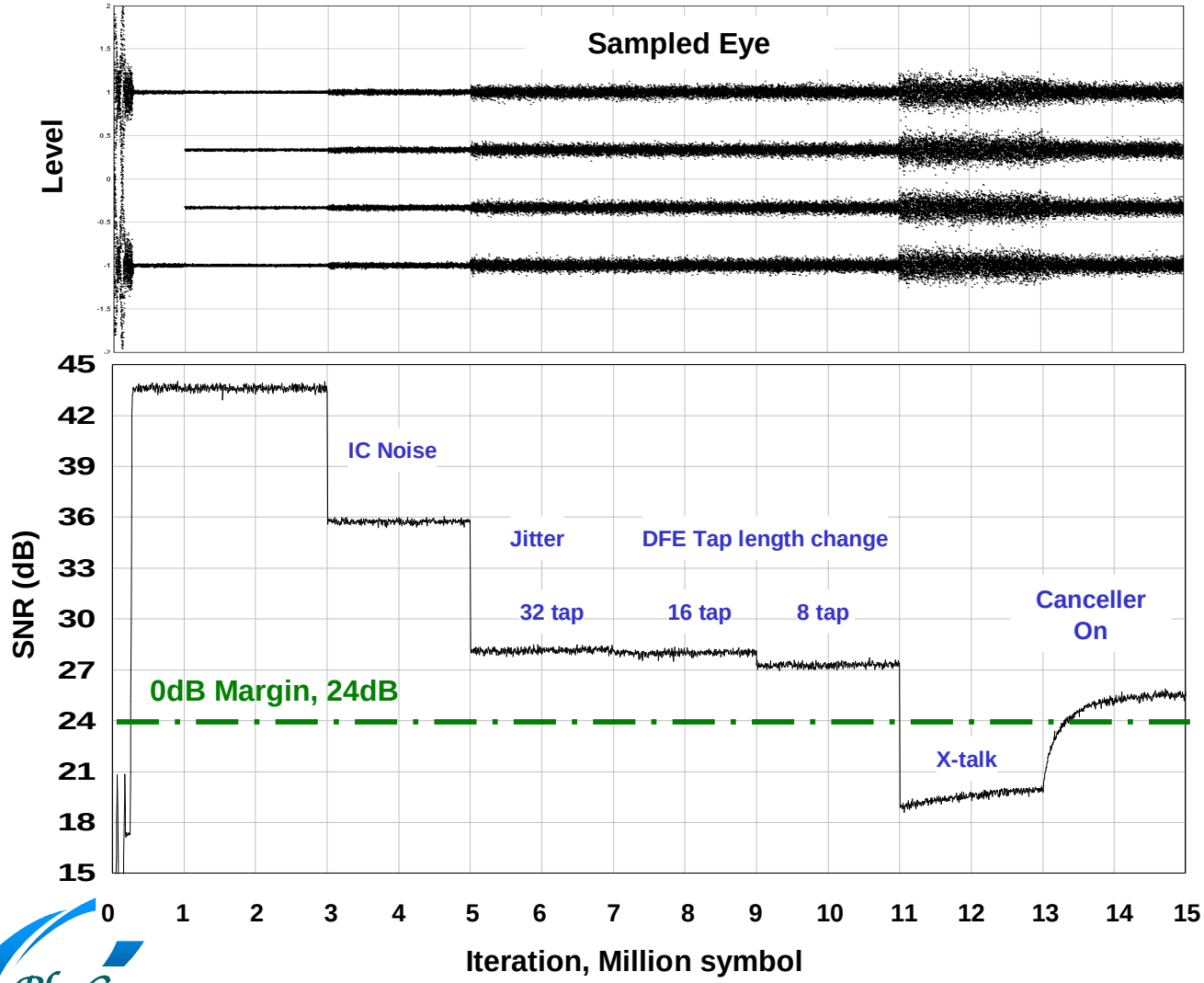
Channel: 30 + 4cm

Noise Margin:

2.3dB
(w/o canceller)

9.4dB
(w canceller)

Result-3: 100G, 25G x 4-Lane



Channel: 30 + 4cm

Noise Margin:

-4dB

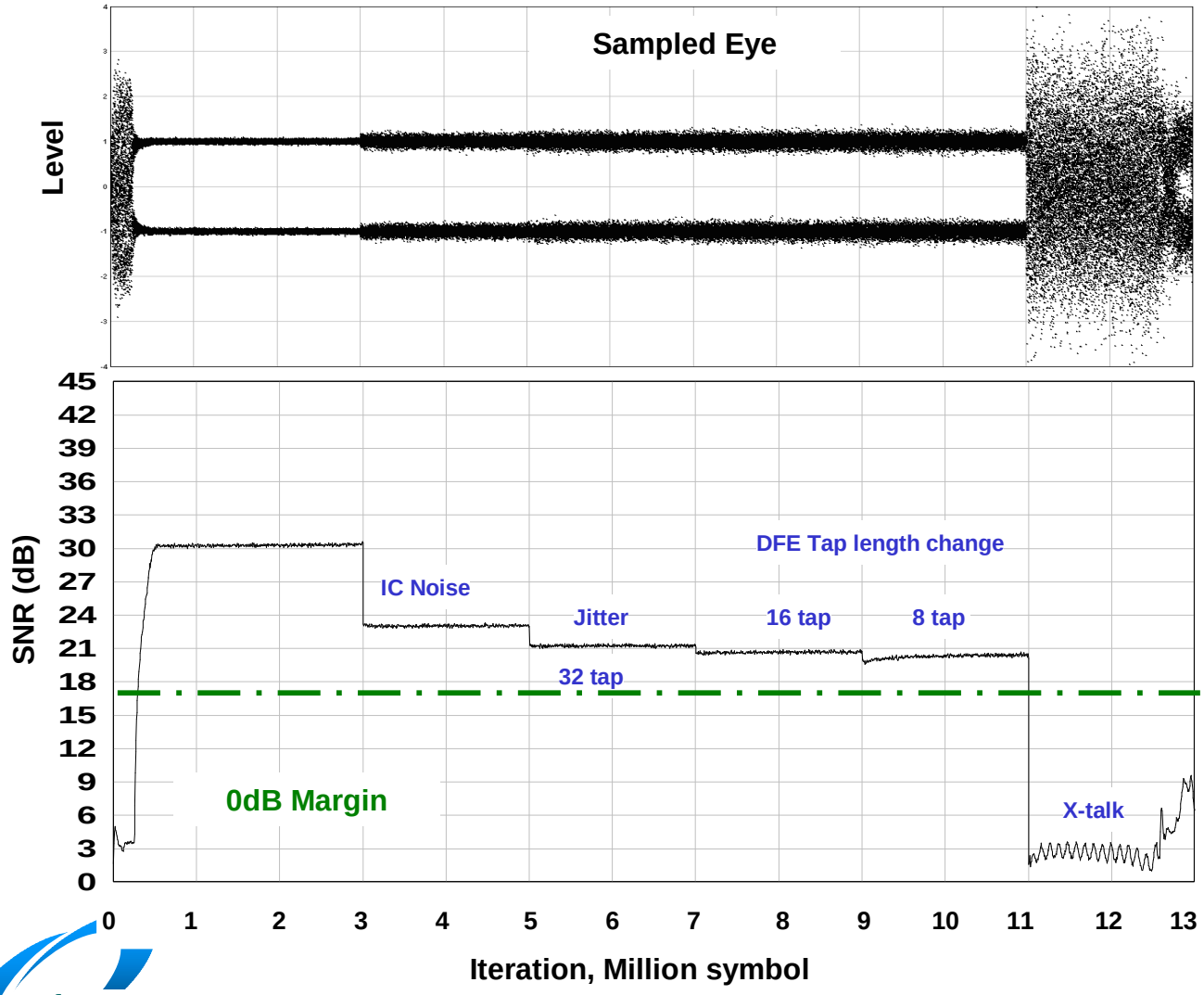
(w/o canceller)

1.6dB

(w canceller)

Result-4: 100G, 25G x 4-Lane

2PAM



Channel: 30 + 4cm

Not functional when crosstalk is added

Noise Margin Summary

	System	Channel	Theory		Time Domain Sim. A-PHY (Host)		
			Salz Margin				
			A (Host)	B (Module)	Basic	Crosstalk Canceller	With FEC (4dB)
40G	10G x 4 KR-4 (2PAM)	5 + 4cm	16.5dB	19.4dB	10.5dB	13.8dB	17.8dB
		15 + 4	15.5	18.6	9.0	14.3	18.3
		30 + 4	14.1	17.4	7.5	13.0	17.0
100G	10G x 10 (2PAM)	5 + 4	11.3	14.8	5.8	10.5	14.5
		15 + 4	10.4	14.0	3.8	10.7	14.7
		30 + 4	9.0	12.9	2.3	9.4	13.4
	25G x 4 (4PAM)	5 + 4	8.0	10.6	0.0	6.0	10.0
		15 + 4	6.8	9.5	-1.5	4.0	8.0
		30 + 4	5.0	7.9	-4.0	1.6	5.6

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Summary

Performance is estimated for 40/100G CEI based on the measured channel and package data.

1st Step: Signaling selection is made from the Salz SNR based on estimated crosstalk (Package and QSFP module) and IC electronic noise.

2nd Step: Check Jitter and other IC implementation loss by the time domain simulator

Results: Channel (IC package + 30cm PCB + QSFP module) & Practical IC implementation

1. **40G, 4-Lane: 2PAM is best. Noise margin is greater than 7.5dB.**
2. **100G,10-Lane: 2PAM is best. Noise margin, 2.3dB is not enough. Need crosstalk canceller and/or FEC.**
3. **100G, 4-Lane: 4PAM is best. Need crosstalk canceller and FEC.**

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