86 and 86A proposed revisions for crosstalk specification

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86. Physical Medium Dependent (PMD) sublayer and medium, type 40GBASE–SR4 and 100GBASE–SR10

86.7.1 Transmitter optical specifications

Each lane of a 40GBASE–SR4 or 100GBASE–SR10 optical transmitter shall meet the specifications of Table 86–6 per the definitions in 86.8.

Table 86–6—40GBASE–SR4 or 100GBASE–SR10 optical transmit characteristics

Description	Type	Value	Unit
Center wavelength	Range	840 to 860	nm
RMS spectral width[a]	Max	0.65	nm
Average launch power, each lane	Max	2.4	dBm
Average launch power, each lane	Min	–8	dBm
Optical Modulation Amplitude (OMA), each lane	Max	3	dBm
Optical Modulation Amplitude (OMA), each lane	Min	–6[b]	dBm
Difference in OMA between any lanes	Max	4	dB
Peak power, each lane	Max	4	dBm
Launch power in OMA minus TDP, each lane	Min	–6.7	dBm
Transmitter and dispersion penalty (TDP), each lane	Max	3.6	dB
Extinction ratio	Min	3	dB
Optical return loss tolerance	Max	12	dB
Encircled flux[c]		≥ 86% at 19 μm, ≤ 30% at 4.5 μm	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} hits per sample	Spec values	0.23, 0.34, 0.43, 0.27, 0.35, 0.4	
Average launch power of OFF transmitter, each lane	Max	–30	dBm

[a] RMS spectral width is the standard deviation of the spectrum
[b] Even if the TDP < 0.7 dB, the OMA (min) must exceed this value.
[c] If measured into type A1a.2 50 μm fiber in accordance with IEC 61280-1-4

86.7.3 40GBASE–SR4 or 100GBASE–SR10 receiver optical specifications

Each lane of a 40GBASE–SR4 or 100GBASE–SR10 optical receiver shall meet the specifications defined in Table 86–8 per the definitions in 86.8.

Table 86–8—40GBASE–SR4 or 100GBASE–SR10 optical receiver characteristics

Description	Type	Value	Unit
Center wavelength, each lane	Range	840 to 860	nm
Damage threshold[a]	Min	+3.4	dBm
Average power at receiver input, each lane	Max	+2.4	dBm
	Min	–9.9	dBm
Receiver reflectance	Max	–12	dB
Optical Modulation Amplitude (OMA), each lane	Max	3	dBm
Stressed receiver sensitivity in OMA, each lane[b]	Max	–5.4	dBm
Peak power, each lane	Max	4	dBm
Conditions of stressed receiver sensitivity test:			
Vertical eye closure penalty (VECP)[c], each lane	–	1.9	dB
Stressed eye J2 Jitter[c], each lane	–	0.3	UI
Stressed eye J9 Jitter[c], each lane	–	0.47	UI
OMA of each aggressor lane	–	–0.4	dBm
Receiver jitter tolerance in OMA, each lane[d]	Max	–5.4	dBm
Conditions of receiver jitter tolerance test:			
Jitter frequency and peak to peak amplitude	–	(75, 5)	(kHz, UI)
Jitter frequency and peak to peak amplitude	–	(375, 1)	(kHz, UI)
OMA of each aggressor lane	–	–0.4	dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
[b] Measured with conformance test signal at TP3 (see 86.8.4.7).
[c] Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver. The apparent discrepancy between VECP and TDP is because VECP is defined at eye center while TDP is defined with ±0.15 UI offsets of the sampling instant.
[d] This is a test of the optical receiver's ability to track low frequency jitter and is inappropriate for any subsystem that does not include a CRU.

86.8.2.1 Multi-lane testing considerations

TDP is defined for each lane, at a BER of 10^{-12} on that lane. Stressed receiver sensitivity, receiver jitter tolerance and host input signal tolerance (in Annex 86A) are defined for an interface BER of 10^{-12}. The interface BER is the average of the four or ten BERs of the receive lanes when they are stressed.

Measurements with Pattern 3 (PRBS31) allow lane-by-lane BER measurements. Measurements with Pattern 5 (scrambled idle) give the interface BER if all lanes are stressed at the same time. If each lane is stressed in turn, the BER is diluted by the three or nine unstressed lanes, and the BER for that stressed lane alone must be found, e.g. by multiplying by 4 or 10 if the unstressed lanes have low BER. To allow TDP measurement with Pattern 5, unstressed lanes for the error detector may be created by setting the power at the reference receivers well above their sensitivities, or by copying the contents of the transmit lanes not under BER test to the error detector by other means. In stressed receiver sensitivity and receiver jitter tolerance measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. ~~Either each~~ One or more receive lane~~s~~ ~~is~~ are stressed in turn while all are operated~~, or all can be stressed together~~. All aggressor lanes are operated as specified. To find the interface BER, the BERs of all the lanes when stressed are averaged.

Where relevant, parameters are defined with all co-propagating and counter-propagating lanes operational so that crosstalk effects are included. Where not otherwise specified, the maximum amplitude (OMA or VMA) for a particular situation is used, and for counter-propagating lanes, the minimum transition time is used. While the lanes in a particular direction share a common clock, the Tx and Rx directions are not synchronous to each other.

86.8.4.7 Stressed receiver sensitivity

Stressed receiver sensitivity shall be within the limits given in Table 86–8 if measured using the method defined by 52.9.9 with the conformance test signal at TP3 and with the following exceptions:

a) 52.9.9 defines the reference test procedure for a single lane. See 86.8.2.1 and below for multi-lane considerations.
b) The sinusoidal amplitude interferer is replaced by a Gaussian noise generator.
c) The sinusoidal jitter is at a fixed 80 MHz frequency.
d) The Gaussian noise generator, the amplitude of the sinusoidal jitter and the Bessel-Thomson filter are adjusted so that the VECP, J2 Jitter and J9 Jitter specifications given in Table 86–8 are simultaneously met (the random noise effects such as RIN, random clock jitter do not need to be minimized).
e) The pattern for the received compliance signal is specified in Table 86–12.
f) The interface BER of the PMD receiver is the average of the BER of all receive lanes while stressed and at the ~~same~~ specified receive OMA.
g) Where nPPI or XLAUI/CAUI is exposed, a PMD receiver is considered compliant if it meets the module electrical output specifications at TP4 given in Table 86A–3 for nPPI, or the requirements in Table 83B–3 for XLAUI/CAUI.

Stressed receiver sensitivity is defined with all transmit and receive lanes in operation. ~~All~~ One or more receive lanes ~~may be stressed at the same time, or each receive lane may be stressed~~ are tested in turn while all aggressor receive lanes are operated as specified in Table 86-8. Pattern 3 or Pattern 5, or a valid 40GBASE–R4 or 100GBASE–R10 signal is sent from the transmit section of the receiver under test. The signal being transmitted is asynchronous to the received signal. If Pattern 3 is used for the transmit and receive lanes not under test, there is at least 31 UI delay between the PRBS31 patterns generated on one lane and any other lane.

For 40GBASE-SR4 and 100GBASE-SR10, the relevant BER is the interface BER. The interface BER is the average of the four or ten BERs of the receive lanes when stressed: see 86.8.2.1.

86.8.4.8 Receiver jitter tolerance

Receiver jitter tolerance shall be as defined as in 68.6.11, with the following differences:

a) 68.6.11 defines the reference test procedure for a single lane: see 86.8.2.1 for multi-lane considerations;
b) The pattern to be received is specified in Table 86–12;
c) The parameters of the signal are specified in Table 86–8 and the power in OMA at the receiver is set to the maximum for receiver jitter tolerance in OMA given in Table 86–8;
d) ~~All~~ One or more receive lanes ~~may be stressed at the same time, or each receive lane may be stressed~~ are tested in turn while all are operated. All aggressor lanes are operated as specified in Table 86–8;
e) The receive lanes not being tested are receiving Pattern 3, Pattern 5, or a valid 40GBASE-R4 or 100GBASE-R10 signal;
f) The transmitter is transmitting one of these signals using all lanes;
g) The transmitter and the receiver are not synchronous;
h) The interface BER of the PMD receiver is the average of the BER of all receive lanes when stressed;
i) The mode-conditioning patch cord suitable for 62.5/125 μm fiber is not used.

Annex 86A

(normative)

Parallel Physical Interface (nPPI) for 40GBASE-SR4 and 40GBASE-LR4 (XLPPI) and 100GBASE-SR10 (CPPI)

86A.4 Electrical specifications for nPPI

86A.4.1 nPPI host to module electrical specifications

Each output lane and signal of the nPPI host (PMA), if measured at TP1a (see 86A.5.1) with the specified crosstalk signals applied on all input lanes, shall meet the specifications of Table 86A–1 per the definitions in 86A.5. Each lane of the nPPI module (PMD) electrical input, if measured at TP1 and TP1a with all Rx lanes (module output) operating, shall meet the specifications of Table 86A–2 per the definitions in 86A.5. The module electrical input shall be AC coupled, i.e. it shall present a high DC common-mode impedance at TP1. There may be various methods for AC coupling in actual implementations.

Table 86A–1—nPPI host electrical output specifications at TP1a

Parameter description	Min	Max	Units	Conditions
Single ended output voltage	–0.3	4	V	Referred to signal common
AC common-mode output voltage	–	15	mV	RMS
Termination mismatch at 1 MHz	–	5	%	
Differential output return loss	See 86A.4.1.1	–	dB	
Common-mode output return loss	See 86A.4.1.2	–	dB	
Output transition time, 20% to 80%	28	–	ps	
J2 Jitter output	–	0.17	UI	
J9 Jitter output	–	0.29	UI	
Data Dependent Pulse Width Shrinkage (DDPWS)	–	0.07	UI	
Q_{sq}	45	–	V/V	
	Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	0.11, 0.31 95, 350		UI mV	Hit ratio = 5×10^{-5}
Crosstalk source VMA, each input lane	700		mV	At TP4
Crosstalk source transition times, 20% to 80%	34		ps	At TP4

Table 86A–2—nPPI module electrical input specifications at TP1 and TP1a

Parameter description	Test point	Min	Max	Units	Conditions
Single ended input voltage tolerance[a]	TP1a	–0.3	4	V	Referred to TP1 signal common
AC common-mode input voltage tolerance	TP1a	15	–	mV	RMS
Differential input return loss	TP1	See 86A.4.1.1	–	dB	10 MHz to 11.1 GHz
Differential to common-mode input return loss	TP1	10	–	dB	10 MHz to 11.1 GHz
J2 Jitter tolerance	TP1a	0.17	–	UI	
J9 Jitter tolerance	TP1a	0.29	–	UI	
Data Dependent Pulse Width Shrinkage (DDPWS) tolerance	TP1a	0.07	–	UI	
		Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	TP1a	0.11, 0.31 95, 350		UI mV	Hit ratio = 5×10^{-5}
Crosstalk calibration signal VMA	TP4	850		mV	While calibrating compliance signal[b]
Crosstalk calibration signal transition times, 20% to 80%	TP4	34		ps	

[a] The single ended input voltage tolerance is the allowable range of the instantaneous input signals

[b] The crosstalk calibration signals are applied to the mated HCB-MCB at TP4a and measured at TP4 following the same principles as the host electrical input calibration (see 86A.5.3.8.5). They are removed before testing.

86A.4.2 nPPI module to host electrical specifications

Each electrical output lane and signal of the nPPI module (PMD), if measured at TP4, shall meet the specifications of Table 86A–3 per the definitions in 86A.5 while the specified crosstalk sources are applied to the module's electrical input. Each lane of the nPPI host (PMA) input shall meet the specifications of

Table 86A–3—nPPI module electrical output specifications at TP4

Parameter description	Min	Max	Units	Conditions
Single ended output voltage tolerance	–0.3	4	V	Referred to signal common
AC common-mode output voltage (RMS)	–	7.5	mV	
Termination mismatch at 1 MHz	–	5	%	
Differential output return loss	See	–	dB	10 MHz to 11.1 GHz
Common-mode output return loss	See 86A.4.2.2	–	dB	10 MHz to 11.1 GHz
Output transition time, 20% to 80%	28	–	ps	
J2 Jitter output	–	0.42	UI	
J9 Jitter output	–	0.65	UI	
	Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	0.29, 0.5 150, 425		UI mV	Hit ratio = 5×10^{-5}
Crosstalk source VMA, each lane	700		mV	At TP1a
Crosstalk source transition times, 20% to 80%	34		ps	At TP1a

Table 86A–4 at TP4 and/or TP4a per the definitions in 86A.5. The module electrical output shall be AC coupled, i.e. it shall present a high DC common-mode impedance at TP4. There may be various methods for AC coupling in actual implementations.

Table 86A–4—nPPI host electrical input specifications at TP4 and TP4a

Parameter description	Test point	Min	Max	Units	Conditions
Single ended input voltage[a]	TP4	–0.3	4	V	Referred to signal common
AC common-mode input voltage tolerance	TP4	7.5	–	mV	RMS
Differential input return loss	TP4a	See	–	dB	
Differential to common-mode input return loss	TP4a	10	–	dB	10 MHz to 11.1 GHz
Host input signal tolerance, interface BER limit		–	10^{-12}	–	
Conditions of host electrical receiver signal tolerance test:[b]					
		Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	TP4	0.29, 0.5 150, 425		UI mV	Hit ratio = 5×10^{-5}
Transition time, 20% to 80%		34		ps	
J2 Jitter	TP4	0.42		UI	
J9 Jitter	TP4	0.65		UI	
Data Dependent Pulse Width Shrinkage (DDPWS)		0.34		UI	
VMA of aggressor lanes	TP4	850		mV	
Crosstalk calibration signal VMA	TP1a	700		mV	
Crosstalk calibration signal transition times, 20% to 80%	TP1a	~~28~~ 34		ps	

[a] The host is required to tolerate (work correctly with) input signals with instantaneous voltages anywhere in the specified range.
[b] The specification values are test conditions for measuring signal tolerance and are not characteristics of the host (see 86A.5.3.8).

86A.5.3.8 Host input signal tolerance

To be compliant the host input signal tolerance shall satisfy the requirements of 86A.5.3.8.1 to 86A.5.3.8.6.

86A.5.3.8.1 Introduction

This clause provides guidance for jitter tolerance testing at the host input (PMA) compliance point TP4/TP4a. Compliance is required with input jitter, vertical eye closure (Y1), and vertical peak level (Y2) as specified in Table 86A–4. Compliance is defined at an interface BER (the average of the BERs of all the lanes when stressed) of 10^{-12}. There are two test conditions: once each for the sensitivity and overload vertical eye parameters conditions. The reference test procedure is described in detail for a single stressed lane. ~~Either each~~ One or more Rx lanes are tested ~~is stressed~~ in turn ~~or they are all stressed at the same time~~ while all lanes are operated. Aggressor lanes are operated with the VMA specified in Table 86A–4.

86A.5.3.8.6 Test procedure

Testing is performed differentially through a Host Compliance Board (see 86A.5.1).

Using a test signal arranged according to and calibrated according to 86A.5.3.8.5, operate the system with the test pattern specified in Table 86A–6. Either ~~each~~ one or more lanes are tested ~~stressed~~ in turn while all are operated, or all can be tested ~~stressed~~ together. Aggressor lanes are operated with the VMA specified in Table 86A–4. The BERs of all the lanes when stressed are averaged to form the interface BER. See 86.8.2.1.

All signals and reference clocks that operate during normal operation are active during the test including all the other host lanes in both directions. The test signal and the host's transmitted signals are asynchronous. The host transmits Pattern 3 (PRBS31), Pattern 5, or a valid 40GBASE-SR4 or 100GBASE-SR10 signal. The sinusoidal jitter is stepped across the frequency and amplitude range according to Table 86A–5 and illustrated in Figure 86A–1, while monitoring the BER of the lane(s). The interface BER of a compliant host receiver remains below 10^{-12}.