# Limiting Versus Linear Optical Receiver for Stressed Receiver Sensitivity

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IEEE P802.3ba, Quebec City, May 2009

# LR4 Stressed Receiver Sensitivity Test

- 40G and 100G Ethernet Optical PMD interfaces specify SRS tests
- For LR4, Table 88-8 specifies stressed receiver sensitivity of -6.8dBm, with conditions of 1.8dB VECP and 0.3UI pk-pk stressed eye jitter
- The stress creates vertical and horizontal pulse shrinkage
- Important to understand implications of this pulse shrinkage and how it relates to linear versus limiting interfaces

# Pulse Shrinkage

- 0.3UI p-p stressed eye jitter is specified in Table 88-8 for the stress pattern. In worst case this could cause pulse shrinkage by 30%.
- In addition, random noise further contributes to jitter and pulse shrinkage. Assuming a compliant receiver with 1dBm margin on specified -8.6dBm receiver sensitivity for 1E-12 BER, we can calculate random noise. We estimate it to contribute approximately 0.35UI p-p jitter.
- Together, the total pulse shrinkage could be as bad as 0.3+0.35=0.65UI. The eye opening remaining will be roughly 14ps.

# Limiting vs Linear Interface

## Limiting Interface

- Pro
  - Overall good SNR
  - Simpler interface
- Con
  - 14ps pulses would require very high bandwidth PHY device

## Linear Interface

- Pro
  - No information is lost
- Con
  - Greater complexity

# Conclusion

- Stress test specified in Table 88-8 is challenging.
- Very narrow pulses can be generated if limiting TIA is used.
- A linear TIA preserves the stressed eye parameters, which can then be resolved in the PHY chip.
- More study is needed to understand potential issues related to pulse shrinkage.

# Backup

# Jitter Estimate

- OMA (with 1dB margin) = -9.6dBm with 1E-12 BER

  => 109.6uW p –p

  => rms noise = 7.77uW (109.6/14.1)
- OMA of -6.8dBm for stressed source

  => 208.9uW p-p

  =>Ratio of swing = 0.525 =>

  Pulse Shrinkage of 0.35UI
  - Assuming sine wave internal waveshape