Clause 83 Directions

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Key issues related to PMA

- PMA vs. PMA stage

  There are multiple stages of PMA – inconsistently referred to as separate PMAs or PMA stages

  Were it not for FEC which can appear between PMA stages, there would be some appeal to using the term “PMA” to talk about the group of PMA stages and “PMA stage” to refer to an individual stage. But presence of FEC between PMA sublayers gives weight to calling the stages individual PMAs

- PMA Interfaces

  Based on comment 383 discussion, all PMA interfaces are abstract unless realized physically as XLAUI/CAUI or PMD service interface for 40GBASE-SR4 or 100GBASE-SR-10

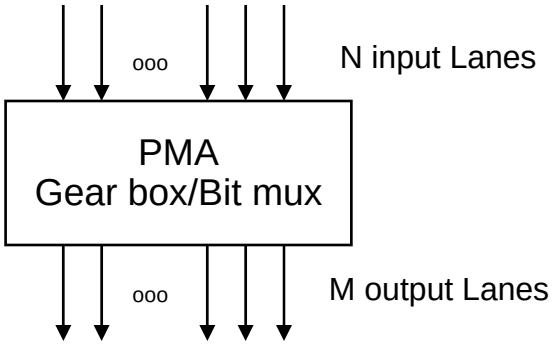
- Unidirectional Specification

  The major mux/demux operation of the PMA is the same whether the PMA is in the Tx or Rx direction. Most logic track participants like the uni-directional paradigm. Bidirectional operation consists of a Tx PMA with p input lanes and q output lanes paired with an Rx PMA with q input lanes and p output lanes

Key issues related to PMA

- Primitive naming
  - Unidirectional specification results in input/output primitives that are independent of Rx or Tx direction
  - Aliases at top and bottom of stack so that adjacent sublayers can use traditional naming
- Indexing of managed devices
  - Open, but approach to be proposed at conclusion of these slides

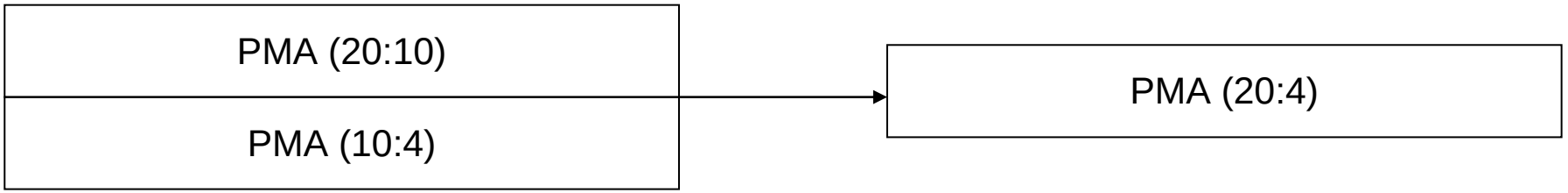
A Parameterized PMA



- Generic Behaviors:
  - Z is the number of PCS Lanes
  - N input lanes, each with Z/N PCS lanes
  - M output lanes, each with Z/M PCS lanes
  - Lane muxing behavior generic, independent of position or direction
- Behaviors dependent on direction:
  - Signal indicate logic – Link Status only in Rx direction
- Behaviors dependent on adjacent interfaces
  - PMA related skew points only measurable when they appear on physically instantiated interfaces
  - Test Patterns only valid when the adjacent interface is physically instantiated (e.g., XLAUI/CAUI) or toward the PMD (whether there is an exposed PMD service interface or not)
- Behavior dependent on position
  - System loopback only valid at top of stack (adjacent to PCS or adjacent PCS/FEC)
  - Line loopback only valid at bottom of stack (adjacent to PMD)

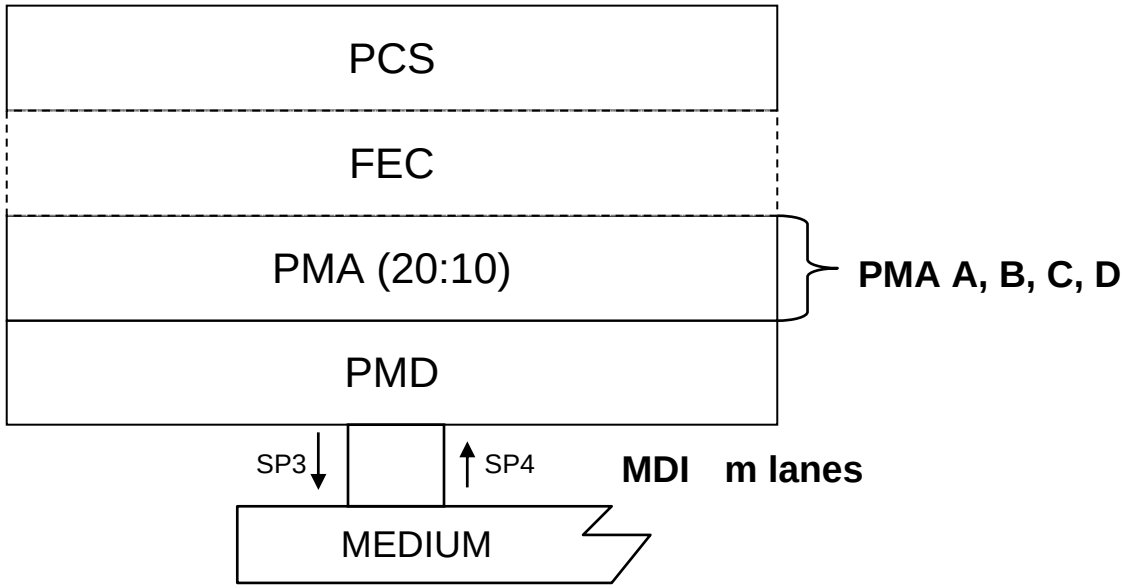
Comment 383 resolution

For 40GBASE-R, the number of input and output lanes are divisors of 4 and
or 100GBASE-R, the number of input and output lanes are divisors of 20



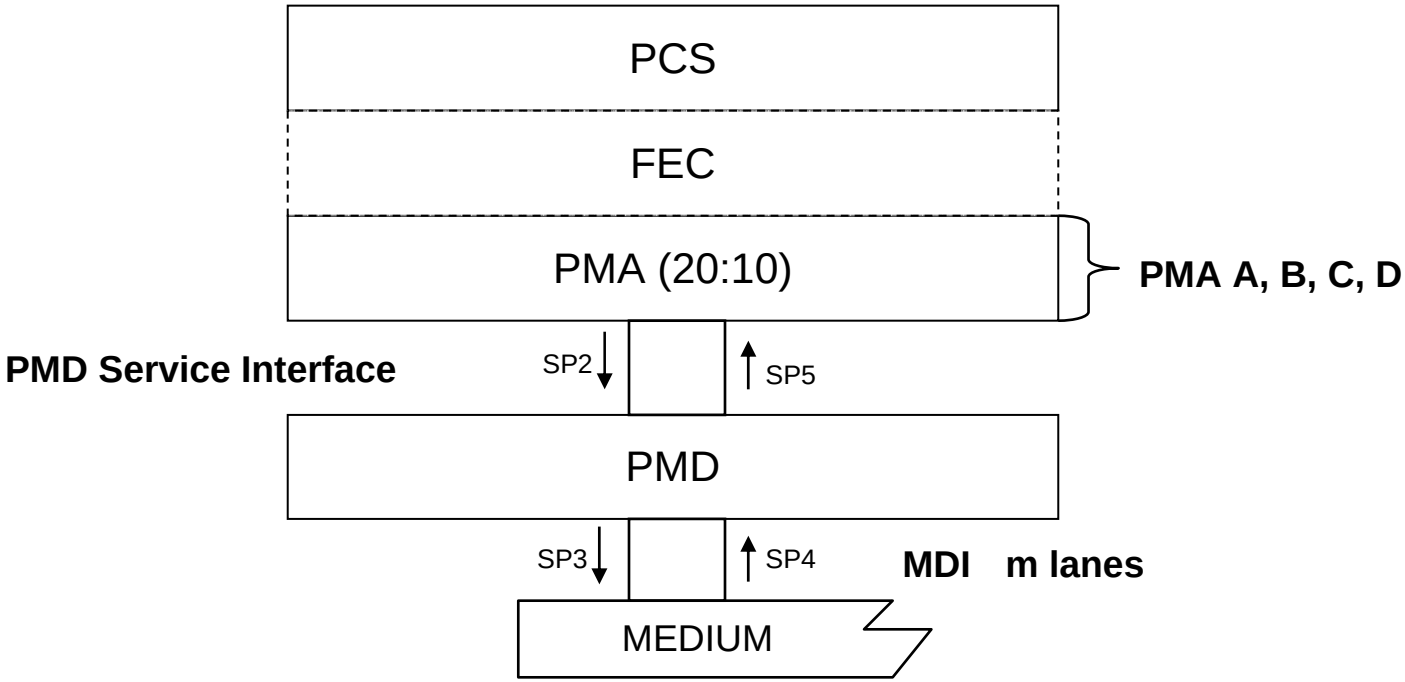
Since the interfaces are abstract when there is not a physical instantiation, we don't need to draw adjacent PMA stages when there is not a physically instantiation of the interface between them

100GBASE-R Case 1
All abstract interfaces, FEC with PCS, if present

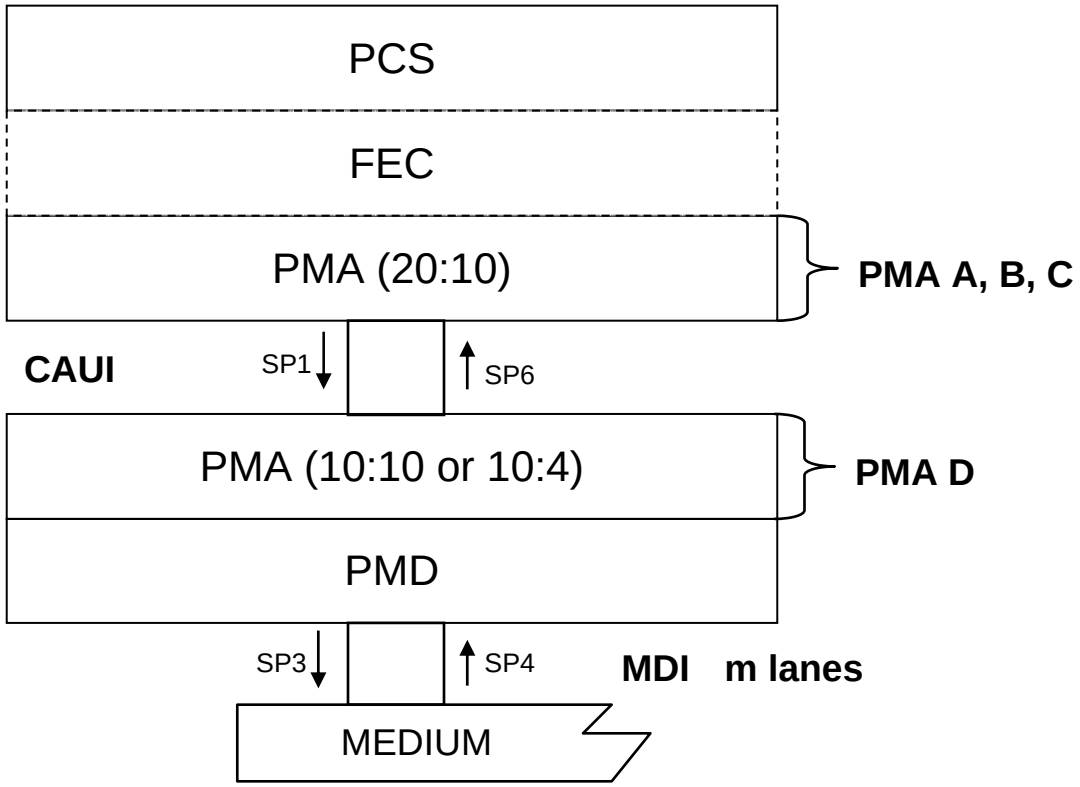


100GBASE-R Case 2

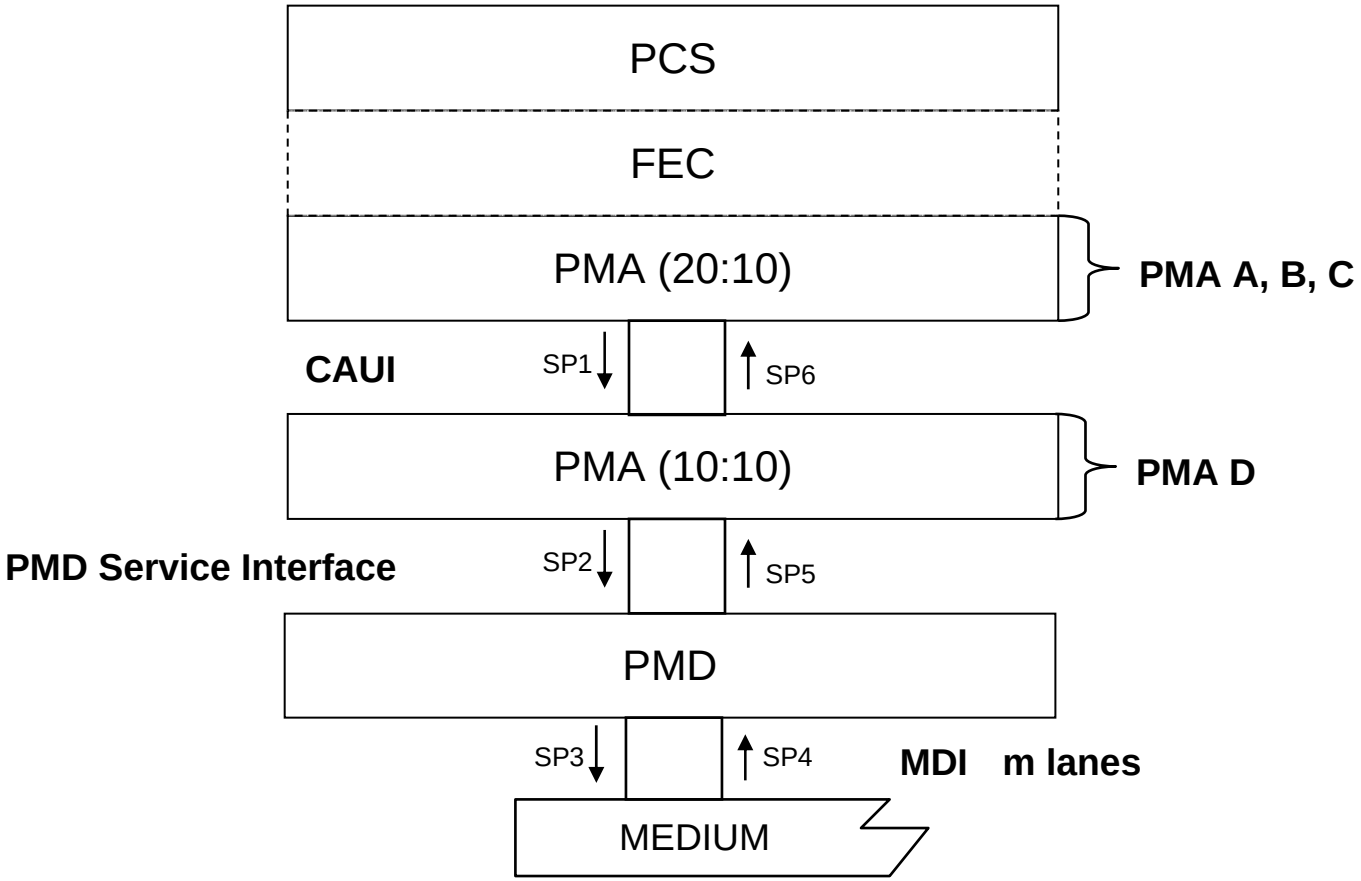
With physical PMD service interface, FEC with PCS, if present



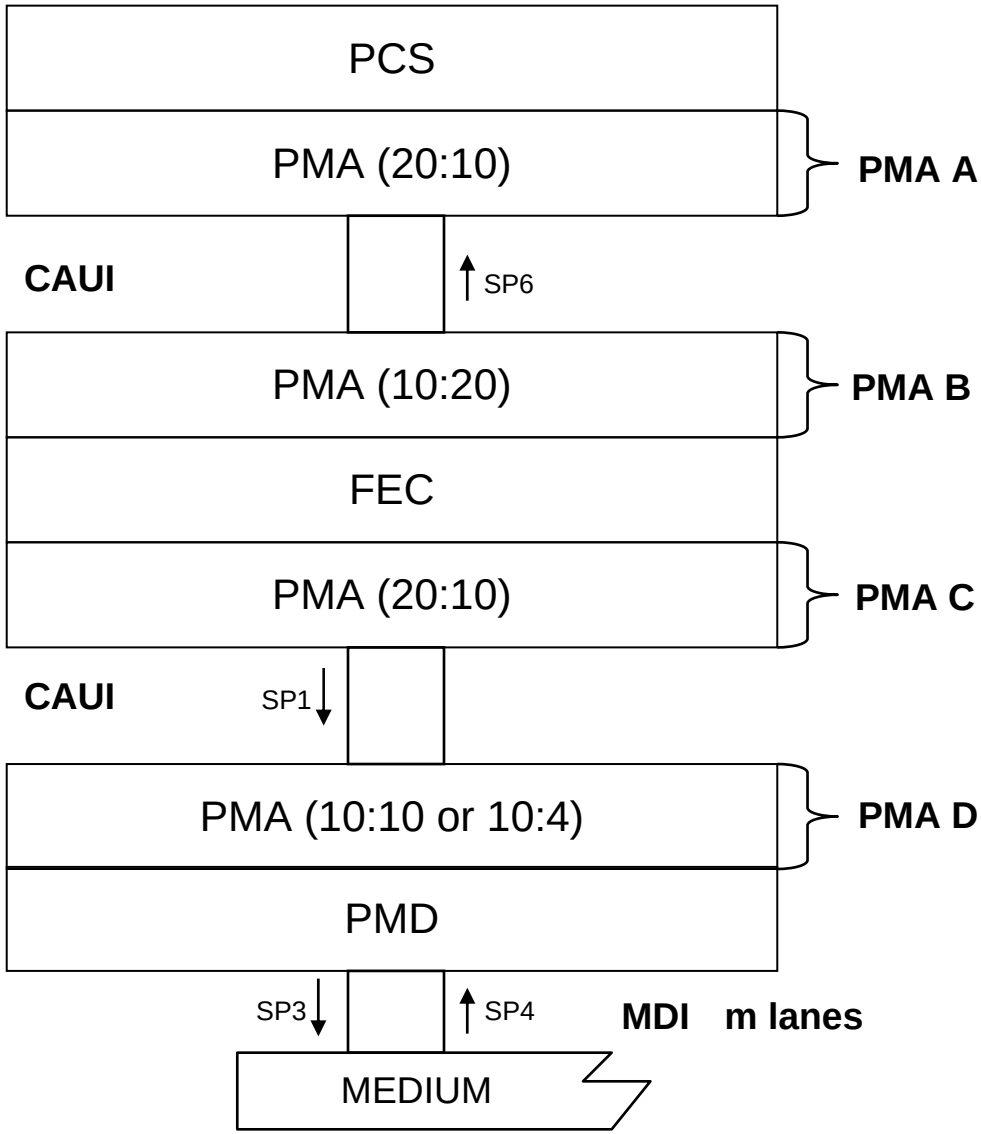
100GBASE-R Case 3
With single CAUI, FEC with PCS, if present



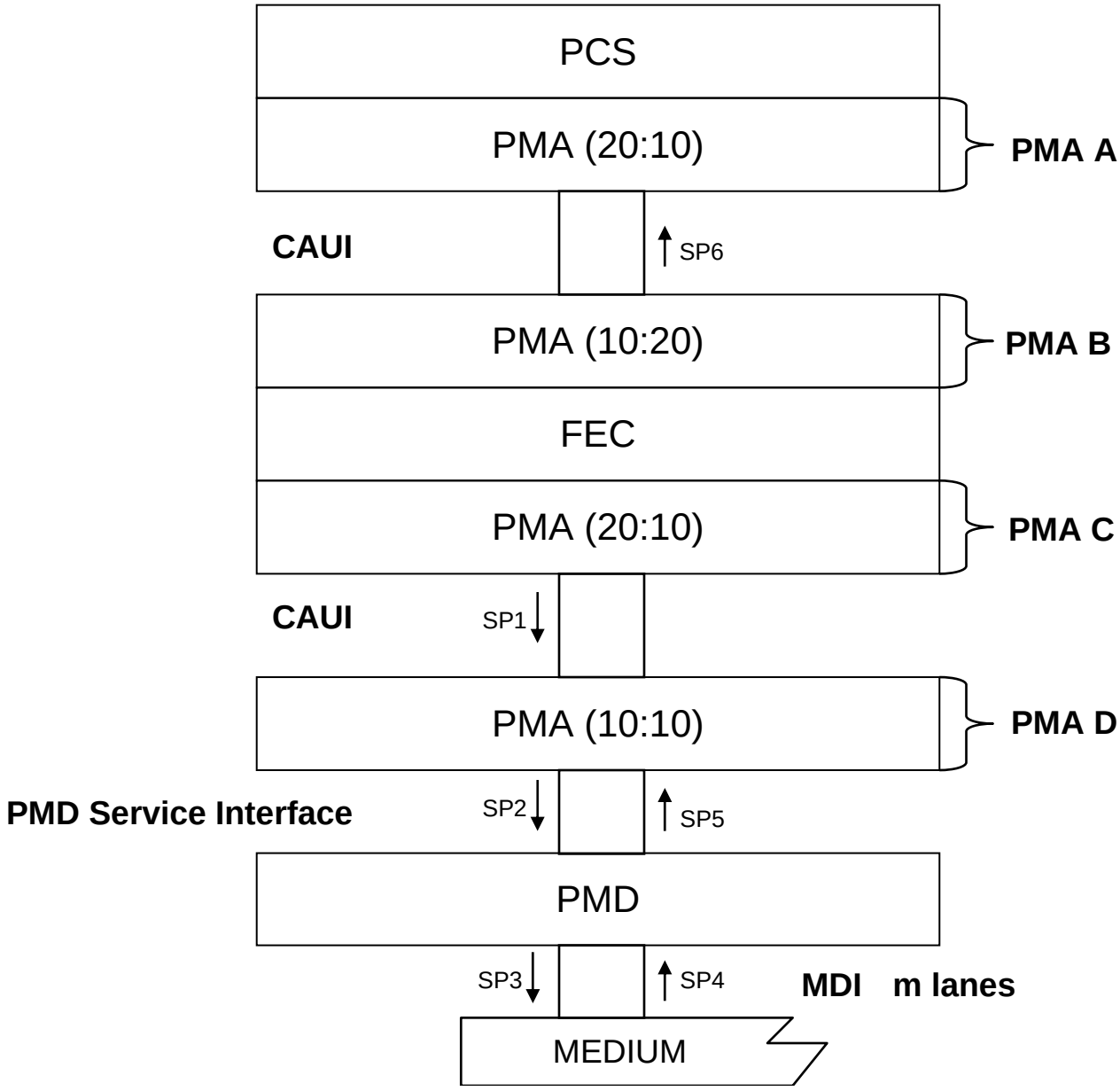
100GBASE-R Case 4
CAUI and PMD service interfaces, FEC with PCS, if present



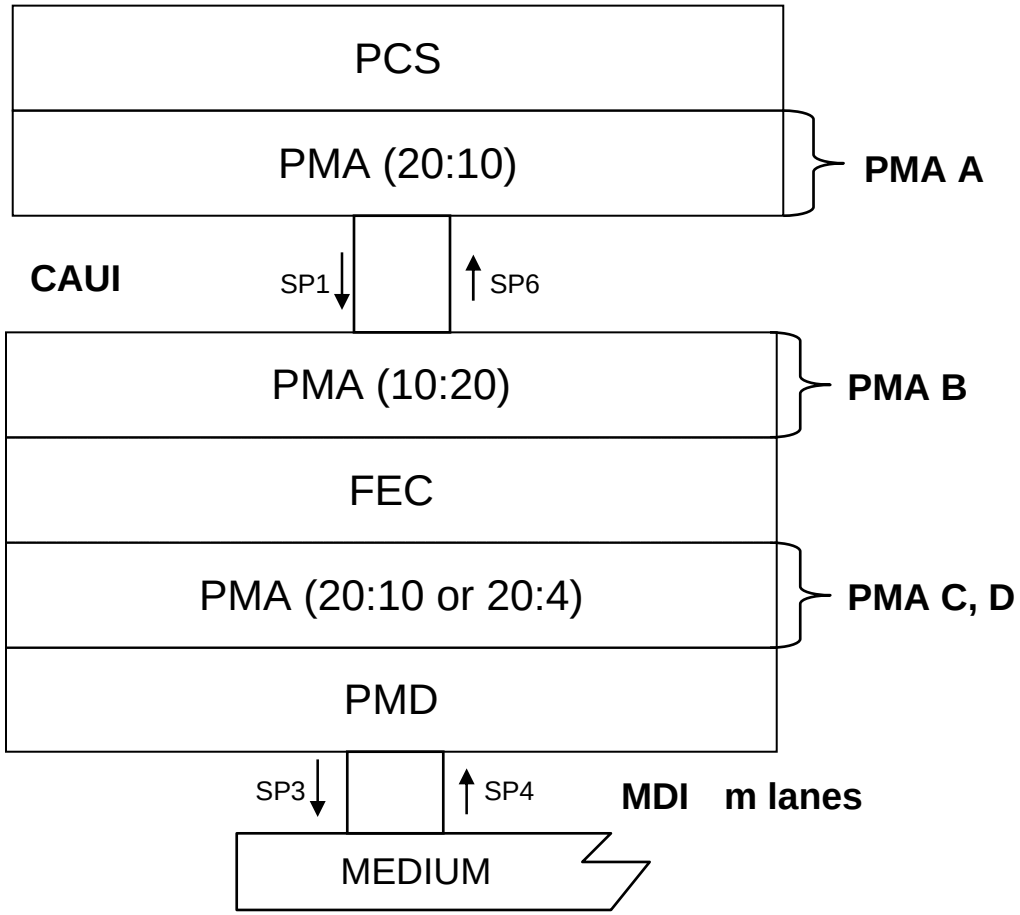
100GBASE-R Case 5
FEC independent of PCS or PMD



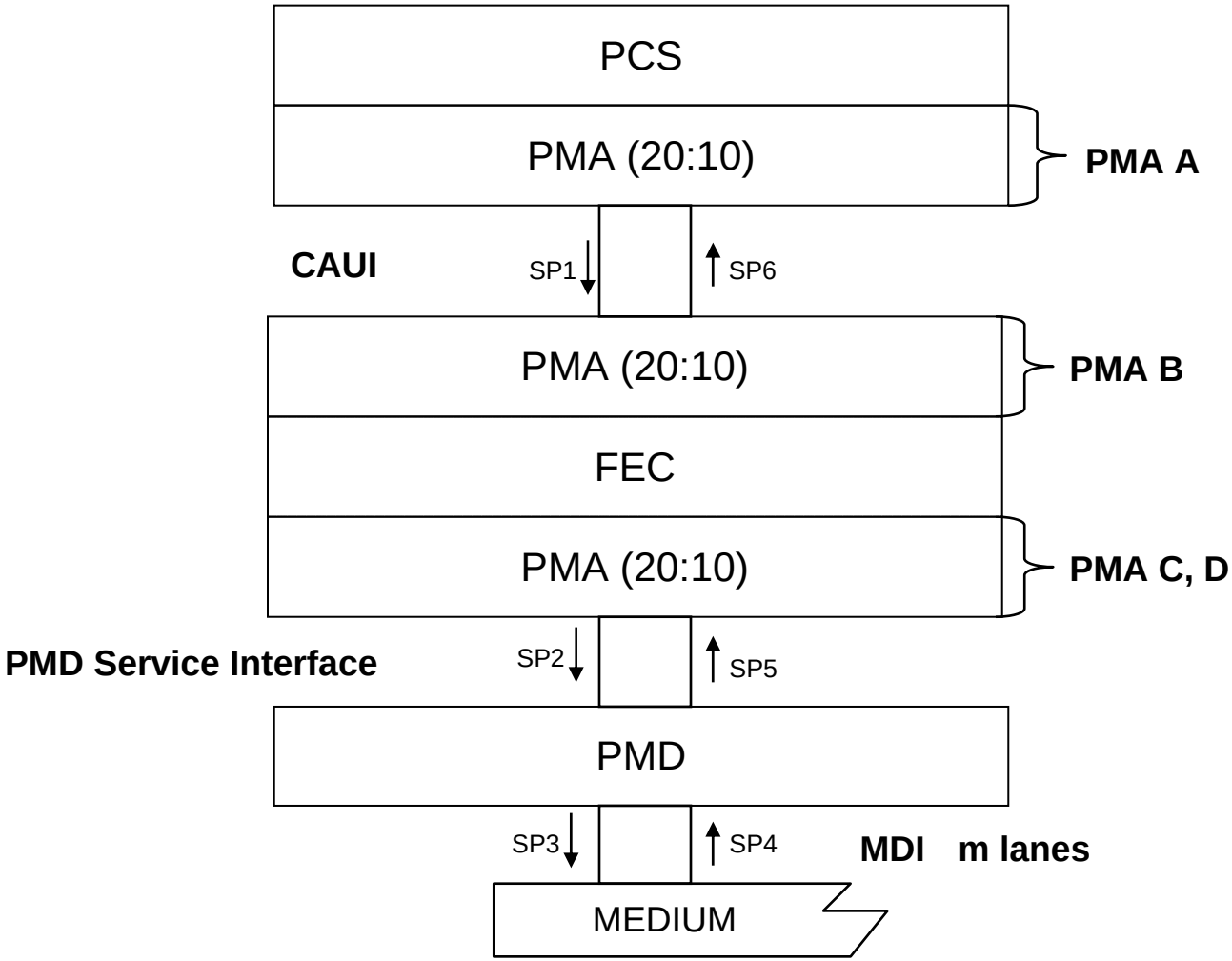
100GBASE-R Case 6
FEC independent of PCS or PMD, physical PMD service interface



100GBASE-R Case 7
FEC with PMD



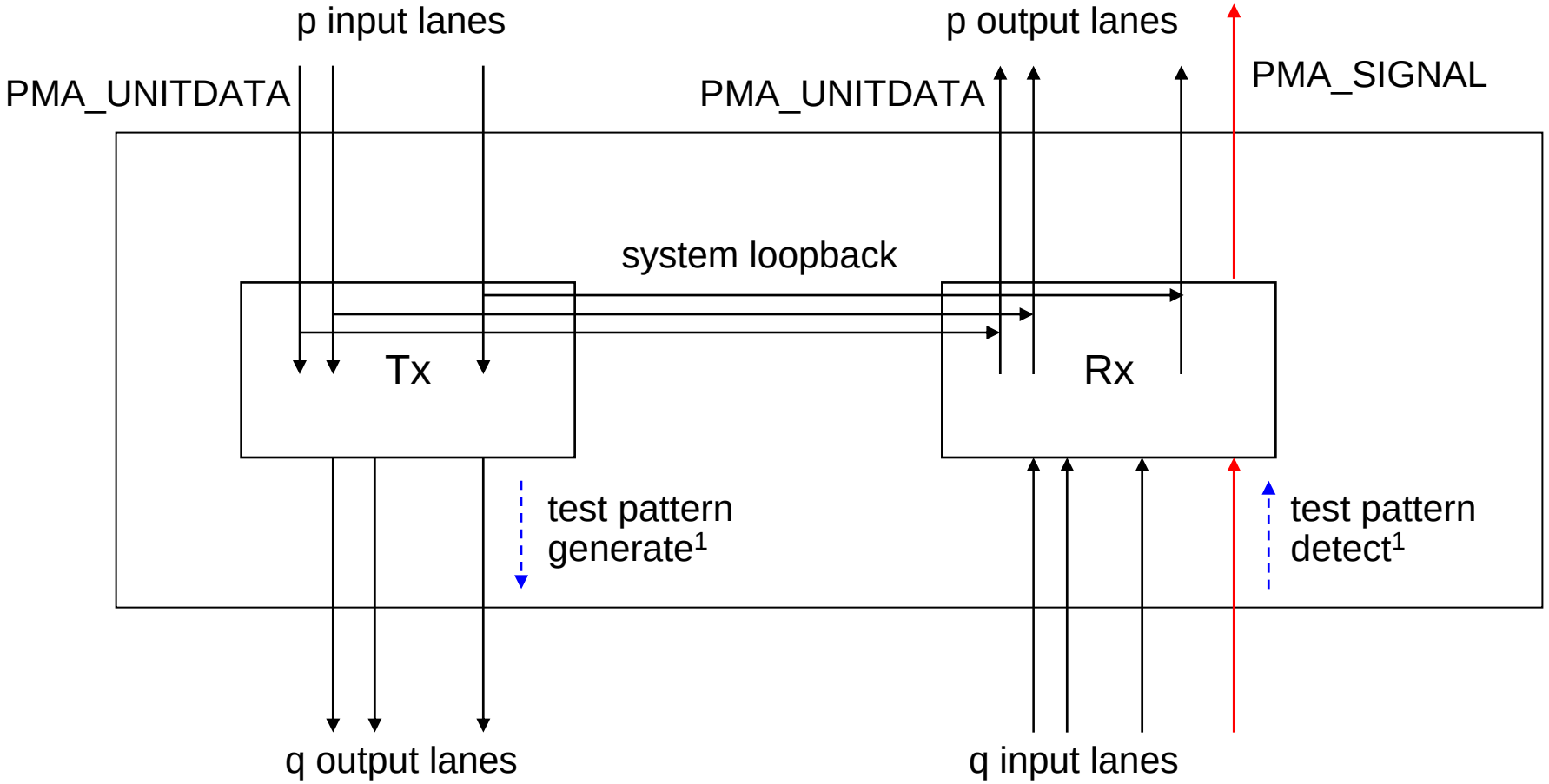
100GBASE-R Case 8
FEC adjacent to PMD, physical PMD service interface



Four possible PMA blocks/groupings

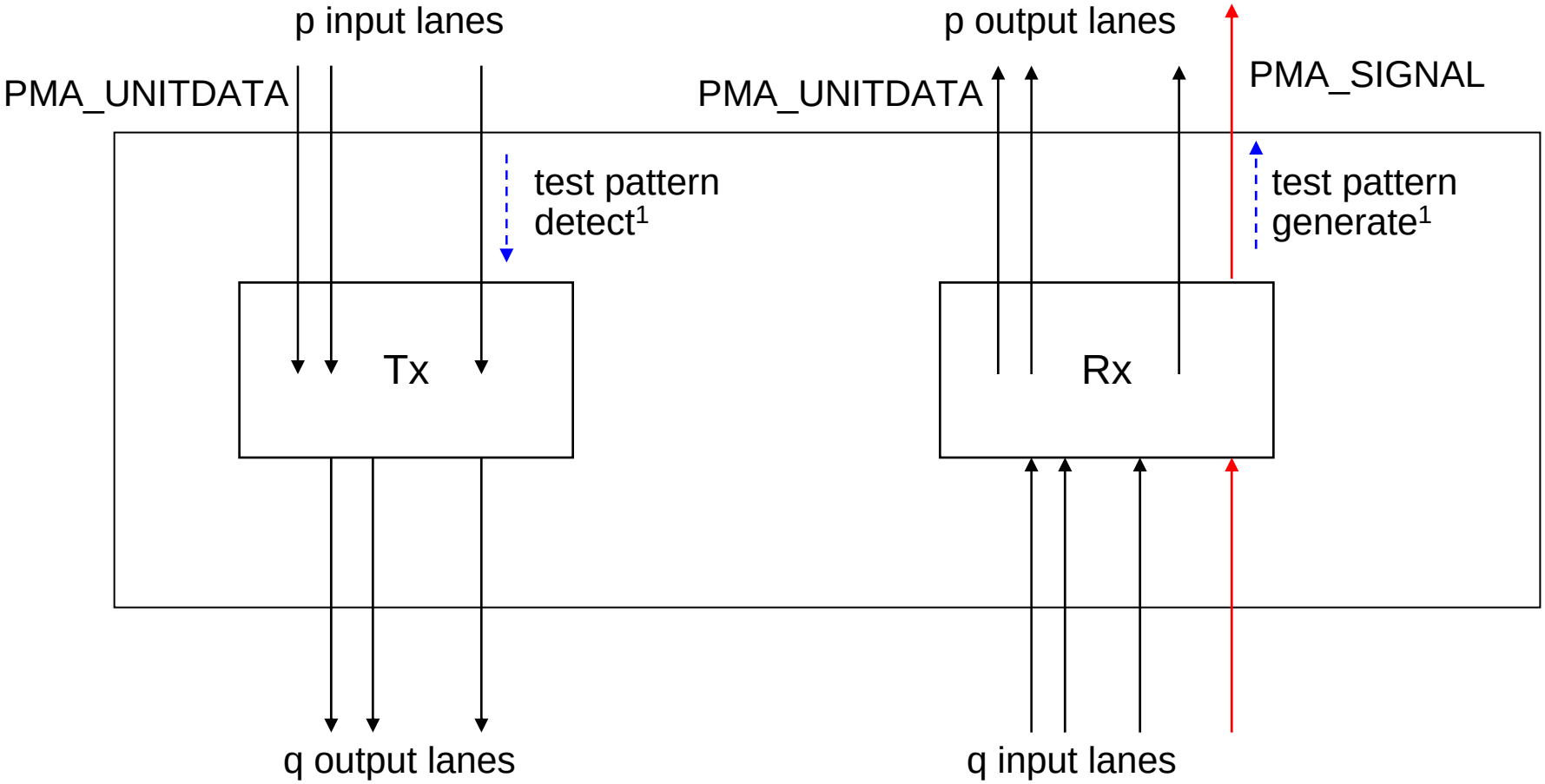
- PMA A
  - Adjacent to PCS, or FEC if FEC is adjacent to PCS
  - Implements System Loopback toward PCS
  - If adjacent CAUI below, implements Tx test pattern generate and Rx test pattern detect
- PMA B
  - Distinct from PMA A only if FEC is separated from PCS by a CAUI
  - PMA between (upper) CAUI and FEC
  - If adjacent CAUI above, implements Rx test pattern generate and Tx test pattern detect
- PMA C
  - Distinct from PMA A, B only if FEC is separated from PCS by a CAUI
  - PMA below FEC
  - If adjacent CAUI below, implements Tx test pattern generate and Rx test pattern detect
- PMA D
  - PMA adjacent to PMD or PMD service interface
  - Distinct from PMA C only if CAUI below separate FEC
  - Implements line loopback
  - Implements Tx test pattern generate and Rx test pattern detect
  - If adjacent CAUI above, implements Rx test pattern generate and Tx test pattern detect

PMA A



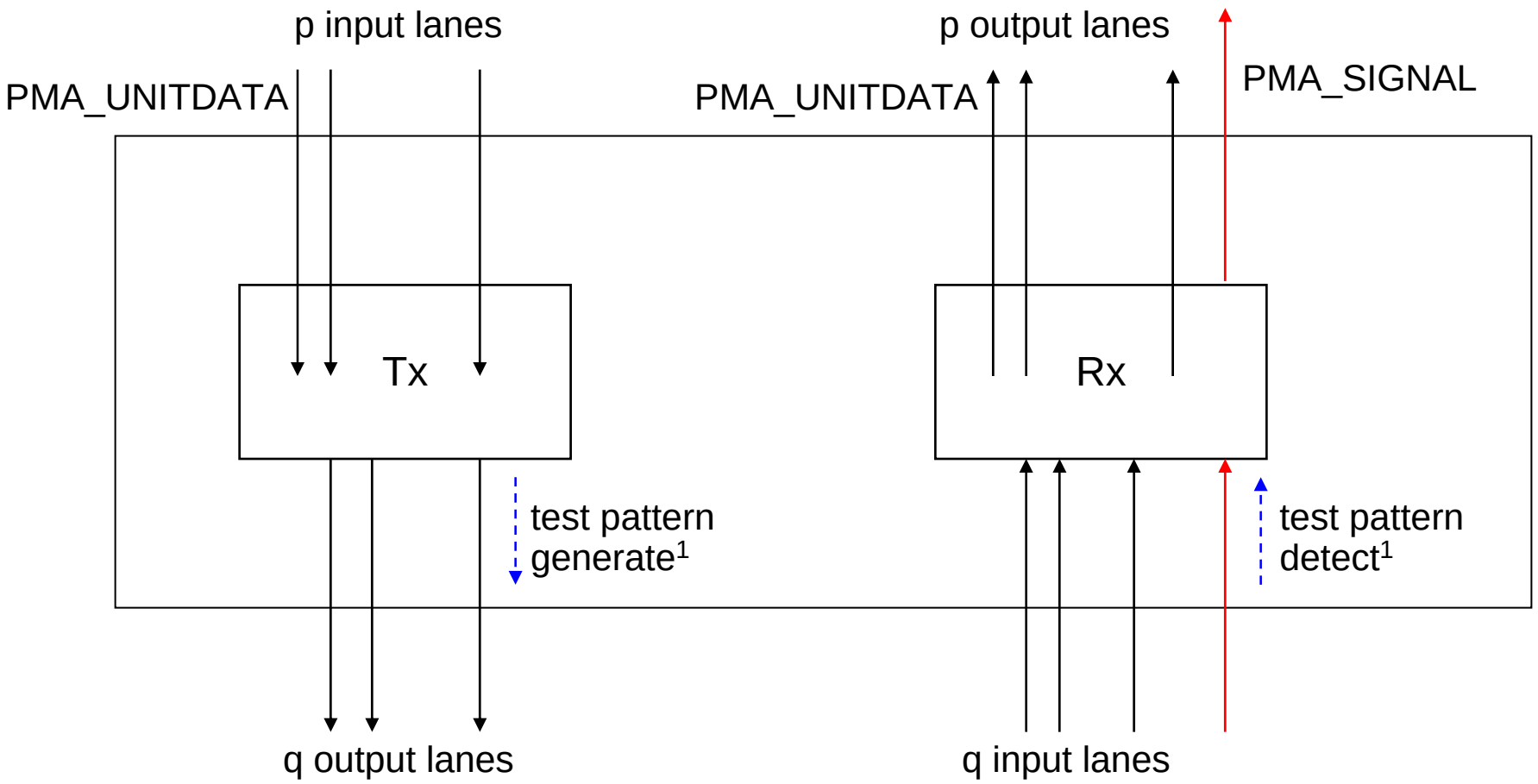
[1]If adjacent XLAUI/CAUI

PMA B



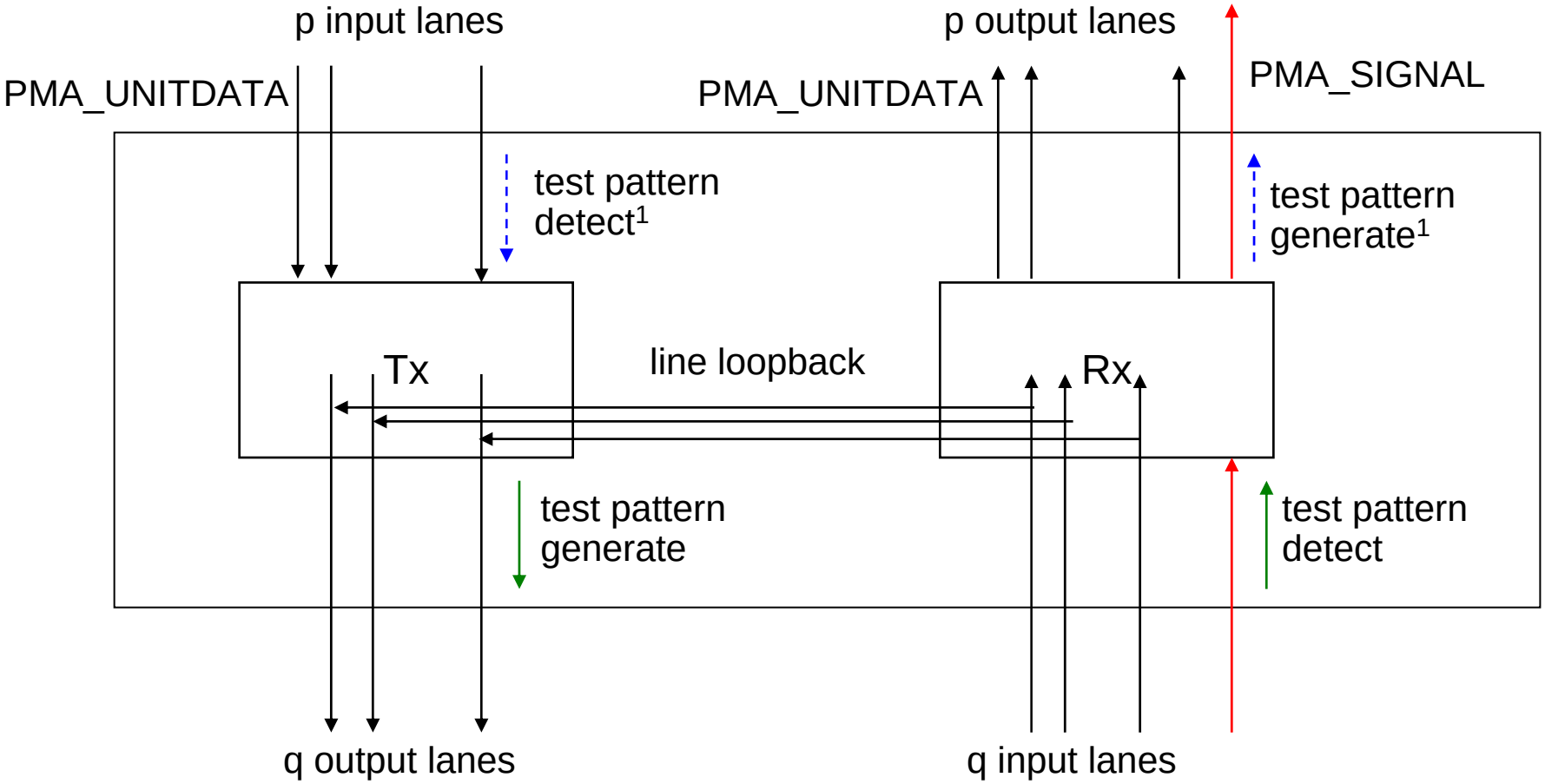
[1]If adjacent XLAUI/CAUI
Add system loopback?

PMA C



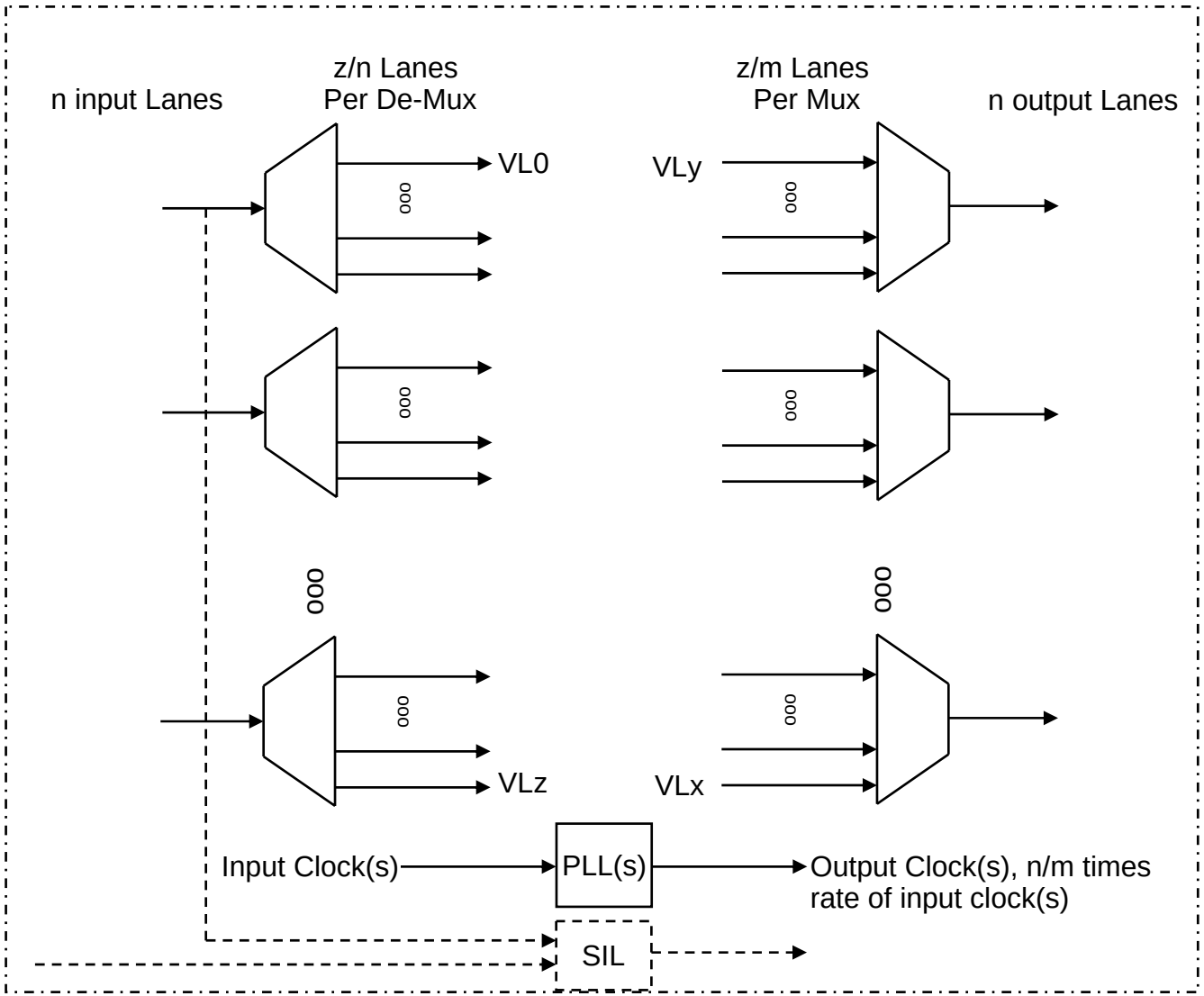
[1]If adjacent XLAUI/CAUI

PMA D



[1]If adjacent XLAUI/CAUI

A Parameterized PMA - Details



All implementations that map every input PCS lane to an output PCS lane position are valid, even if they do not completely demux and remux the PCS lanes