Lane markers for 40GbE

Pete Anslow, Nortel Networks

IEEE P802.3ba, Dallas, November 2008

Introduction

During the review of Draft 0.9 of 802.3ba in Seoul, it was proposed by Piers Dawe to use a different set alignment markers for the 40GbE lanes from the 100GbE lanes.

If this is agreed, this contribution proposes a suitable set of alignment markers for 40GbE based on a section of the $1 + x^{39} + x^{58}$ scrambler output with all zeros input. The markers were chosen so that each byte (M_0, M_1, etc.) is unique for each marker including the 20 100GbE alignment markers. This contribution also presents simulation results that show that these markers will have acceptable properties should a 40Gb serial PHY be introduced in the future.

Proposed alignment markers

Table 82–2—Alignment marker encodings for 40GBASE-R

Lane Number	Encoding[a] $\{M_0, M_1, M_2, M_3, M_4, M_5, M_6, M_7\}$
0	0x90, 0x76, 0x47, 0x3e, 0x6f, 0x89, 0xb8, 0xc1
1	0xf0, 0xc4, 0xe6, 0x63, 0x0f, 0x3b, 0x19, 0x9c
2	0xc5, 0x65, 0x9b, 0x33, 0x3a, 0x9a, 0x64, 0xcc
3	0xa2, 0x79, 0x3d, 0xd8, 0x5d, 0x86, 0xc2, 0x27

[a]Each octet is transmitted LSB to MSB

Simulations

Using these new alignment codes, all possible combinations of virtual lanes for serial 40GbE were then re-analysed to find the worst cases for Baseline Wander (BW) and Clock Content (CC). These searches also included lane delays of -16 through to +16 bits for each VL.
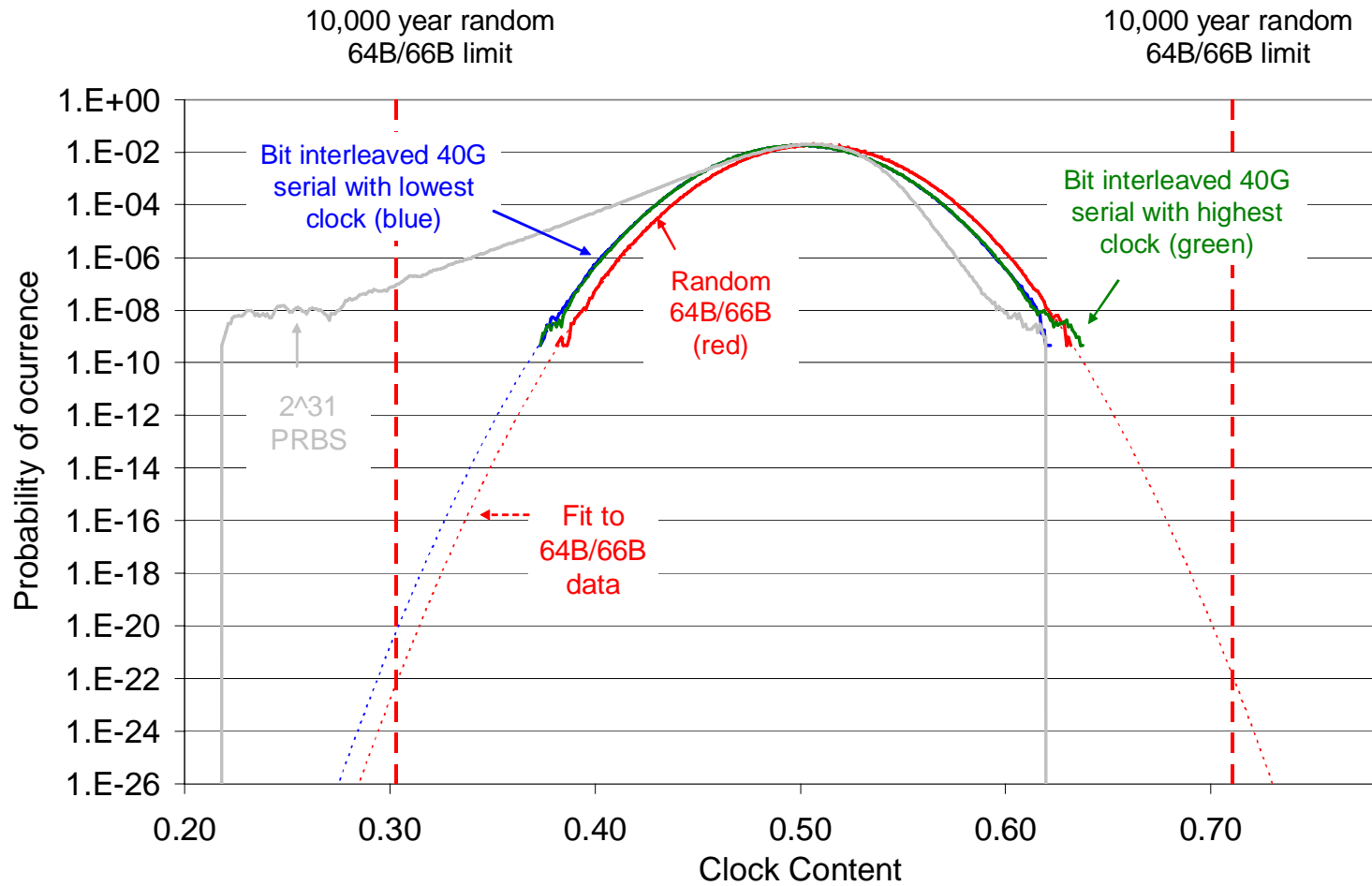
The worst case VL combinations and delays were then used to generate the worst case PDFs for 40 GbE serial with random data.

For more explanation of these plots and definitions of terms see
anslow_01_0108.pdf

Baseline wander PDF for 40GbE serial
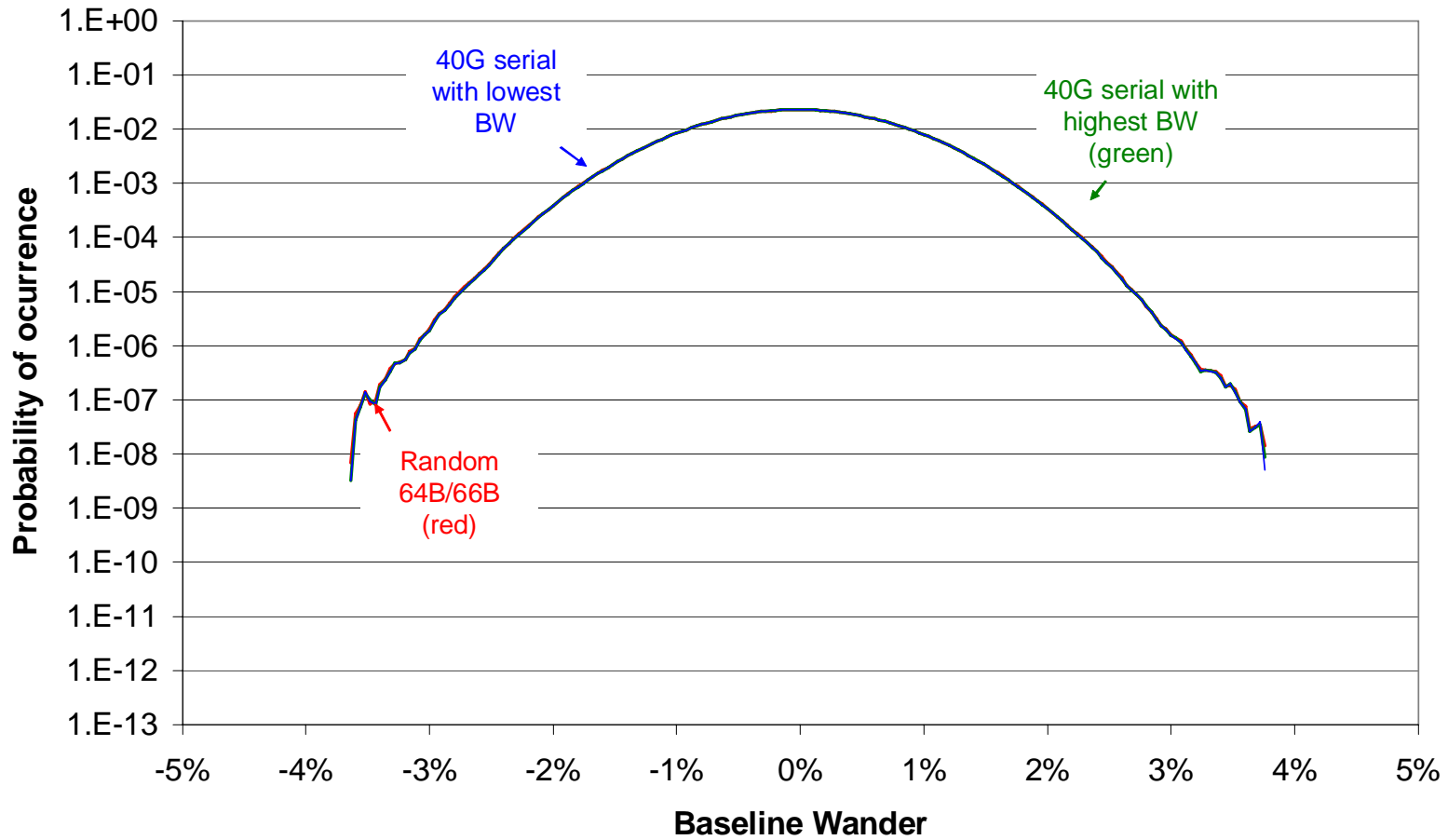
Clock content PDF for 40GbE serial

Conclusion

If it is agreed to use a different set of alignment markers for the 40GbE lanes from 100GbE then a suitable set of markers for 40GbE is proposed.

These markers have been analysed for baseline wander and clock content for the possible future case of a 40GbE serial PHY with acceptable results.

Thanks!

Pete Anslow,
Nortel Networks