Refinement of xAUI Specifications

IEEE 802.3ba

Dallas

Nov 11 2008

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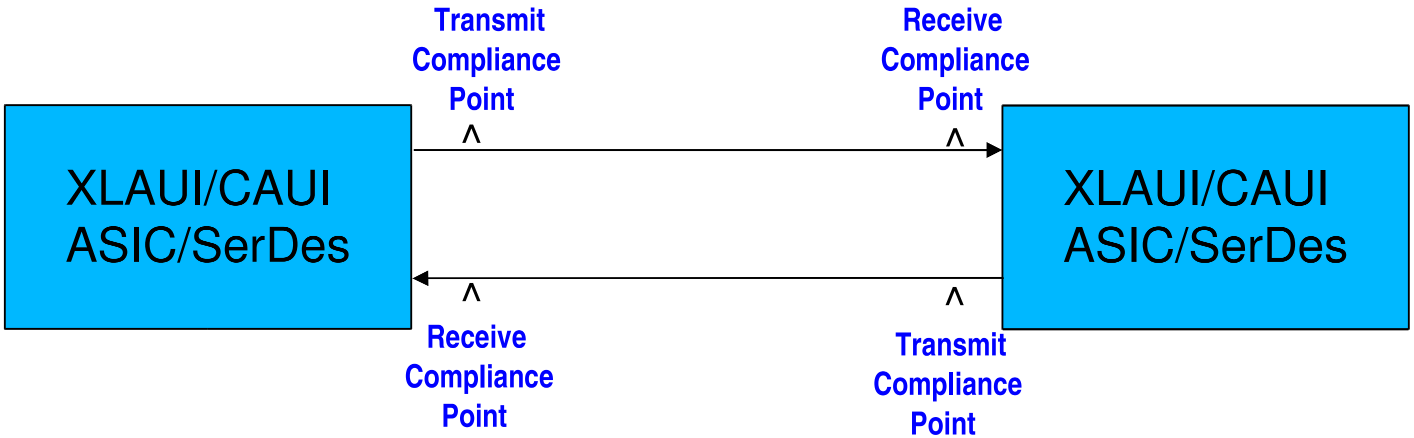
Key Items Require Further Work

- **PMA to TP1 and TP4 to PMA loss**
- **How to test transmitter for compliance**
- **What should be the channel definition s-parameters, ..**
- **How to test receiver for compliance**
- **Jitter Methodology**

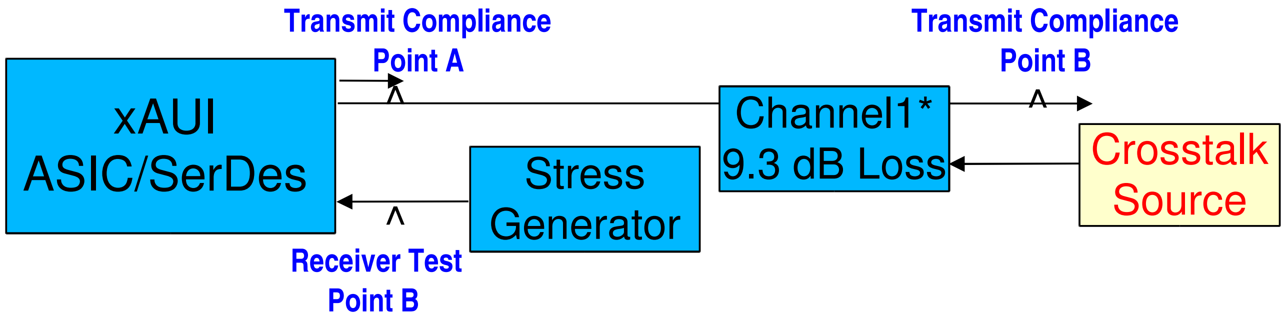
xAUI Compliance Point

- **Chip to chip with 10 dB loss at Nyquist**
  - May include one connector
  - Keep it simple and lets not get wrapped in specific implementations which will change over time!
- **Where should the transmit and receive compliance point be?**
  - At the ball?
  - Allow short PCB trace to allow some form of high speed connector?



xAUI Test Methodology Chip-Chip

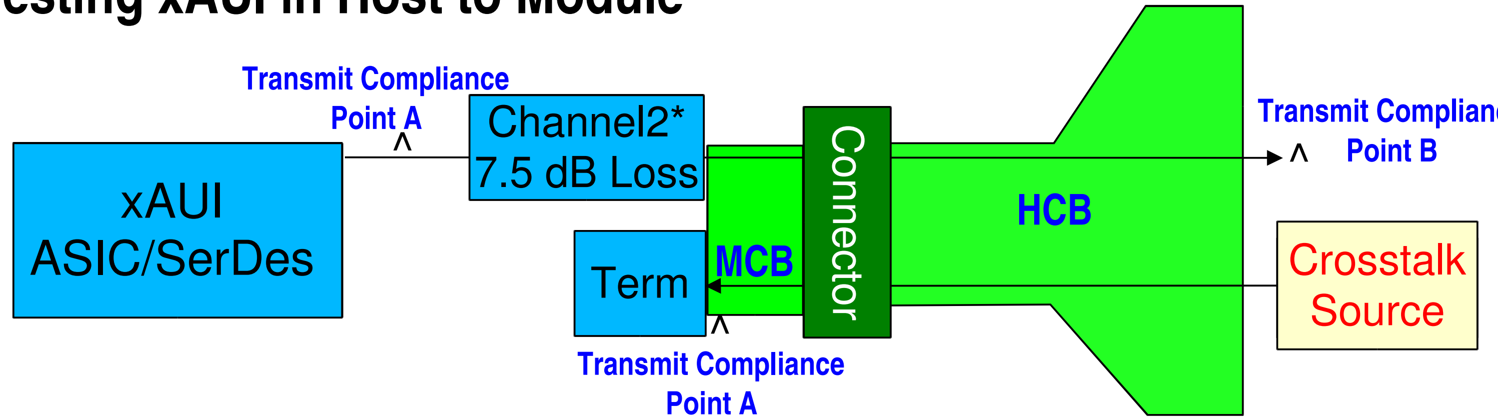
- **Testing xAUI chip to chip applications**



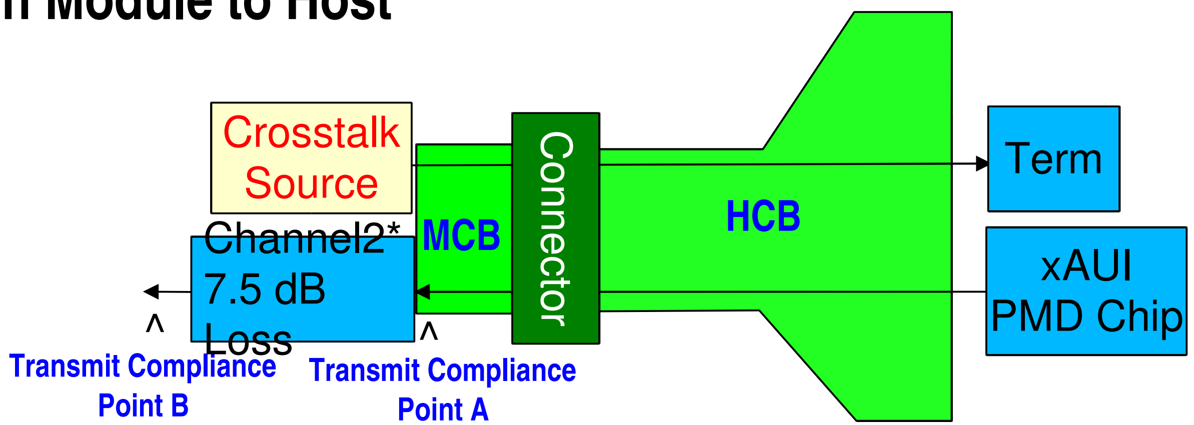
Channel1 Loss = 10 dB – xAUI DUT loss = 9.3 dB

xAUI Test Methodology Chip-Module

- **Testing xAUI in Host to Module**



- **Testing xAUI in Module to Host**



Channel2 loss ~ 10 dB – PMD_Chip(DUT) loss – HCB Loss – Connector loss = 10 – 0.7 – 1.3 – 0.5= 7.5 dB
TX Compliance Point A from PMD chip measured by replacing Channel 2 with MCB with max loss of 0.7 dB
Min channel loss= MCB loss + Connector loss + HCB loss + PMD chip loss = 0.7 + 0.5 + 1.3 + 0.7 dB = 3.2 dB

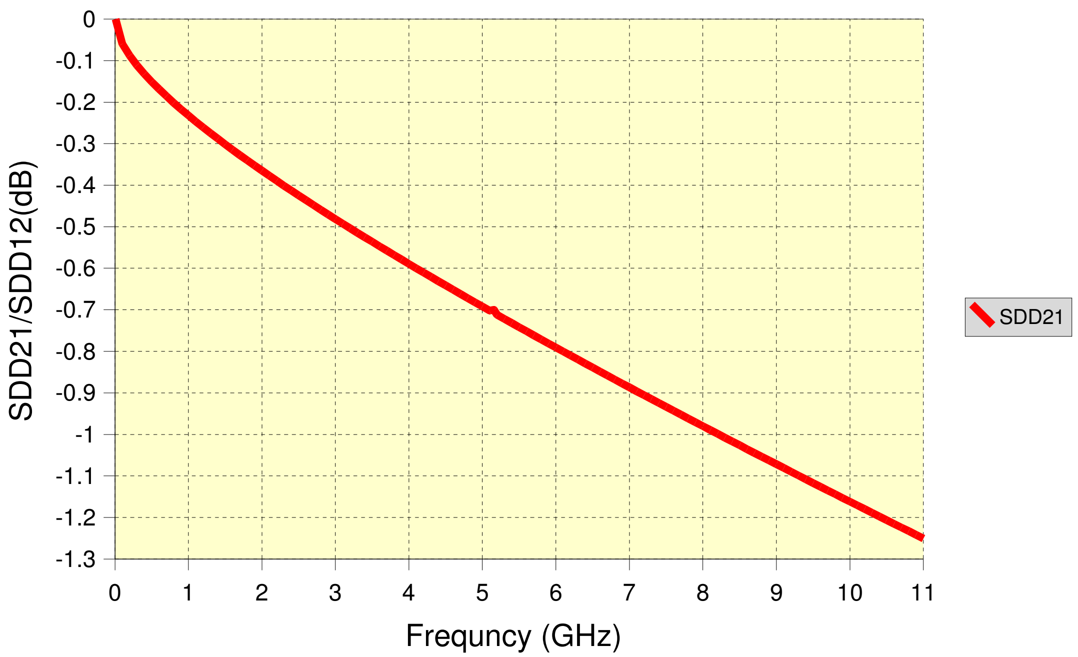
What Can be Summarized About the Test Points

- **xAUI applications are chip-chip and chip-module.**
- **Test point should be based on chip-chip application with point A and B.**
  - As illustrated the test point A and B can be applied for chip-module applications but there is no reason to define various applications of xAUI in the 802.3ba.
- **Following definition simplifies the test points**
  - Point A – Min channel loss
    - Chip to chip = 0.7 dB
    - Chip to module = 2.5 dB
  - Point B – Max channel loss
    - Chip to chip = 9.3 dB (10 dB – 0.7 dB (DUT loss))
    - Chip to Module = 7.5 dB
- **xAUI far end compliance is verified with b2b and a channel with 10 dB loss at Nyquist (including the loss of test boards).**

PMA Chip to TP1 or TP4 Loss

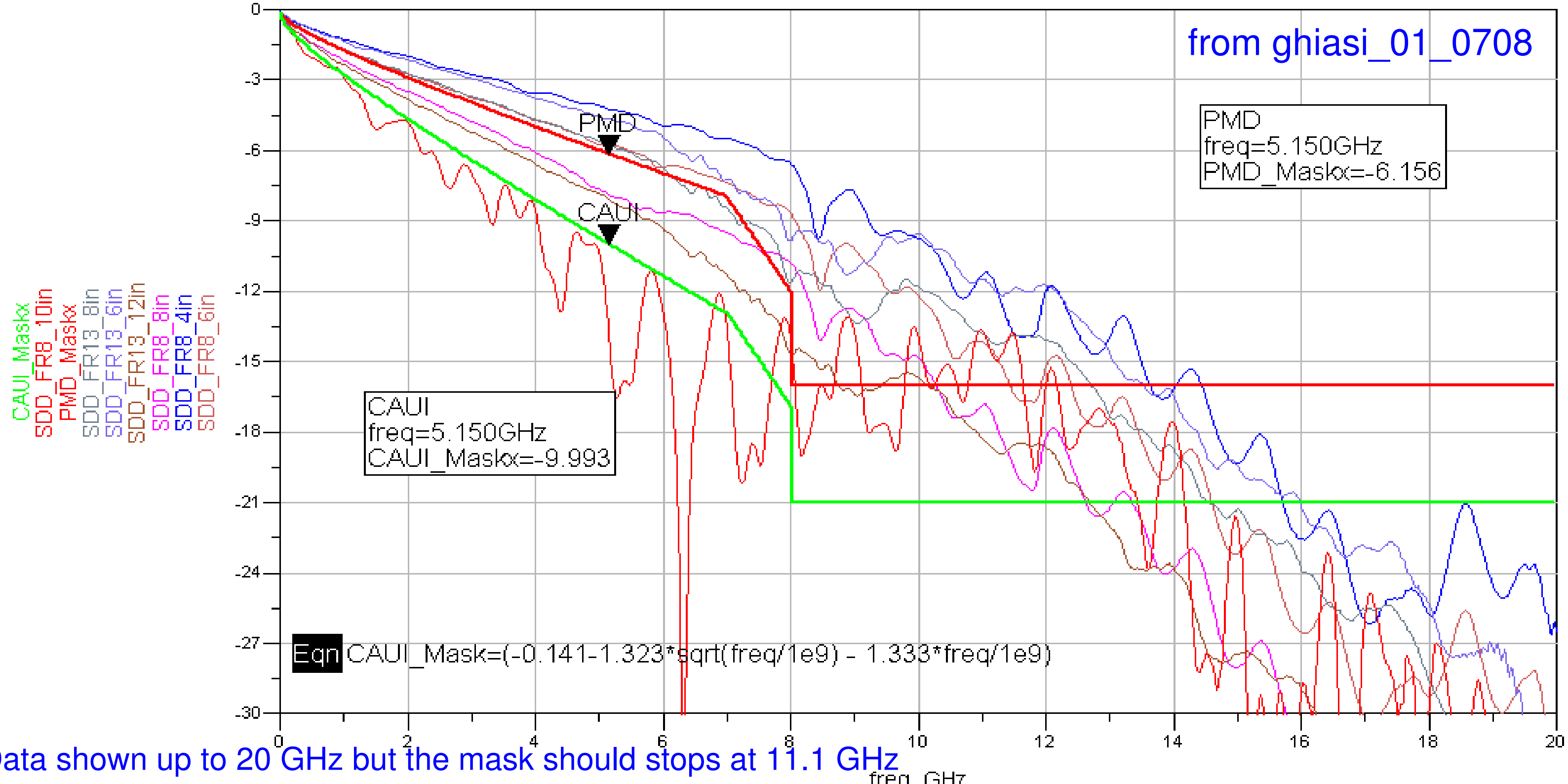
- **It has been suggested 3” of PCB traces for xAUI to TP1 or TP4 which is unacceptable even on low loss material which will mask the measurement and reduce accuracy.**
- **xAUI PMA chip to TP1 or TP4 loss <=0.7 dB at Nyquist 0.2 dB higher than SFP+.**
  - **About 40 mm trace length in Rogers 4350B material with RF connector.**

$$SDD21(dB) = (-0.0007 - 0.1684\ x sqrt(f) - 0.0617\ x f)$$



XLAUI/CAUI Channel SDD21

- **The 10 dB channel was created by cascading s4p file of a 2nd PCB with 2 dB loss at Nyquist with the 8"which is adding some ripple.**
- **Option for including compliance channel are include s4p, include SDD21, or fitted complex function to the SDD21.**



Data shown up to 20 GHz but the mask should stops at 11.1 GHz

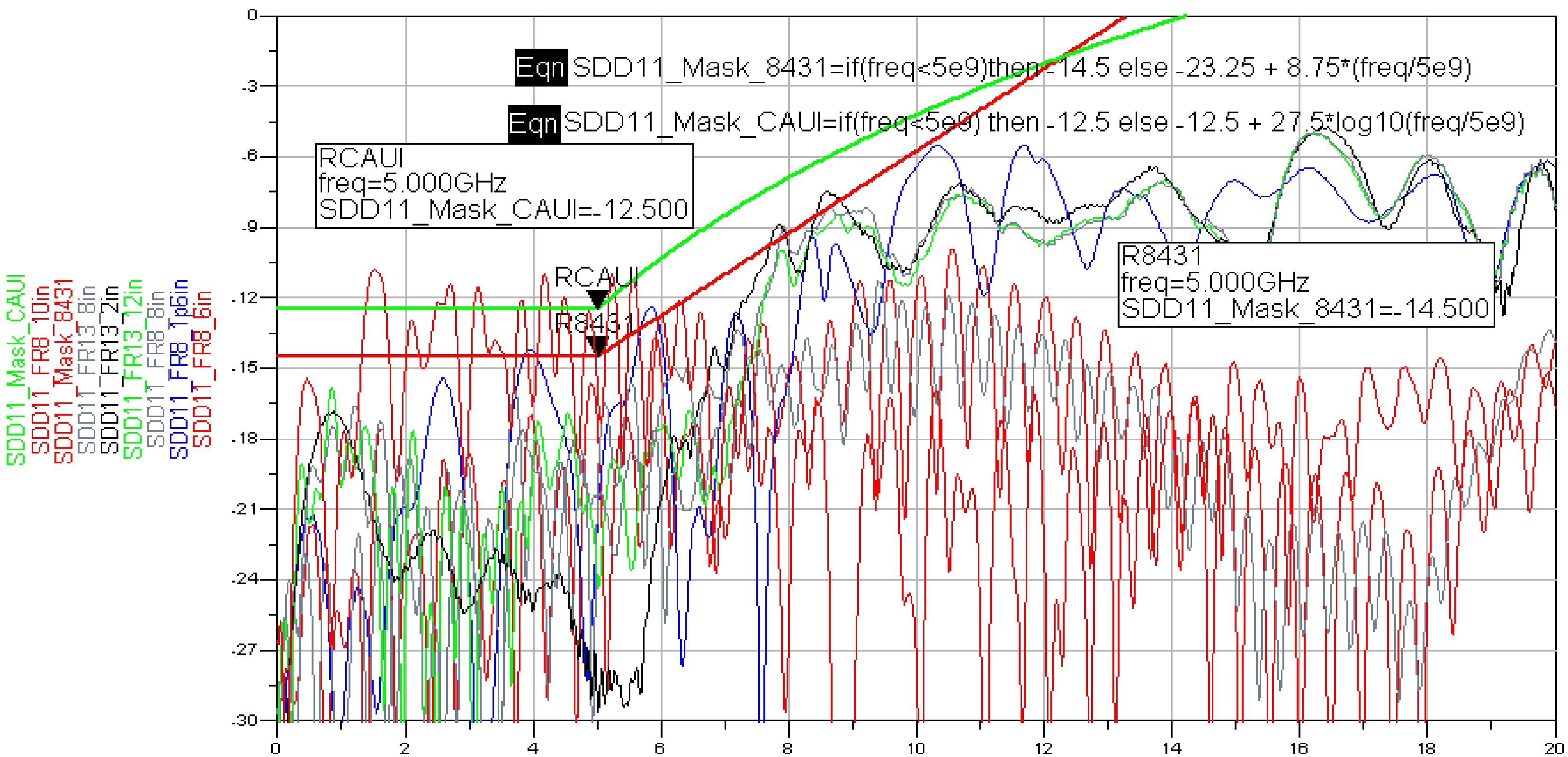
Eqn CAUI_Maskx=if(freq<7e9) then (-0.141-1.323*sqrt(freq/1e9) - 1.33*freq/1e9) elseif (freq<=8e9) then 15.1-4.*freq/1e9 else -21 endif

Eqn PMD_Maskx=if(freq<7e9) then (-0.108-0.845*sqrt(freq/1e9) - 0.802*freq/1e9) elseif (freq<=8e9) then 20-4*freq/1e9 else -16 endif

XLAUI/CAUI Channel SDD11

- **The cascaded channel with 10 dB loss at Nyquist its SDD11 is degrades about 3 dB.**
- **How to include the return loss effect in the far end compliance?**
  - **Propose to use a channel with return loss at the limit.**

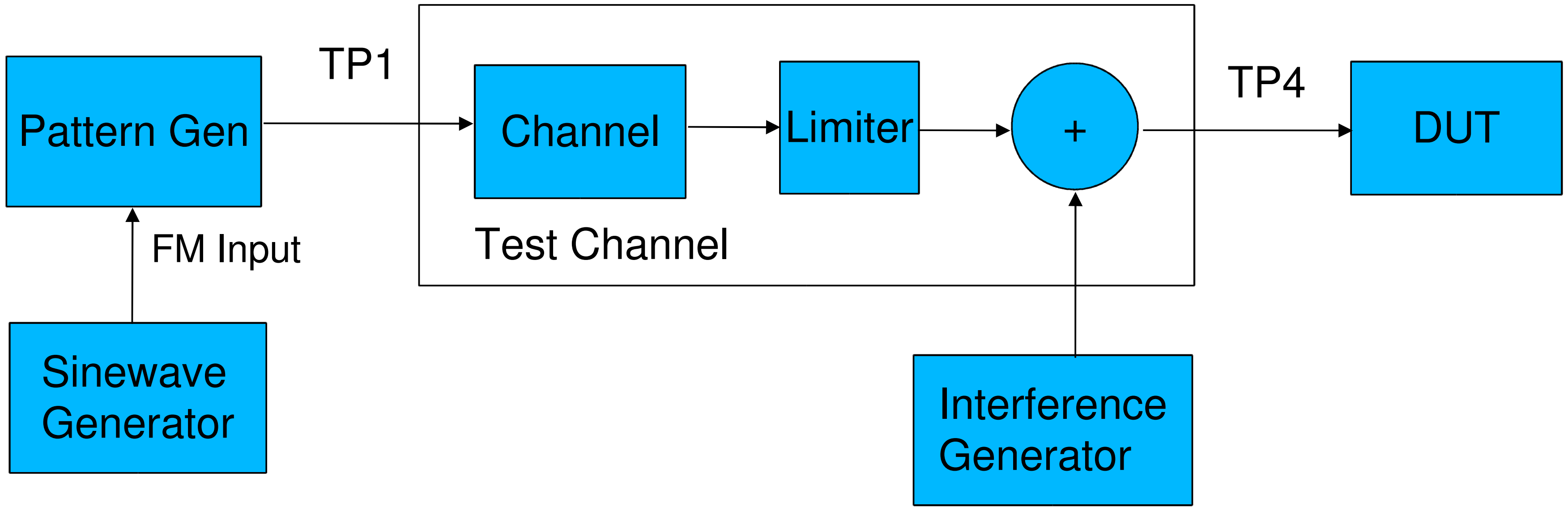
from ghiasi_01_0708



Data shown up to 20 GHz but the mask should stops at 11.1 GHz

xAUI Receiver Interference Testing

- Leverage KR interference model with XLAUI/CAUI longest channel.
- The set-up
  - SJ as defined by Fig 83A-8
  - TP1 set to max UJ
  - Add a channel with 10 dB loss at Nyquist
  - Adjust pre-emphasis till 99% jitter J2 of 0.42 UI achieved at TP4
  - Turn on the interference generator till 1E-15 TJ value reached.



Jitter Methodology

- Use of MJSQ if the jitter PDF is not dual-dirac often results in DJ values which much smaller than high probability jitter BER<1E-2.
- In the case of xAUI the problem is much simpler as DJ is not used for the receiver specifications.
  - SFP+ just after 1 year of investigation replaced DJ at TP4 with 99% probability.
- In xAUI DDJ and DDPWS captures the high probability jitter effect without the DJ baggage
  - Keep TJ the same
    - TJ is tested with PRBS31 or valid 64B/66B signal
  - Replace DJ of 0.17 UI with DDJ of 0.16UI and add DDPWS with value of 0.12 UI.
    - DDJ and DDPWS are tested with PRBS9

Jitter Methodology cont.

- What is non-EQJ
  - non-EQJ=TJ – ISI (1st order HPF) = RJ + DDPWS + PJ + ISI (higher order ISI)
- It has been suggested non-EQJ Jitter for the receiver should be removed to allow more implementation flexibility.
  - non-EQJ of 0.42 UI leaves 0.2 UI for residual ISI which was helpful with XFI receiver which did not have pre-emphasis
- For robust CDR operation high probability jitter must be limited.
  - non-EQJ require measurement of 1st order ISI which is difficult
  - The total jitter @BER of 1E-2 will limit the high frequency jitter and can be directly measured.
  - Replace non-EQJ with (TJ-ISI)=0.42 UI with 99% probability J2=0.42 UI.

Updating nAUI TX and RX Jitter

Table 83A–1—Transmitter characteristics

Parameter	Value	Units
Signalling speed per lane (range)	10.3125 GBd +- 100 ppm	GBd
Unit interval nominal	96.96969697	ps
Single-ended output voltage range maximum minimum	 4.0 –0.4	 V V
Maximum Differential Output Voltage, peak-to-peak	760	mV
Maximum Termination Mismatch at 1MHz	5	%
Maximum Output AC Common Mode Voltage, RMS	15	mV
Minimum Output Rise and Fall time (20% to 80%)	24	ps
Differential Output S-parameters	(see "Equation 83A-1")	dB
Common Mode Output S-parameters	(see "Equation 83A-2")	dB
Maximum Total Jitter[a] @1E-15	0.32	UI
Maximum ~~Deterministic~~ Jitter[b] DDJ	0.17 0.16	UI
Transmitter eye mask definition X1[c]	0.16	UI
Transmitter eye mask definition X2[c]	0.38	UI
Transmitter eye mask definition Y1[c]	190	mV
Transmitter eye mask definition Y2[c]	380	mV

[a] Total Jitter Measurement Methodology defined in section 83A.4.3
[b] Deterministic Jitter Measurement Methodology defined in section 83A.4.3
[c] Transmitter Eye Mask illustrated in Figure 83A–5

add DDPWS = 0.12 UI

Table 83A–2—Receiver characteristics

Parameter	Value	Units
Signalling speed per lane (range)	10.3125 GBd +- 100 ppm	GBd
Unit interval nominal	96.96969697	ps
Minimum Differential Input Voltage, p-p	See receiver eye mask definition	mV
Maximum Input AC Common Mode Voltage, RMS	20	mV
Minimum Input Rise and Fall Time (20% to 80%)	24	ps
Differential Input S-parameters	(see "Equation 83A-3")	dB
Differential Common Mode Input Conversion S-parameters	(see "Equation 83A-4")	dB
Maximum Total Jitter[a] @1E-15	0.62 0.64	UI
Maximum non-EQ Jitter (TJ-ISI)[b] TJ (1E-2)	0.42	UI
Receiver eye mask definition X1[c]	0.31	UI
Receiver eye mask definition X2[c]	0.5	UI
Receiver eye mask definition Y1[c]	45	mV
Receiver eye mask definition Y2[c]	425	mV

Max 1σ (RJ) =1 ps (RJ/16)