0.1 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that may provide control and status information for and about the PCS. Mapping of MDIO control variables to PCS control variables is shown in Table TBD. Mapping of MDIO status variables to PMD status variables is shown in Table TBD.

Table 88–1—MDIO/PMD control variable mapping

MDIO control variable	PCS register name	Register/ bit number	PCS control variable
Reset	Control register 1	3.0.15	reset
Loopback	Control register 1	3.0.14	Loopback
Transmit test-pattern enable	10/40/100GBASE-R PCS test-pattern control register	3.42.3	tx_test_mode
Receive test-pattern enable	10/40/100GBASE-R PCS test-pattern control register	3.42.2	rx_test_mode

Table 88–2—MDIO/PMD status variable mapping

MDIO status variable	PCS register name	Register/ bit number	PCS status variable
10/40/100GBASE-R and 10GBASE-R recieve link status	10/40/100GBASE-R and 10GBASE-T PCS status 1 register	3.32.12	PCS_status
10/40/100GBASE-R and 10GBASE-T PCS high BER	10/40/100GBASE-R and 10GBASE-T PCS status 1 register	3.32.1	hi_ber
Lane x lock	Multi-lane BASE-R PCS alignment status register 1 and 2	3.50.7:0 3.51.11:0	block_lock<x>
Lane x aligned	Multi-lane BASE-R PCS alignment status register 3 and 4	3.52.7:0 3.53.11:0	am_lock<x>
PCS lane alignment status	Multi-lane BASE-R PCS alignment status register 1	3.50.12	align_status
BER	10/40/100GBASE-R and 10GBASE-T PCS status 2 register	3.33.13:8	ber_count
Errored blocks	10/40/100GBASE-R and 10GBASE-T PCS status 2 register	3.33.7:0	errored_block_count
Test-pattern error counter	10/40/100GBASE-R PCS test-pattern error counter register	3.43.15:0	test_pattern_error_count