4x10G vs Serial 40G SerDes Maturity and Cost

IEEE 802.3ba
Interim Meeting

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List of Supporters

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- Kieth Conroy – AMCC
- Howard Frazier - Broadcom
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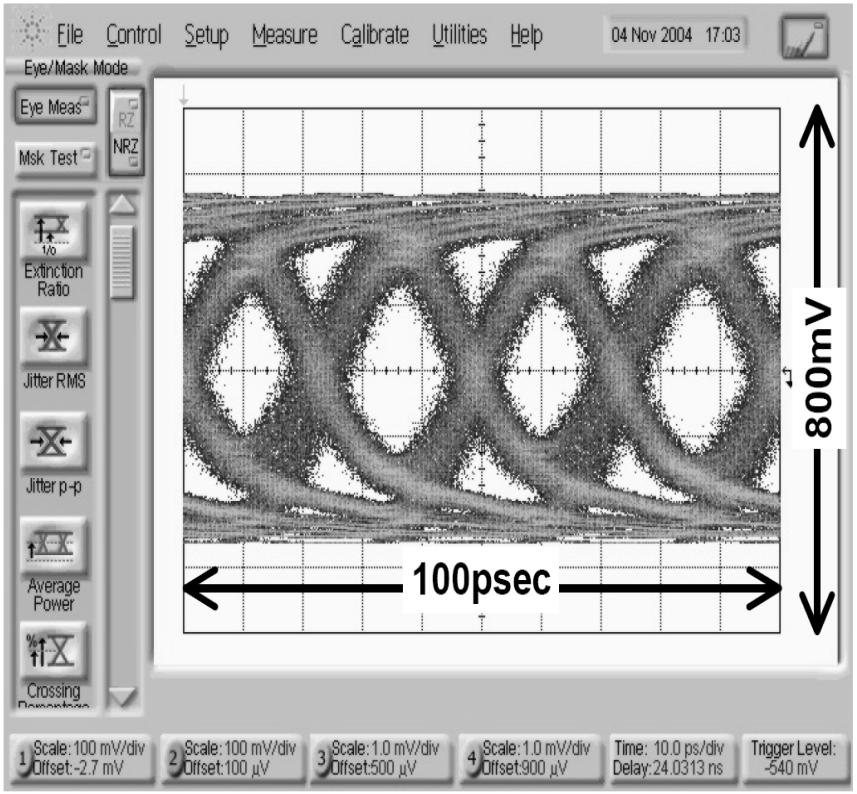
- Ryan Latchman – Gennum
- Drew Perkins - Infinera
- Rick Rabinovich – Alcatel-Lucent
- Stephen Trowbridge - Alcatel-Lucent
- Siddharth Sheth – NetLogic Micro
- Jim Tavacoli – Santur

10 GbE Historical Perspective

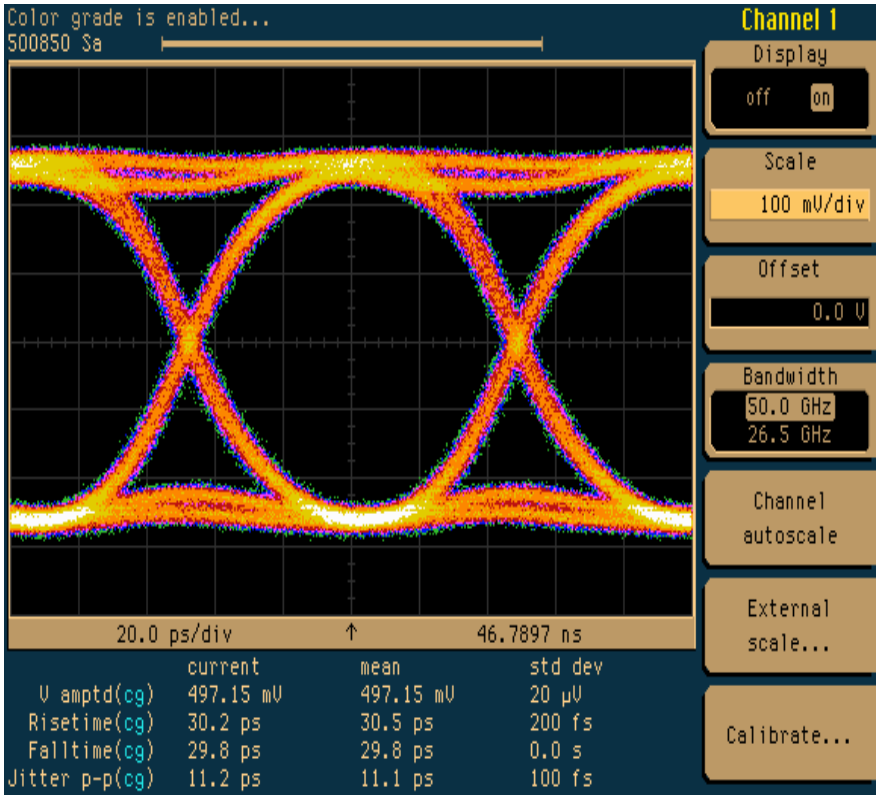
- 10GbE Call for interest March 1999
- 10GbE study group started on June 1999
- Newport Communication introduced 1st CMOS OC-192 production XCVR July 1999
- Initial serial PMD proposal presented in IEEE HSSG Nov 1999
- IEEE 802.3ae had their 1st task force meeting March 2000
- Newport Communication was acquired by Broadcom Aug 2000
- Broadcom introduces 1st 10 GbE XAUI-serial XCVR May 2001 based on CMOS
- In IEEE 802.3 our standards are designed for high volume, low cost implementation, and are based on nearly mature technology
  - Production 10G CMOS was available when 802.3ae defined serial PMDs.

Comparisons of 40G Research Serdes vs 1st 10G Production Serdes

- 4x1 Mux, ISSCC 2005 8.2 K. Kanada
- 90 nm CMOS 20 GHz clock supplied externally, state of the art!



- Newport Com/Broadcom 0.18 um CMOS XAUI XCVR 2000.
- Production grade XCVR!

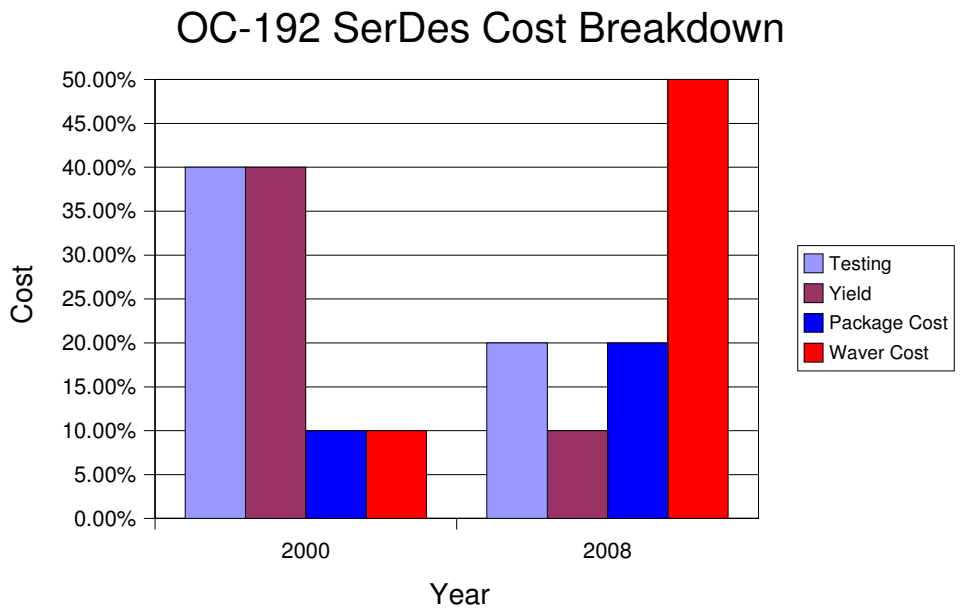


What Does Low Risk and Available Mean?

- traverso_02_0708 state the following:
  - "CMOS; Low Power CDR (73 mW) Is Available Today(*1)"
  - "45 nm CMOS is sufficient for 40 Gb/s Driver"
- (Ref 1) T. Toifle, et. al., D12-3, ISSCC2007
  - Excellent state of the art work!
  - 65 nm CMOS-SOI
  - 8x oversampled DLL with 10GHz clock externally supplied
  - No mux or 40G driver implemented (just de-mux)
  - For an open eye input the de-mux had only 11 ps eye opening!
    - Not enough jitter margin for practical transmitter + Optical TX + Fibre + Optical RX
- Ref 1 on traverso_02_0708 does not use standard CMOS and does not implement a mux/driver!
  - Uses SOI and only implement a de-mux.

OC-192 SerDes Cost Breakdown

- **Primary driver for cost reduction**
  - **Moving from very expensive bench top testing every part to ATE**
  - **Yield increase**
- **Secondary driver for cost reduction**
  - **Package cost**
  - **Wafer cost**
- **Other factor contributing to cost reduction**
  - **Availability of SerDes from 3-5 suppliers**
  - **Standard CMOS**
  - **Volume**



OC-768 SerDes Cost

- **Currently OC-768 SerDes cost more than 100x an OC-192 SerDes!**
- **Our estimate is that OC-768 SerDes cost dominated by yield and testing!**
  - **It has been claimed that replacing GPPO with SMT package will result in 87% cost reduction!**
    - **How is this possible when the package is only 10% of the SerDes cost?**
    - **How is this possible when the cost is dominated by yield and testing?**
- **The LGA package may complicate at speed testing and lower the yield!**

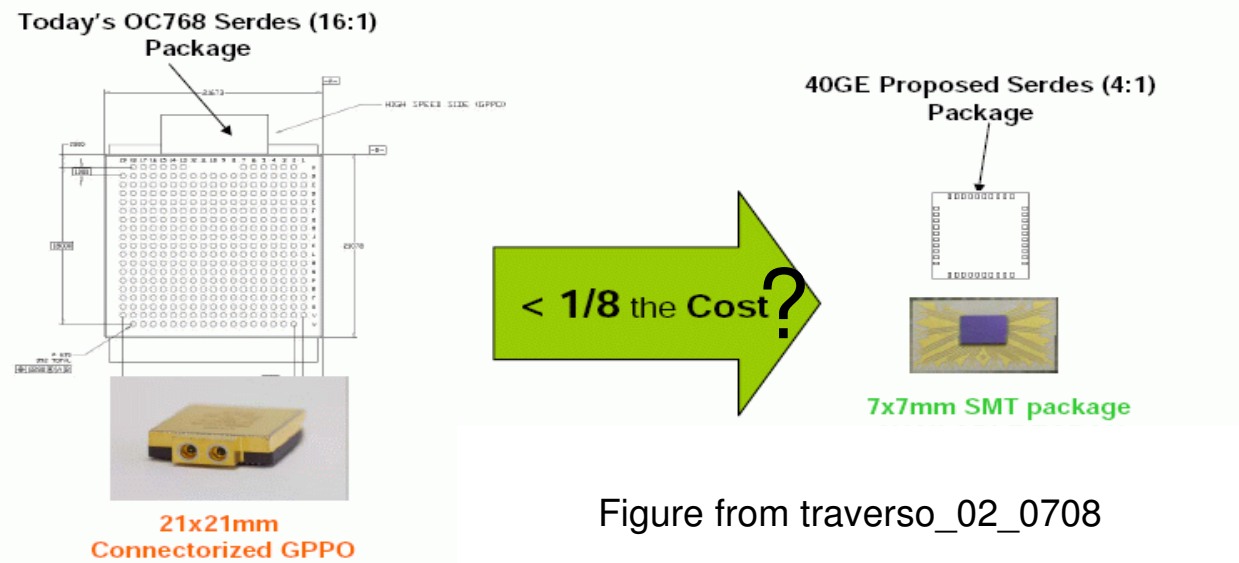
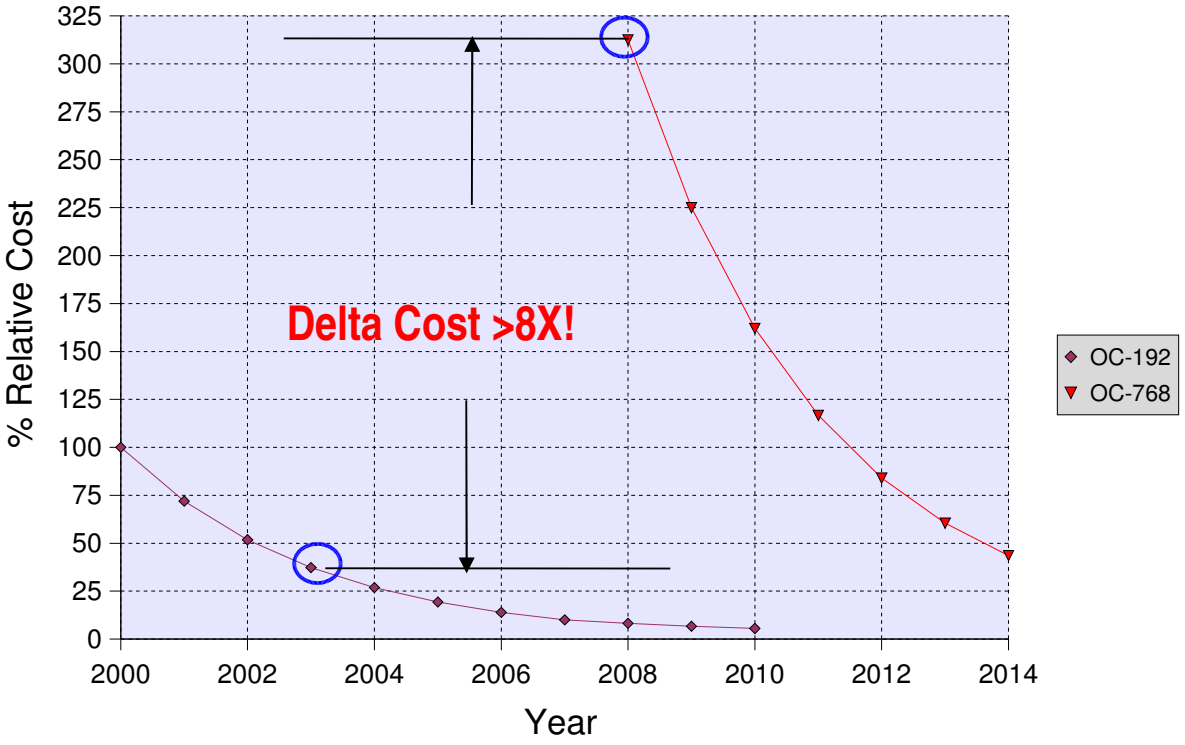


Figure from traverso_02_0708

Cost Comparison of OC-192 vs OC-768 SerDes

- **Current OC-768 SerDes cost is >8x the OC-192 SerDes cost in 2003, both 6 years from product introduction!**
  - **Product shipment for OC-192 started in ~1997**
  - **Product shipment for OC-768 started in ~2002**



* OC-768 cost was assumed to follow 28% YoY cost reduction

Summary

- **Even after 6 years after OC-768 product introduction it has not yet followed OC-192 volume curve or cost reduction.**
  - **As result of test equipment cost, yield, skilled labor, test time, signal integrity, packaging, and requirement for esoteric processes.**
  - **ITU SG-15 is actually considering alternative modulation scheme with better spectral efficiency and lower Baudrate (2x20 or 4x10 Gigabud).**
- **Even if 87% cost reduction is possible by using LGA/BGA package for the 40G SerDes, the 40G Mux/De-Mux still will cost 6x the cost of quad CDR (see latchman_01_0908)!**
- **IEEE 802.3ba should standardize 4x10G SMF PMD based on maturity, low cost, technology reuse, and synergy with 4x10G/10x10G MMF PMD.**