Two Markets, Two Channels, Two PHYs

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- Mark Nowell - Cisco
- Shimon Muller – Oracle
- Adam Healey – LSI
- Steve Carlson – High Speed Design

Outline

- Motivation
- Summary of prior presentations
- Introduction to the current suite of presentations
- Summary
- Proposal for new objectives

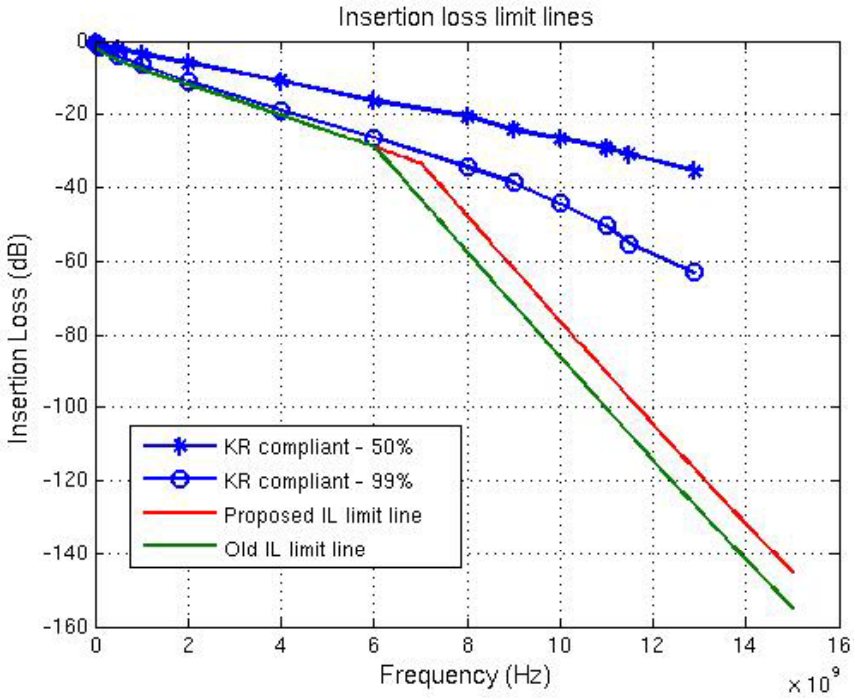
Motivation

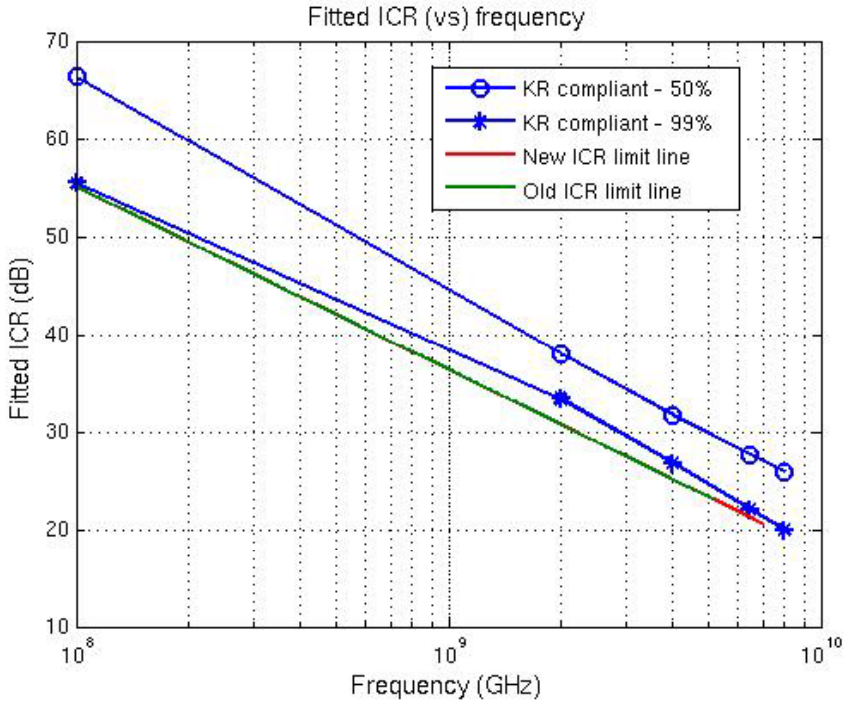
- Material presented to the SG and TF demonstrates that there are two markets for 100 Gb/s Ethernet on backplanes
  - High end network equipment and HPC
  - Blade server/ATCA/mid range network equipment
- In order to achieve Broad Market Potential, the standard should serve both markets

Prior presentations

- Market potential
  - H. Frazier, V. Parthasarathy, *Study of 100 Gb/s on 40GBASE-KR4 channel*, parthasarathy_01_0111.pdf
  - D. Chalupsky, *Broad Market Potential and Economic Feasibility of the 100Gb Backplane and Cu Cable Solutions for the Volume Blade and Rack Server Markets*, chalupsky_02_0311.pdf
  - M. Brown, *100G backplane PHY: NRZ and PAM4*, brown_01_0911.pdf
  - K. Lusted, D. Chalupsky, *The Case for Legacy Channels*, lusted_01a_1111.pdf
  - B. Patel, J. D'Ambrosia, *Blade Servers and the Relative Cost Impact of Material*, dambrosia_02a_1111.pdf
- Channel characteristics
  - V. Parthasarathy, R. Mellitz, *Rough channel targets for 4 x 25 Gb/s operation on existing backplanes*, parthasarathy_02_0511.pdf
  - H. Frazier, et al, *Characteristics of Installed Backplane Channels*, frazier_01_0911.pdf
  - V. Parthasarathy, H. Frazier, *Channel Characteristics at 12.5 GHz*, parthasarathy_01a_1111.pdf
- Technical Feasibility
  - V. Parthasarathy, et al, *Feasibility of 100 Gb/s Operation on Installed Backplane Channels*, parthasarathy_01a_0511.pdf
  - A. Ran, *Time-domain SNR analysis on contributed channels*, ran_01a_0511.pdf
  - Z. Hatab, *SNR Budget Analysis for 25 Gb/s over Backplane Channels*, hatab_01_0511.pdf
  - Z. Wang, C. Chen, *Feasibility of 100G-KR FEC*, wang_01_0511.pdf
  - S. Bhoja, et al, *FEC Proposal for 100G KR*, bhoja_01_0911.pdf
  - D. Dabiri, *Enabling Improved DSP Based Receivers for 100G Backplane*, dabiri_01_0911.pdf
  - S. Bhoja, et al, *Precoding proposal for PAM-4 Modulation*, parthasarathy_01_0911.pdf
  - K. Lusted, et al, *A Preliminary Proposal for PAM-4 TX Specification*, bliss_01a_0911.pdf
  - D. Dabiri, *Performance Analysis of PAM4 Receivers over Long Backplane Channels*, dabiri_01_11.pdf
  - A. Ran, *Time-domain performance analysis for recently contributed channels using PAM-4 signaling*, ran_01a_1111.pdf
  - Z. Hatab, *Output Voltage Proposal for PAM-4 Transmitter*, hatab_01a_1111.pdf

Previously proposed limits to 7 GHz





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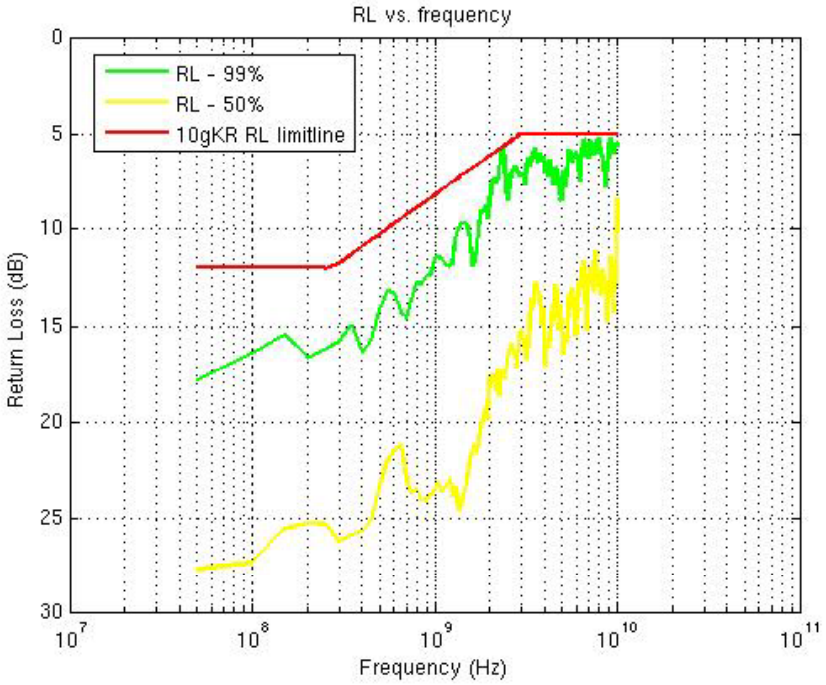
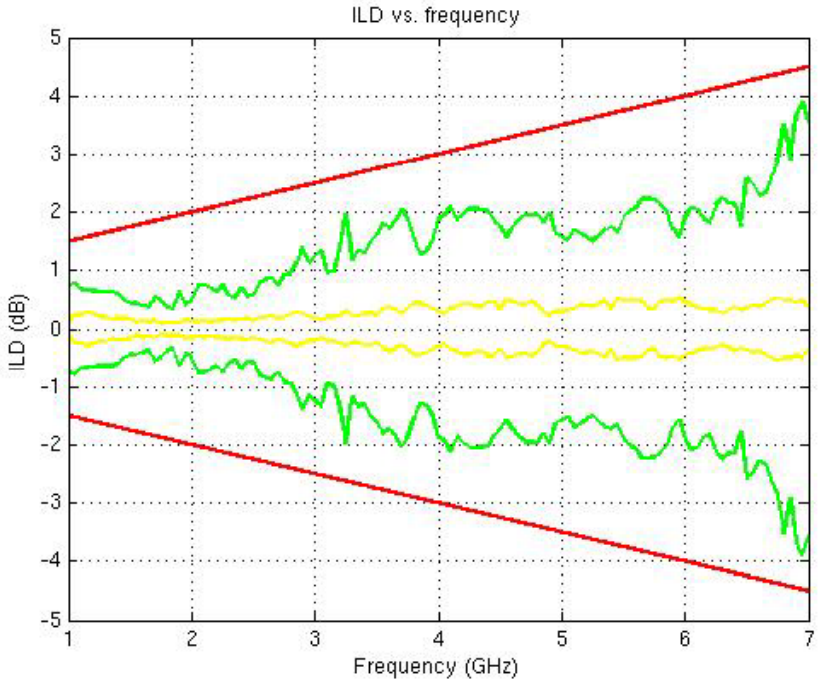




Current suite of presentations

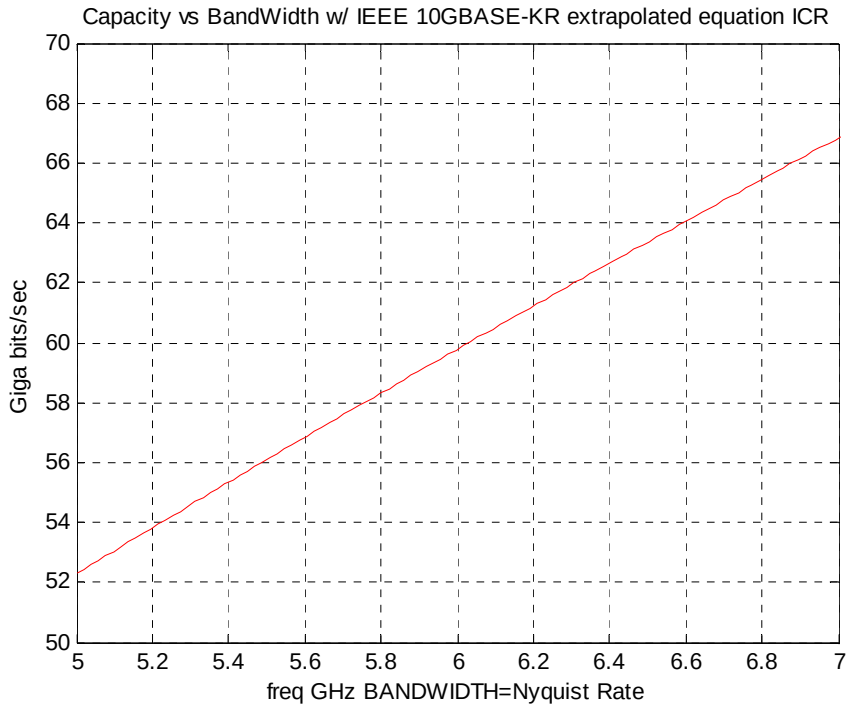
- Presentations delivered at this meeting will
  - Demonstrate that there are two market opportunities that require two sets of channel specifications and two PHY specifications
  - Provide a detailed proposal for PAM4-based transmitter framing
  - Evaluate the performance of three distinct PAM4 receiver architectures, all of which are compatible with the proposed transmitter framing

Current suite of presentations

- Mark Nowell – System Vendors: Thoughts on Two PHY Approach
- Rich Mellitz - 100 Gb/s Backplane/PCB Ethernet: Two Channel Model and Two PHY proposal
- Matt Brown – PAM4 Transmitter Framing
- Adee Ran – PAM4 Analog Receiver Performance
- Dariush Dabiri – PAM4 MLSE Termination and Receiver Performance
- Vasu Parthasarathy – PAM4 digital receiver feasibility and performance

Summary

- Exploit the capacity of the channel by using well-known signaling techniques



Summary

- The case for two markets, two channels, and two PHYs is well established
- The feasibility of a PAM4 PHY is well established
- The path forward is clear

Proposed objectives

- Define a 4 lane PHY for operation over backplanes with a loss of <= 33 dB at 7 GHz
- Define a 4 lane PHY for operation over backplanes with a loss of <= 35 dB at 12.9 GHz