FEC Options

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Introduction

- Over the past few meeting cycles many different FEC options have been presented, this paper attempts to narrow down the pool into a few optimum options, and then makes a few recommendations

- Considerations are:
  - Effective gain (includes raw FEC coding gain and burst error behavior)
  - Logic complexity and power
  - Achievable latency
  - Over-clocking requirements

- A strawman proposal is shown for an NRZ backplane FEC

- The FEC processing flow is updated

0% Over-clocking Options

- Option 1 has the good gain, latency < 100ns and has an acceptable complexity; option 2 is similar with a little more complexity but with better MTTFPA; Option 5a is interesting since it has an associated ½ rate code (umbrella code)
- All options assume some trans-coding across lanes
- None of these options can handle cross lane correlated error bursts well
- All have an integer reference clock multiplier (RCM = 165)

Option	FEC Code RS(n, k, t, m)	Trans-coding	Effective Gain BER= 10^{-15}	Overall Latency	Total Area (40nm gates)	Total Power	Input BER for 10^{-15} BER	Input BER for 10^{-12} BER
1	RS(528, 514, 7, 10)	512b/514b	4.87 dB	99.4 ns	275k	101 mW	4.68×10^{-6}	2.34×10^{-5}
2	RS(528, 513, 7, 10)	512b/513b	4.87 dB	99.4 ns	285k	105 mW	4.68×10^{-6}	2.34×10^{-5}
3	RS(528, 516, 6, 10)	512b/516b	4.52 dB	96.8 ns	243k	88 mW	1.86×10^{-6}	1.12×10^{-5}
4a	RS(468, 456, 6, 9)	512b/513b	4.51 dB	96.3 ns	197k	72 mW	1.82×10^{-6}	1.23×10^{-5}
4b	RS(234, 228, 3, 9)	512b/513b	2.06 dB	52.9 ns	108k	40 mW	2.39×10^{-10}	9.77×10^{-8}
5a	RS(528,516,6,10)	256b/258b	4.52 dB	90 ns	212k	77mW	1.86×10^{-6}	1.12×10^{-5}
5b	RS(264,258,3,10)	256b/258b	2.35dB	49 ns	113k	41mW	9.12×10^{-10}	1.12×10^{-7}

3% Over-clocking Options

- Option 3 is preferred, it has good gain, latency < 100ns and has less complexity
- All options assume some trans-coding across lanes
- All options can handle very short duration (< 22 bit) cross lane correlated error bursts
- All have an integer reference clock multiplier (RCM = 170)
- Choose a 3% option if you need to correct short duration correlated errors across lanes and/or you need the extra ~1dB of gain

Option	FEC Code RS(n, k, t, m)	Trans-coding	Effective Gain BER= 10^{-15}	Overall Latency	Total Area (40nm gates)	Total Power	Input BER for 10^{-15} BER	Input BER for 10^{-12} BER
1a	RS(544, 514, 15, 10)	512b/514b	6.10 dB	121.5 ns	516k	187 mW		
1b	RS(544, 514, 15, 10)	512b/514b	6.10 dB	100.6 ns	1004k	363 mW		
2a	RS(544, 516, 14, 10)	512b/516b	5.96 dB	118.9 ns	472k	171 mW		
2b	RS(544,516, 14, 10)	256b/258b	5.96 dB	99.6 ns	504k	183 mW		
3	RS(544, 520, 12, 10)	64b/65b	5.62 dB	99.8 ns	364k	133 mW	7.94×10^{-5}	1.91×10^{-4}

6% Over-clocking Options

- None of these seem like good options given that we can get similar gain with a 3% overhead code
- Two options can handle short duration (< 42 bit) cross lane correlated error bursts
- All have an integer clock multiplier
- Several codes have ‘umbrella’ options

Option #	FEC Code RS(n, k, t, m)	Transcoding	Effective Gain	Overall Latency	Total Area (40nm gates)	Total Power	RCM
1a	RS(448, 416, 16, 10)	64b/65b	5.82 dB	99.9 ns	460k	168 mW	175
1b	RS(224, 208, 8, 10)	64b/65b	4.49 dB	52.7 ns	219k	80 mW	175
1c	RS(112, 104, 4, 10)	64b/65b	2.52 dB	29 ns	110k	30 mW	175
2	RS(560, 514, 23, 10)	512b/514b	6.39 dB	110ns	871k	318mW	175
3a	RS(560, 516, 22, 10)	256b/258b	6.31 dB	108ns	816k	298mW	175
3b	RS(280, 258, 11, 10)	256b/258b	5.21 dB	60.4ns	351k	128mW	175

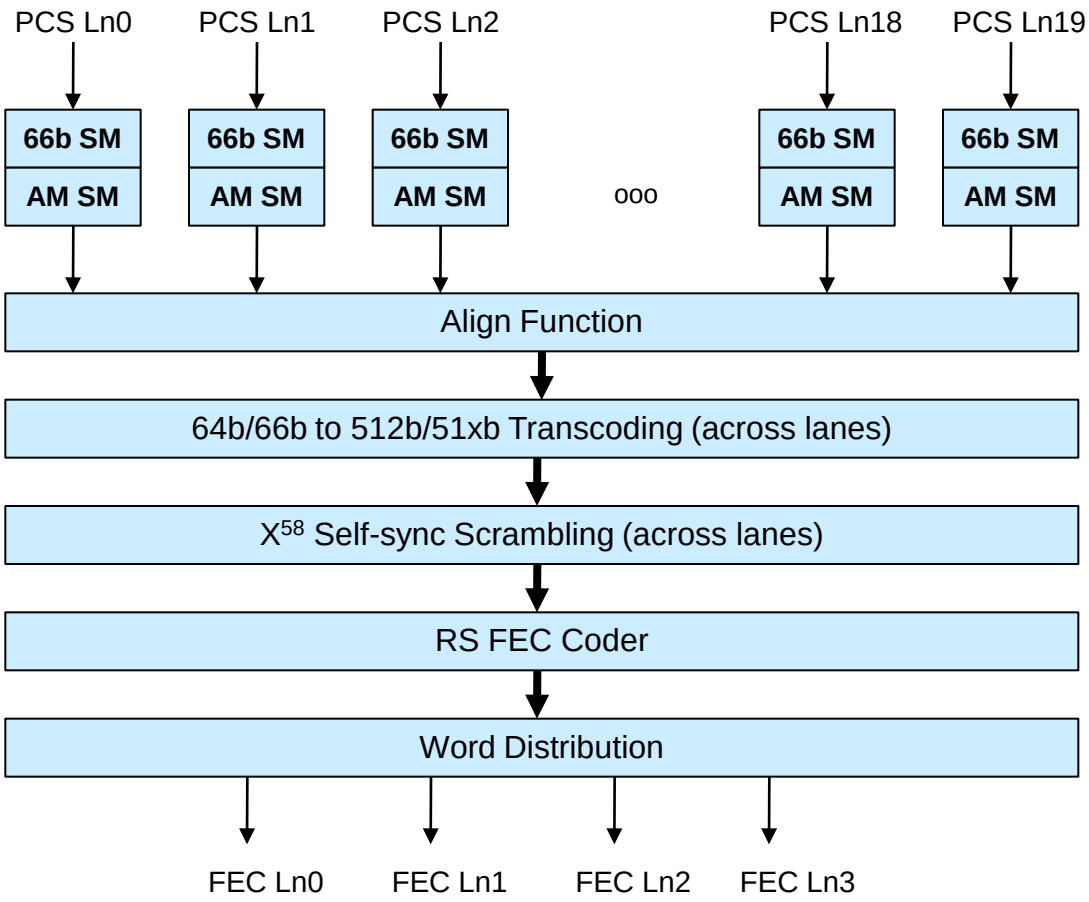
What Use is an Umbrella Code?

- We have shown several options that include ‘Umbrella’ code options
- Each Umbrella code has two or more related codes that scale the complexity/power and latency vs. gain
- How could we take advantage of an umbrella code?
  - Lets look at RS(528,516,6,10) – 4.5dB and RS(264,258,3,10) – 2.3dB as an example
  - The standard could allow:
    - No FEC, 30dB NRZ channel, 10^{-12} BER
    - Light FEC (RS264), 30dB NRZ channel, better than 10^{-15} BER
      - Replaces the function of today’s KR FEC but with very low latency
    - Heavy FEC (RS528), 35dB NRZ channel, better than 10^{-12} BER
  - A single implementation could be designed to decode/correct either related FEC variant

Strawman for Going Forward

- Backplane NRZ:
  - Same lane rate (25.78G) with or without FEC
  - FEC is optional, total channel is 30 dB without FEC, ~35 dB with FEC
    - Actual channel gain vs. FEC gain is TBD
  - Without FEC there is no transcoding (64b/66b encoding)
  - With FEC enabled there is 512b/51xb transcoding
  - FEC use is auto-negotiated
  - Proposed FEC code is option 1, 2 or 5a from the 0% overhead FEC options (~4.xdB of gain)
    - Need to do more work on MTTFPA, transcoding and understand the desirability of a umbrella code
- Backplane PAM4:
  - Being discussed separately
- Copper cable:
  - TBD, depends if we need additional budget

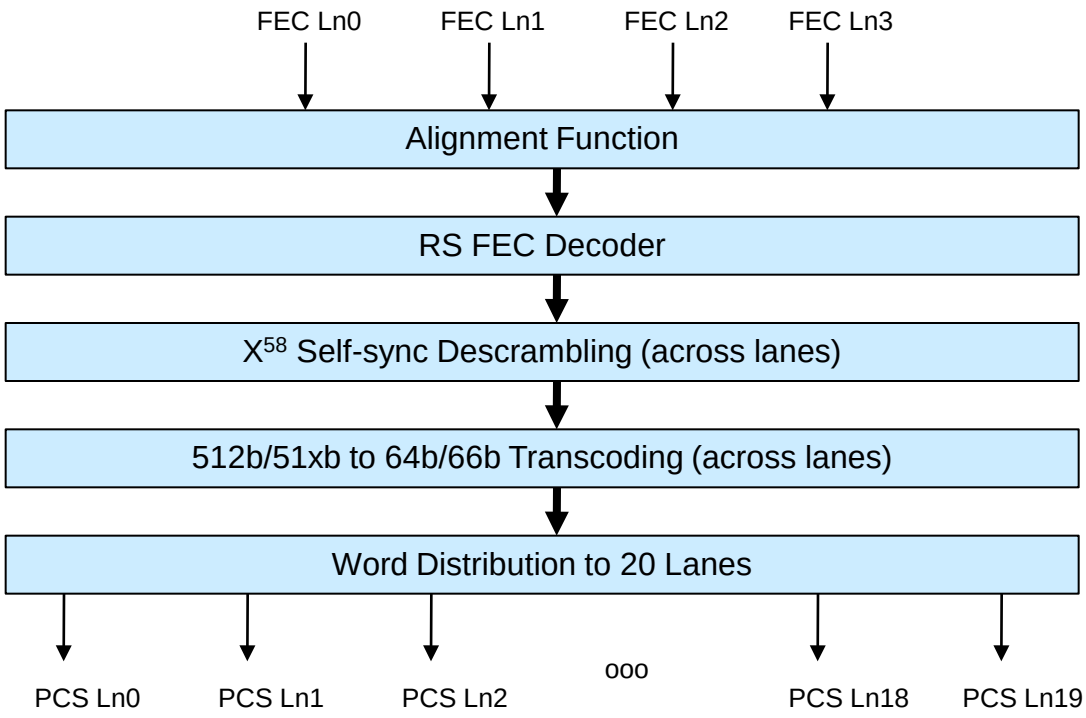
Low Latency TX FEC Architecture



Includes descrambling of 64b/66b stream

Includes all bits except the AM payloads

Low Latency RX FEC Architecture



Thanks!