System Vendors: Thoughts on Two PHY Approach

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  - Beth Kochuparambil – Cisco

Summary

- Attempt to illuminate the technology adoption criteria that a system vendor needs to consider for its product development.
- This presentation is not advocating one PHY proposal over another but is arguing that the industry will be well served by IEEE developing two PHYs specs.
- Both PHY proposals have merit and will have broad market potential

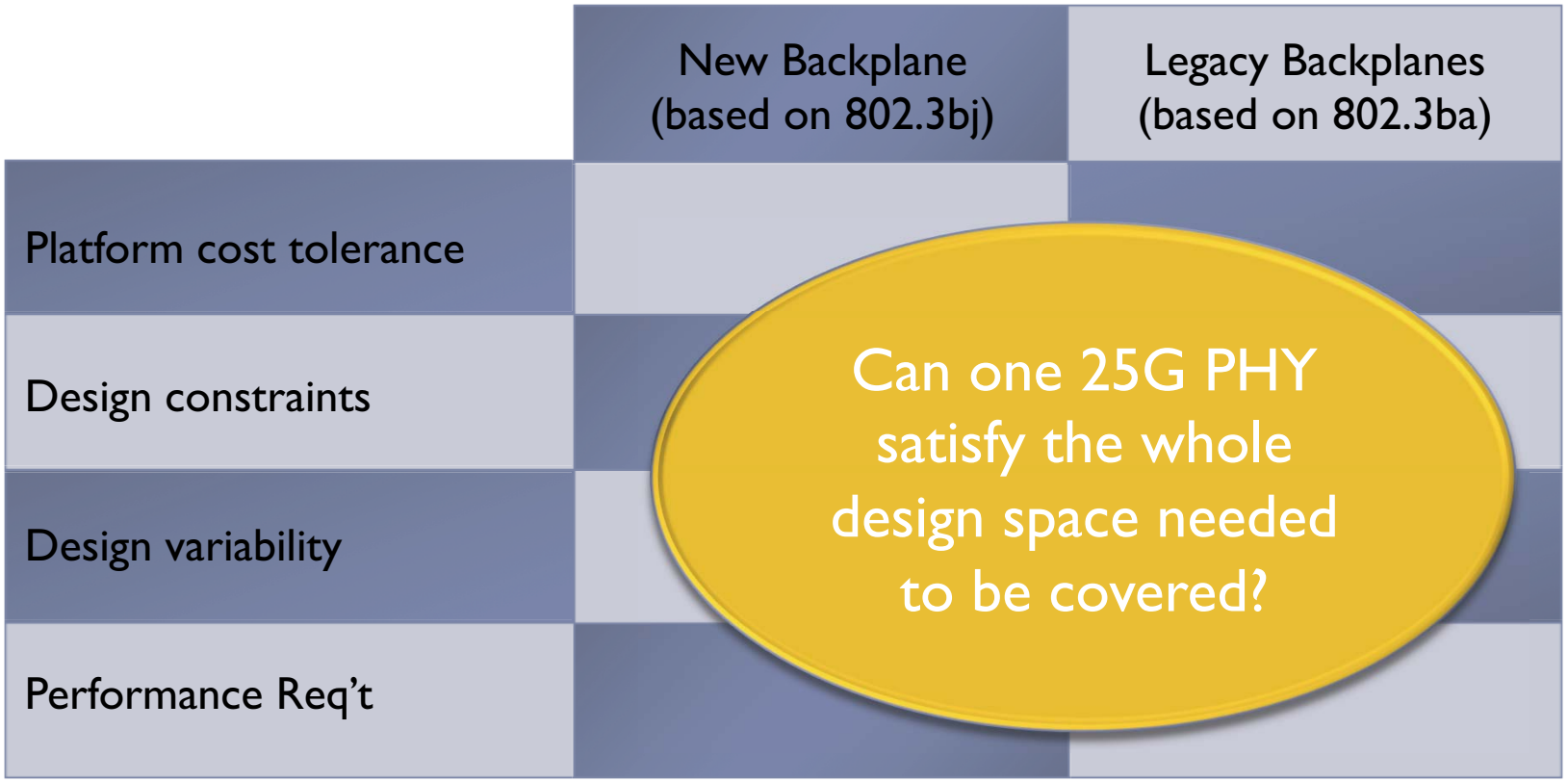
System vendor backplane decision space

- Product breadth
  - Generally a system vendor has numerous product families across product portfolio
  - Switching – low-end access to high-end core
  - Routing – low end access to high-end core
  - Transport – low-end access to high-end core
  - Server – low-end server to high-end blade server
- Wide range of initial design dates
  - Platforms designed up to x years ago could still be being supported. Plus, backplanes are currently being designed or are in planning today. Once design is locked they are unable to be changed for lifetime of platform.
- Backplane is unique
  - Once a platform ships, backplane performance is key factor in EOL decision. No other system component has this level of criticality.

Application Debates

- Applications / Products – lots of different types
  - High-end, mid, low-end
  - Different capacities to support
  - Different cost targets
  - Preventing backplane EOL
- Design considerations
  - Trace length, width, thickness, surface roughness, geometries
  - Boards: board thickness, # of layers, PWB materials / glass / resin, use of counterboring
  - Cost, cost, cost….
  - etc…
- The application, its economics and competitive considerations will dictate the solution

The design space challenge



Design space considerations

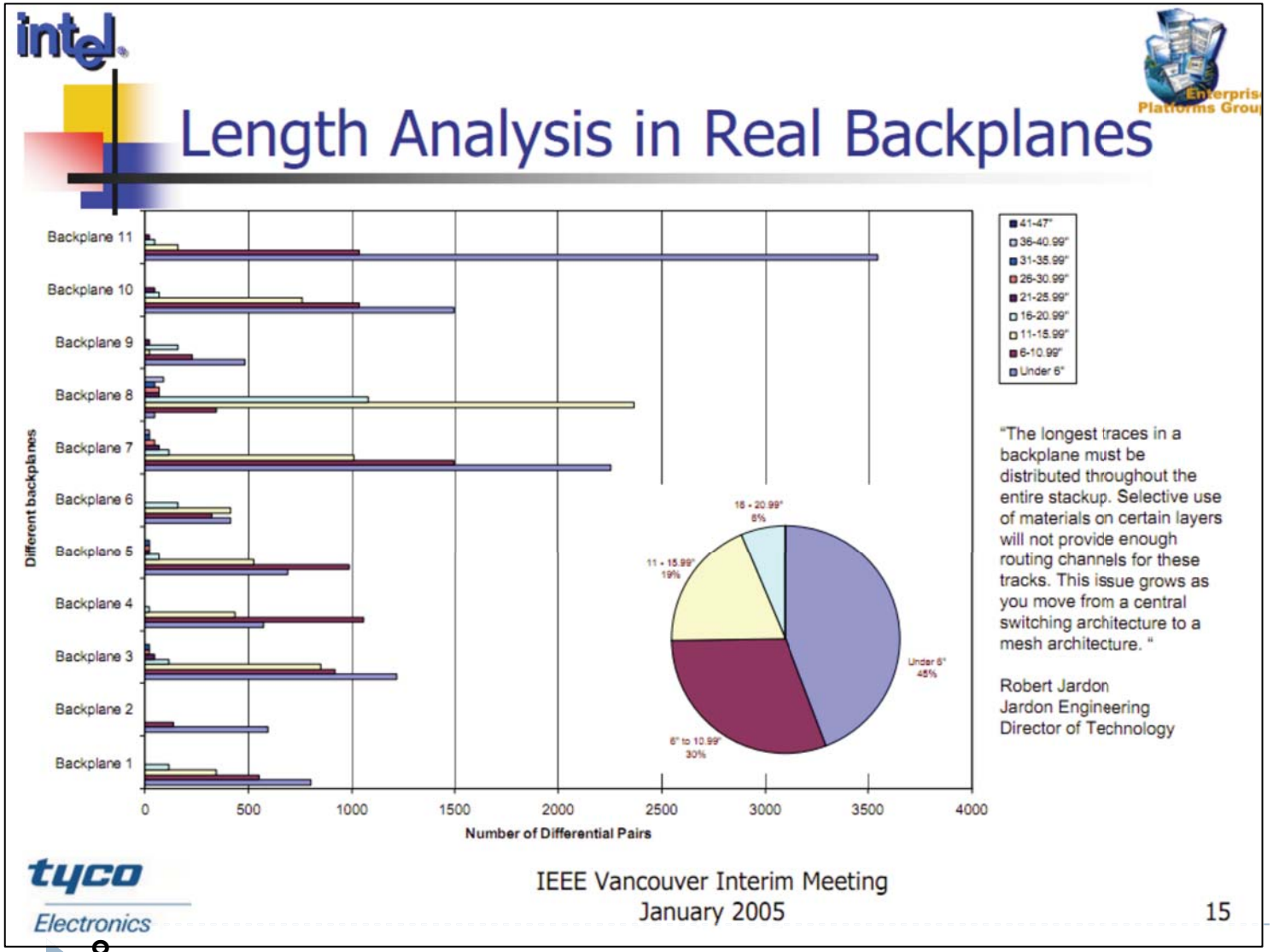
What follows are some examples showing the breadth of issues and considerations that a system vendors works through during a platform development process.

Key point to keep in mind is that for any specific platform, a specific backplane PHY will be optimum…

…but may not be the generic solution for all the platforms that will need a backplane PHY.

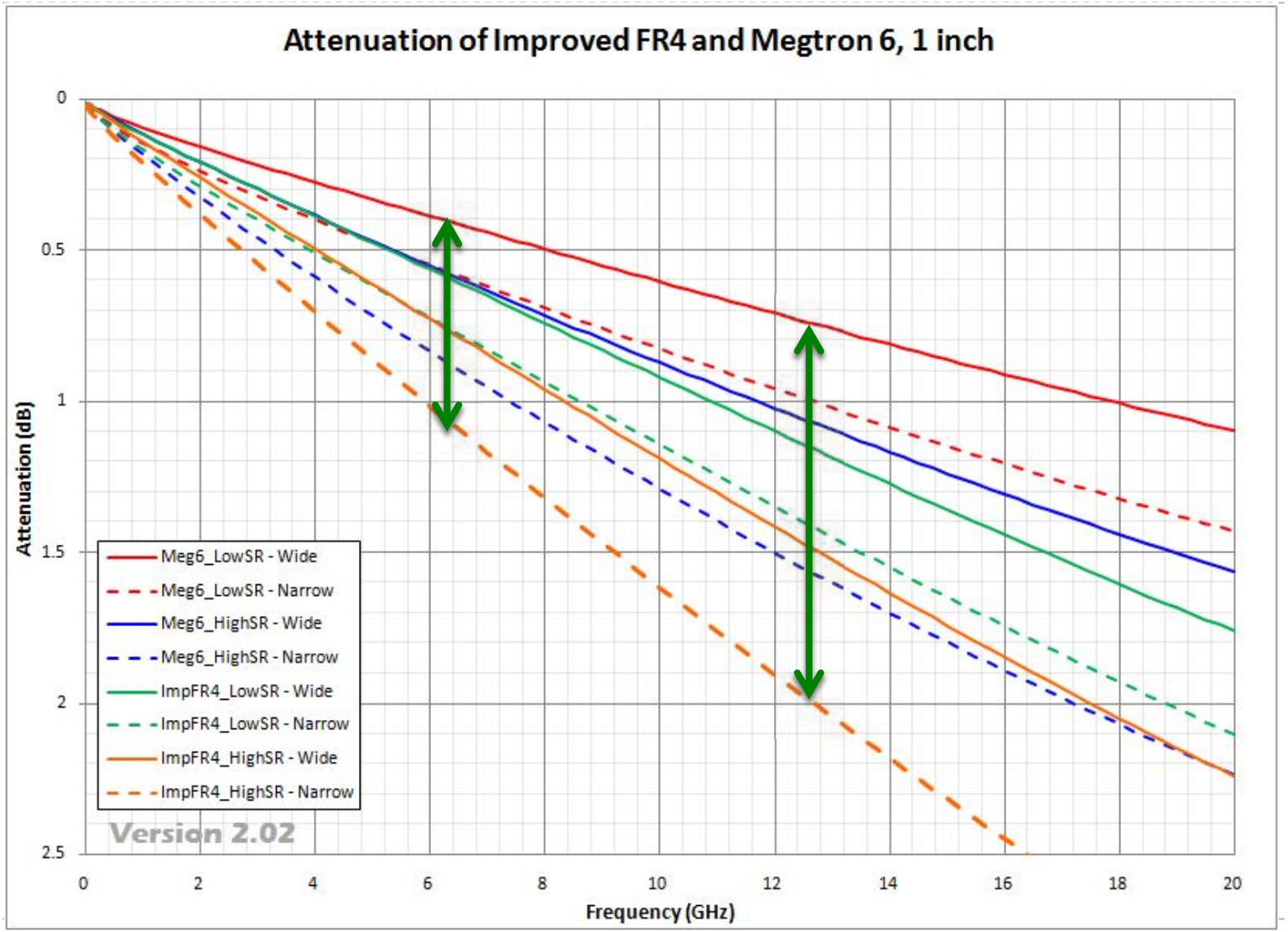
A detailed technical analysis the key issues will be presented in goergen_01_0112

Design space challenge: Breadth of backplane trace lengths



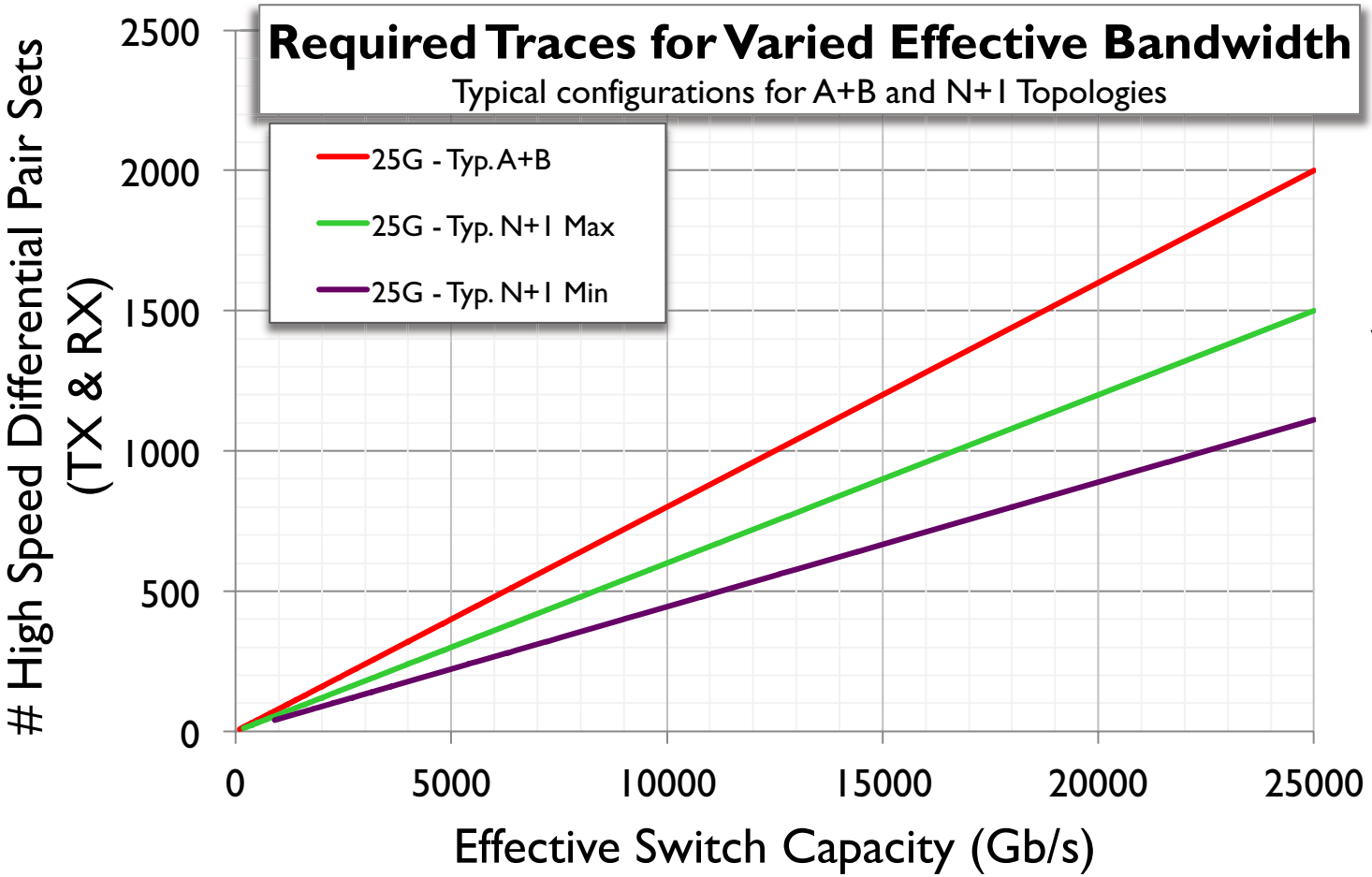
Source: http://www.ieee802.org/3/bj/public/nov11/dambrosia_02a_1111.pdf

Design space challenge: Range of PWB Losses



Source: Beth Kochuparambil, Cisco

Design space challenge: Backplane design & manufacturing complexity

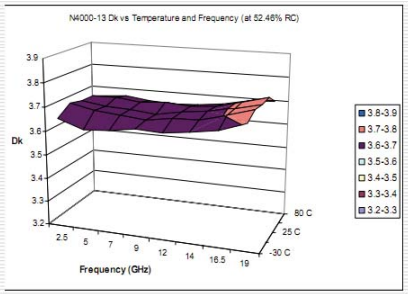


Manufacturing variations require design margin

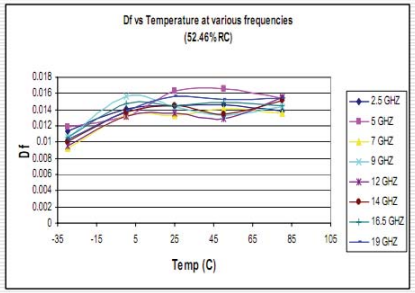
Source: Beth Kochuparambil, Cisco

Design space challenge: Manufacturing & Environmental variation

Material Variance



Impact of Temperature and Frequency on d_k for Nelco 4000-13



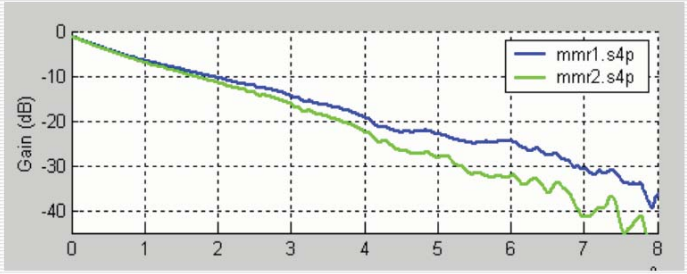
Impact of Temperature and Frequency on d_f for Nelco 4000-13

Observations

- Manufacturing @ 34 inches
  - @ 2.5 GHz – 3 dB deviation
  - @ 5 GHz - 6 dB deviation
- Environmental @ 20 inches
  - @ 2.5 GHz – 5dB deviation
  - @ 5 GHz - 7 dB deviation

Backplane Ethernet Study Group January, 2004 — John D'Ambrosia Tyco Electronics — 16

QuadRoute Backplane – Manufacturing Variance @ 34 Inches

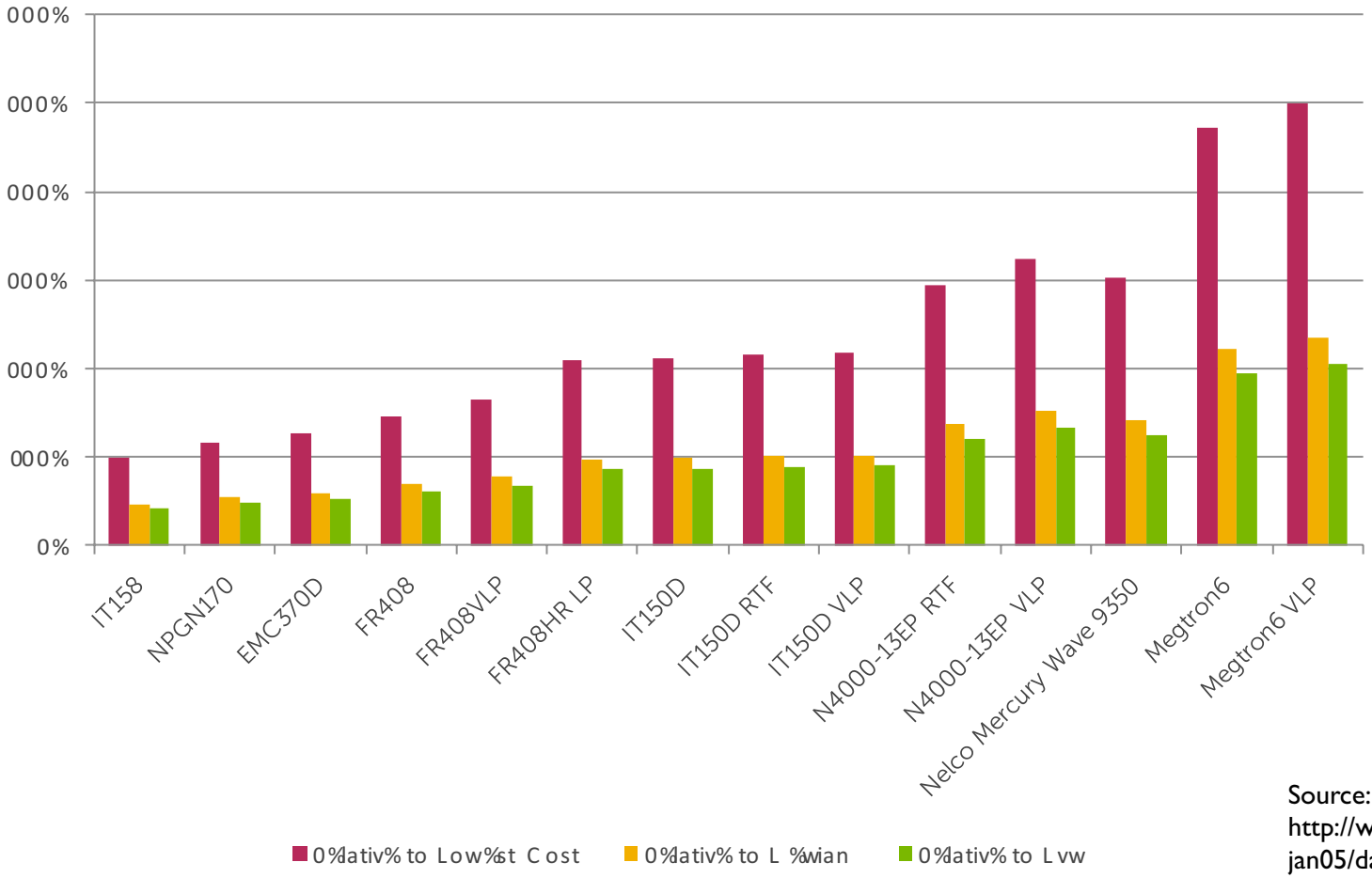


Backplane Ethernet Study Group January, 2004 — John D'Ambrosia Tyco Electronics — 13

Source: http://www.ieee802.org/3/bladesg/public/jan04/dambrosia_01_0104.pdf

Design margin required to ensure high yield

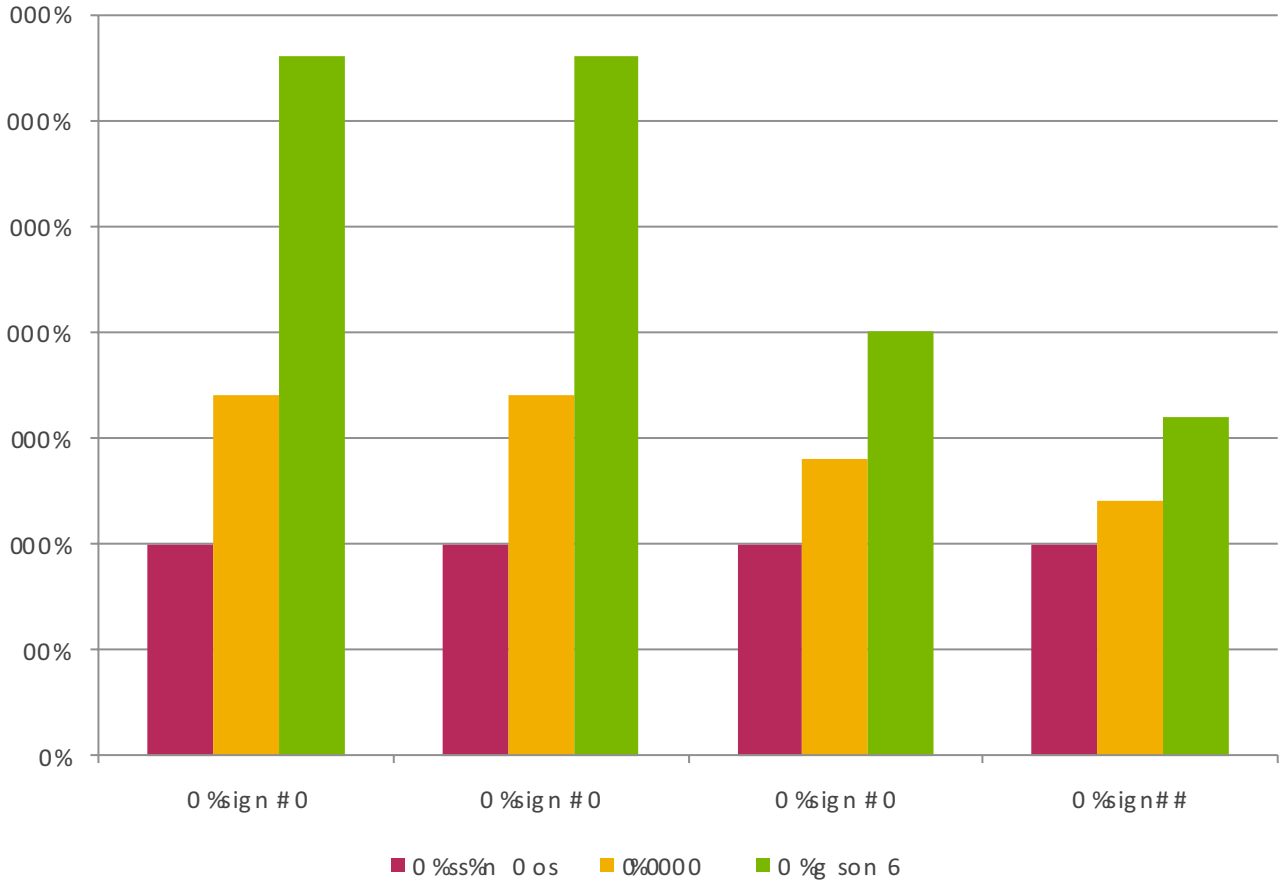
Design space challenge: Relative Cost Impact of Materials



"Relative cost" impact depends on where you are!

Source: http://www.ieee802.org/3/ap/public/jan05/dambrosia_01_0105.pdf

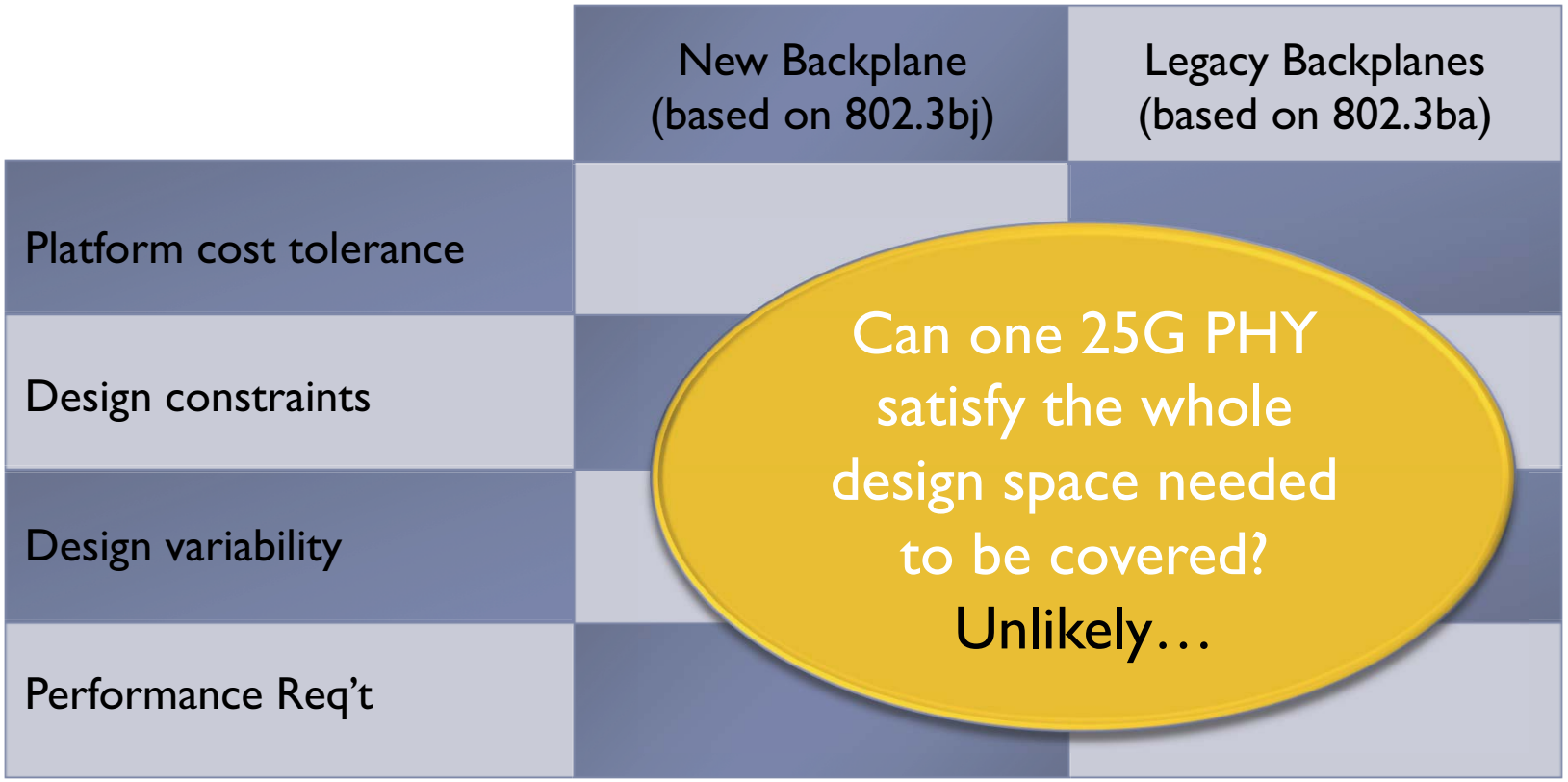
Design space challenge: Design/Material cost dependency



"Relative Cost" of materials impacted by Design

Source: http://www.ieee802.org/3/bj/public/nov11/dambrosia_02a_1111.pdf

The design space challenge



Choosing a PHY proposal (1)

- This presentation supports both NRZ and PAM4 PHY approaches
- It is felt that the NRZ PHY will be the dominantly used PHY for next generation backplane applications.
- PAM4 PHY will be necessary to enable the transition of 802.3ba backplanes or compatible channels to support 100G.

- Concern that lack of closure within the task force of the PHY issue will unnecessarily delay the 802.3bj standard. A 2 PHY approach is valid path forward to resolve the TF deadlock.

Choosing a PHY proposal (2)

- PAM2 and PAM4 both have merits
- Broad range of applications to be supported drive different PHY requirements
- Assumption is that both PAM2 and PAM4 approaches WILL be adopted by market to satisfy wide breadth of design challenges.

- Therefore strong preference that BOTH be specified with same rigor and scrutiny by industry experts within IEEE

Summary

- There are diverse applications / products with unique needs that need to be supported
- Different design / cost requirements
  - This is an implementation issue
  - Numerous views presented in 802.3bj are probably all valid for the specific assumptions used
- System vendors will want to use both types of PHYs

- We support and recommend the development of two PHYs targeting two classes of channels, based on two different classes of materials… Add an objective!

Thank You!