In Support D1.3 Comments

IEEE 802.3bj Task Force

Ali Ghiasi –Broadcom
Will Bliss - Broadcom

Jan 23-24, 2013

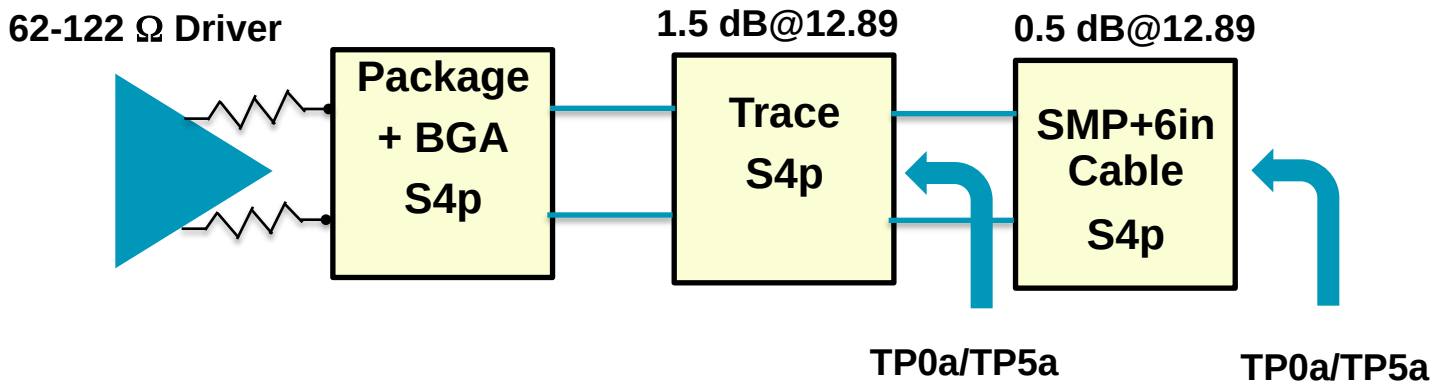
Phoenix

Overview

- Addressing following comments
  - 128/129/132/134 –KR4 TX/RX
  - 130 – TX/RX host PCB CL92A
  - 133/140 – KP4 TX CDR BW and KP4 jitter tolerance

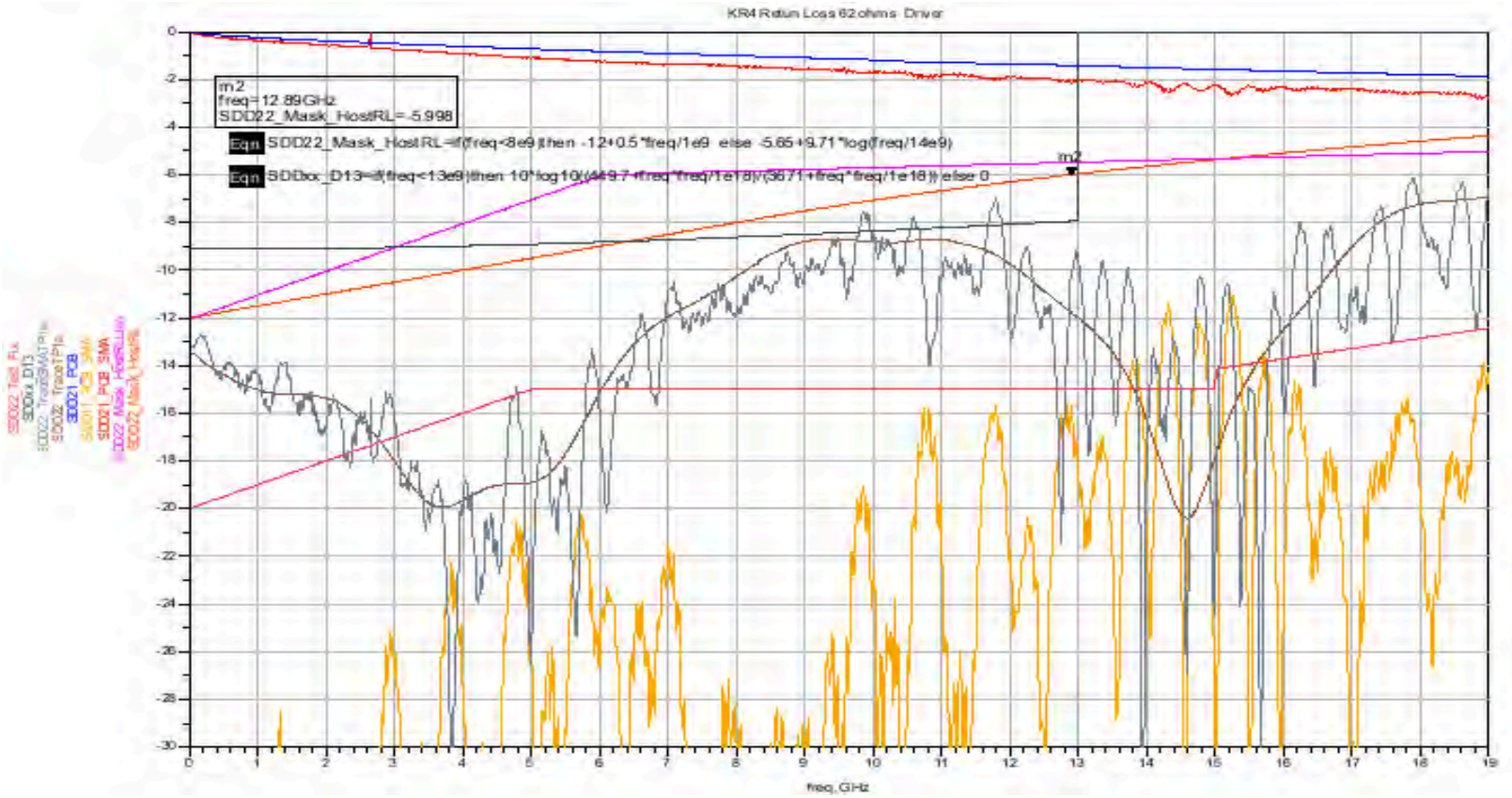
KR4 TP1a/TP5a Return Loss

- KR4 return loss needs to be defined at TP0a/TP5a at measurable test points
  - TP0a/TP5a are defined to have loss of 1.2-1.6 dB at 12.89 GHz and RL meeting 93-1
- To emulate TP0a/TP5a the test setup was as following



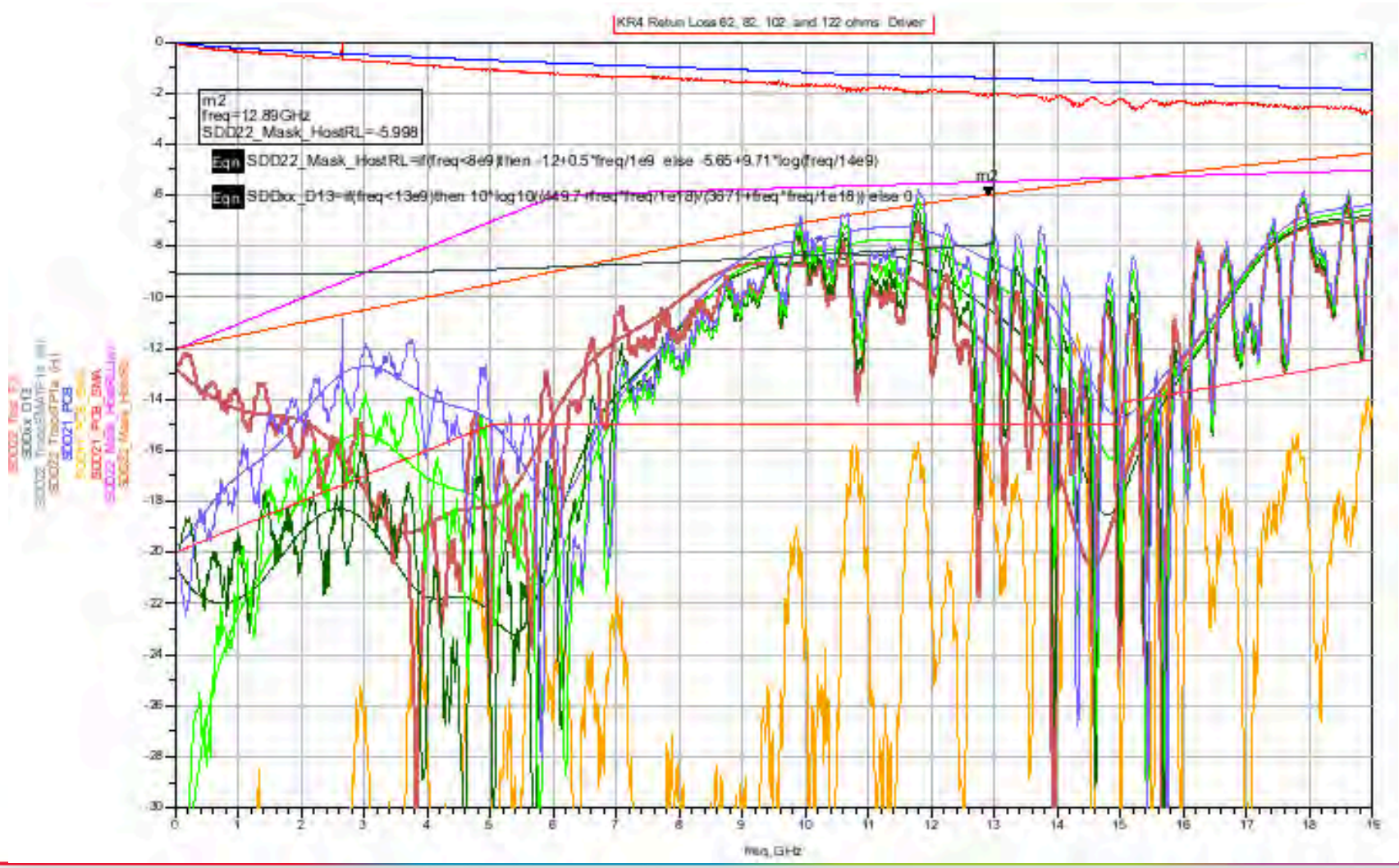
TP0a/TP5a Return Loss

- Return loss for 62 Ω driver shown at output of the stripline as well as at output of SMP 6” cable
  - Also shown is proposed masked proposed during adhoc meeting (Blue) that could result failing CR4 TP2 RL
  - Proposed mask (red) identical to eq 92-5 addressing comment 128/129/132/134



TP0a/TP5a Return Loss

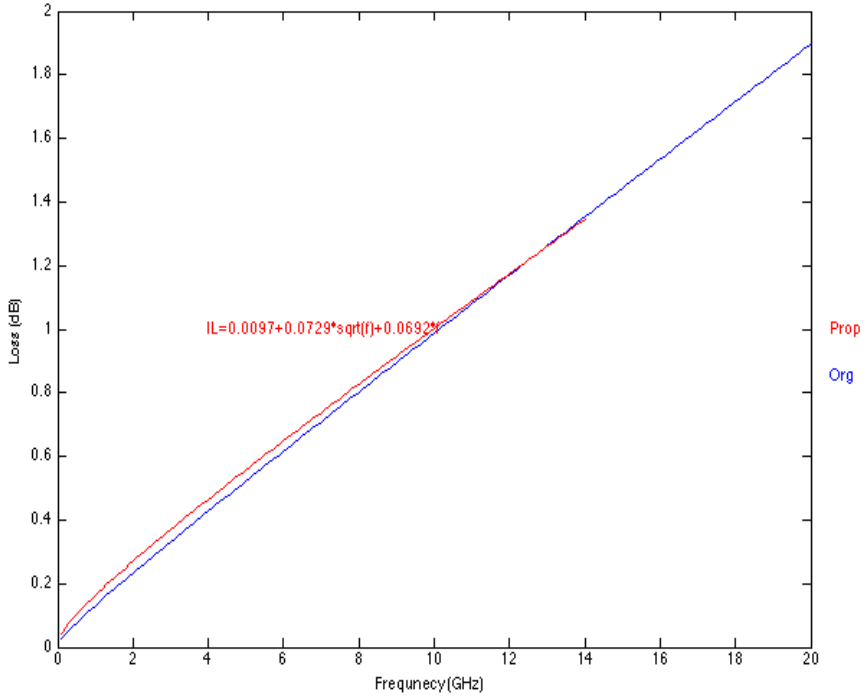
- Return loss from 62 -122 Ω driver in 10 Ω steps
  - Worst RL for 122 ohms driver



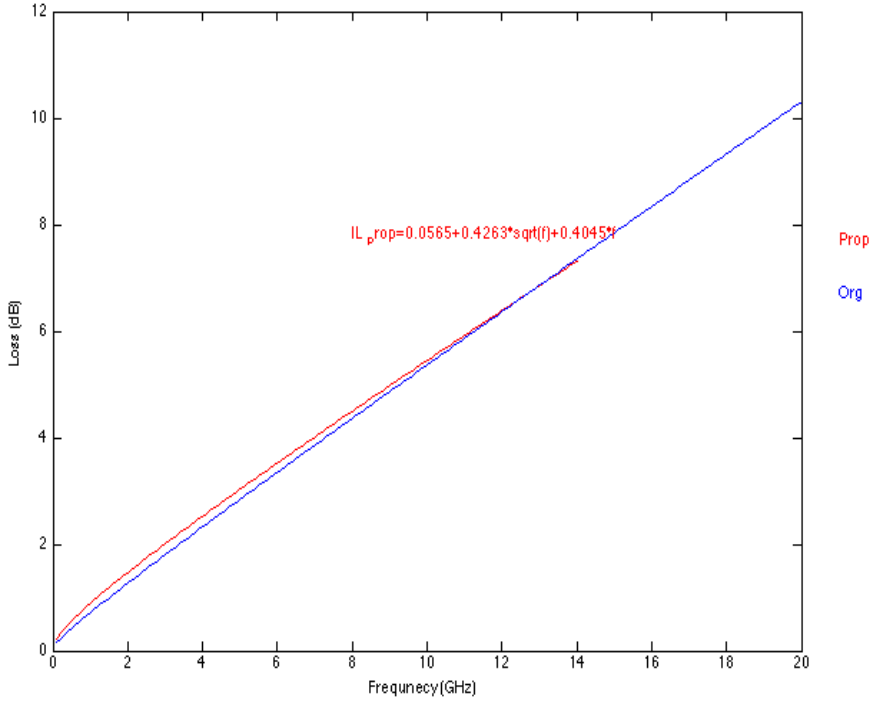
Transmitter and Receiver Differential Host Board Loss

- Addressing comment 130
  - Current differential PCB loss is not consistent with the channel TP0-TP2 or TP3-TP5
  - Equation 92A-1 and 92A-2 linear term is >2x the sqrt term
  - But the channel loss Eq 92-4 linear term ~ as the sqrt term

Min Loss



Max Loss



Standalone KP4 Sinusoidal Jitter Test

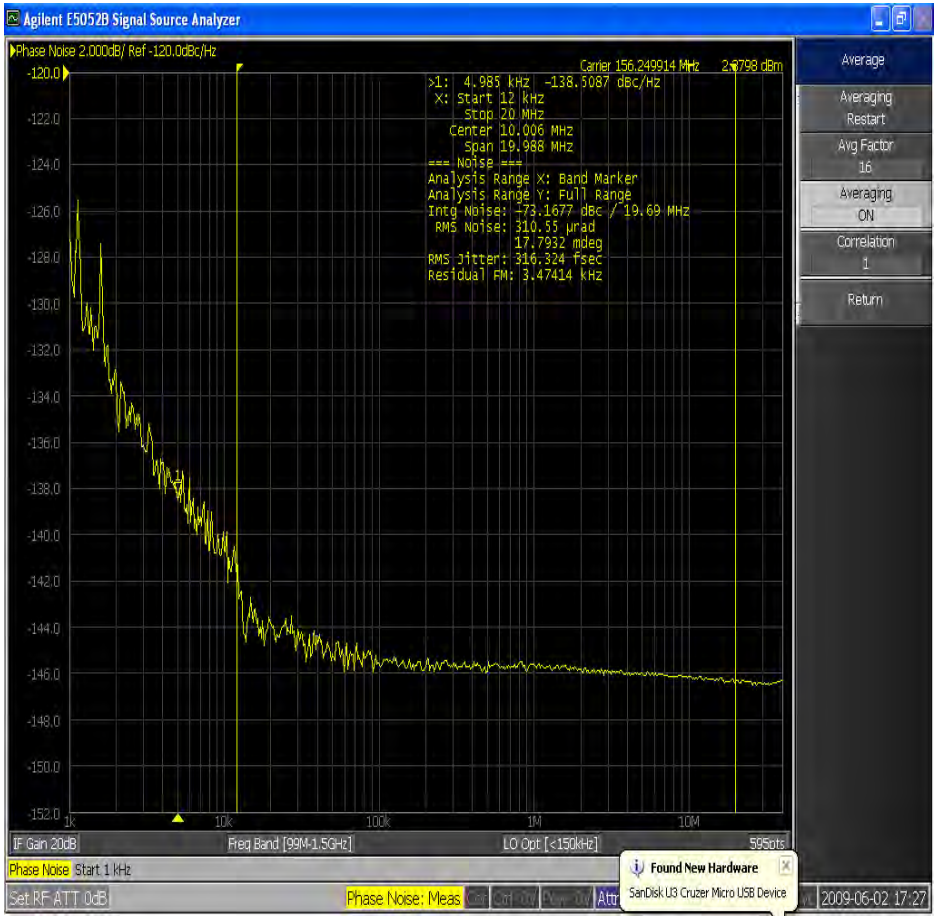
- Other standards such as 10Gbase-LRM, 40Gbase-CR4/ KR4, 16G FC have used standalone Sinusoidal Jitter test to the receiver to make sure clock jitter allowed by transmitter is trackball by the receiver
  - Separate interference tolerance based on worst case channel will test the receiver equalization capability
  - Adding SJ to the above test will be too complex
- Since time of 10 GbE the loop BW for golden CDR to track allowed jitter by the transmitter has been Fbaud/2500
  - This was reasonable loop BW for days when good oscillators were costly and the receiver was simple Bang-Bang CDR
  - KP4 having more complex receiver and with availability of low cost good performance oscillator the golden CDR BW should be reduced to Fbaud/33,985
- Addressing comment 133/140

CDR with Loop Latency

- The lowest power DSP implementations of PAM-4 will have considerable latency in the ‘CDR loop’
  - This limits the readily achievable ‘corner frequency’
  - Which changes the engineering motivation for the TX jitter specification and budget
  - Which changes the supporting RX jitter tolerance test specification
- There are many choices for CDR
  - A simple Type II PLL (aka PI = Proportional + Integral control) is assumed here, except for the addition of latency to model DSP operations and delays though analog interfaces and processing

Typical Low Cost Oscillator Phase Noise Plot

- Most oscillator phase noise is flat after 1 MHz
  - There is no benefit to higher CRU BW!

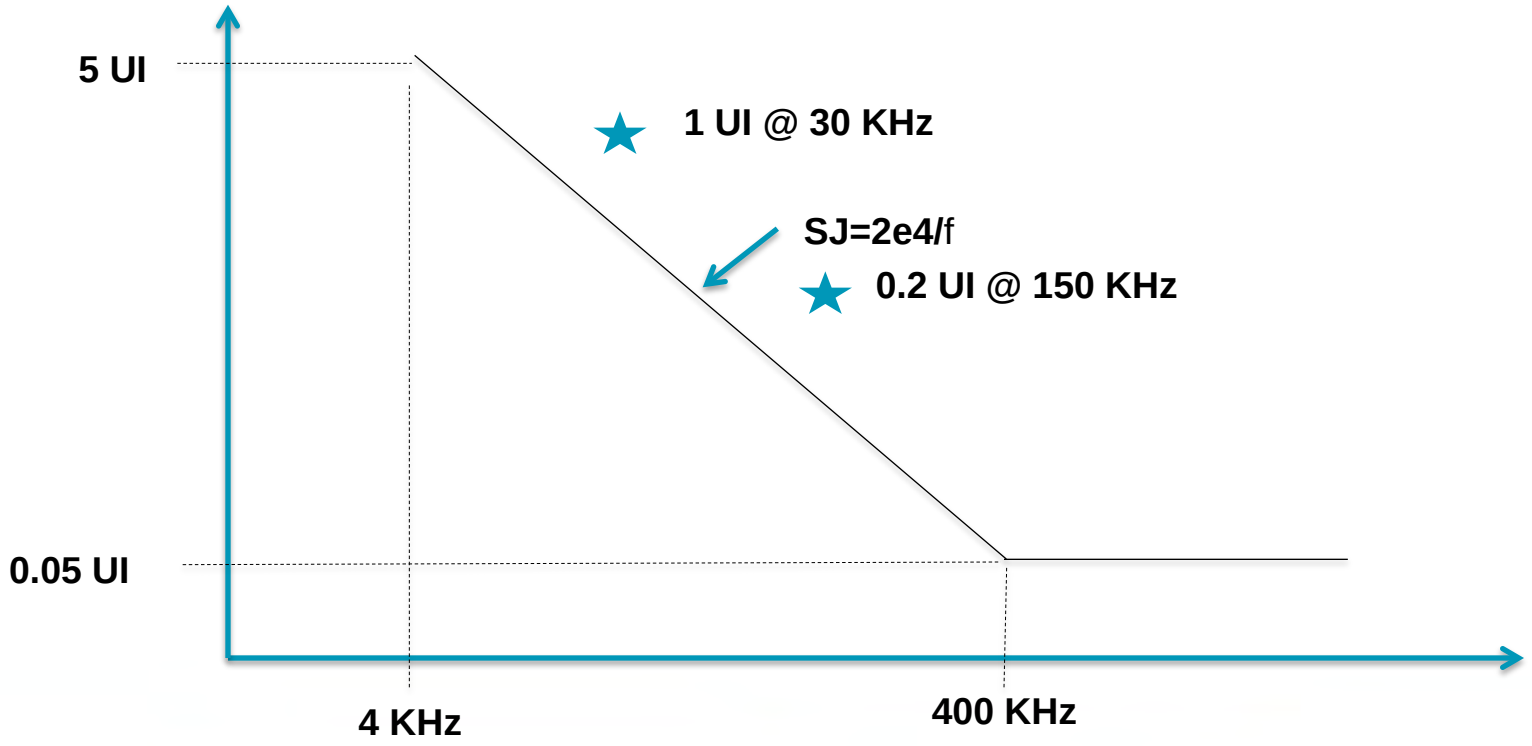


Consideration for CRU and CDR BW

- Consideration for golden PLL CRU BW
  - Oscillator phase noise
    - Typically no benefit as the phase noise is flat >1 MHz
  - Crosstalk
    - High frequency efect >> CRU BW
  - VCO phase noise
    - No benefit for CRU BW >4 MHz
- Consideration for CDR BW
  - Pattern dependent effects
    - Does not apply to 64/66B or 256/257B with spectrum in the sum 100 KHz
  - Power
    - Higher loop BW results in higher power
  - Receiver DFE
    - Fast tracking loop require low latency timing recovery loop which burns significantly more power
- With additional feedback received during the meeting the proposed CRU BW is reduced to 400 KHz to accommodate more flexible receiver at slight jitter penalty on the transmitter.

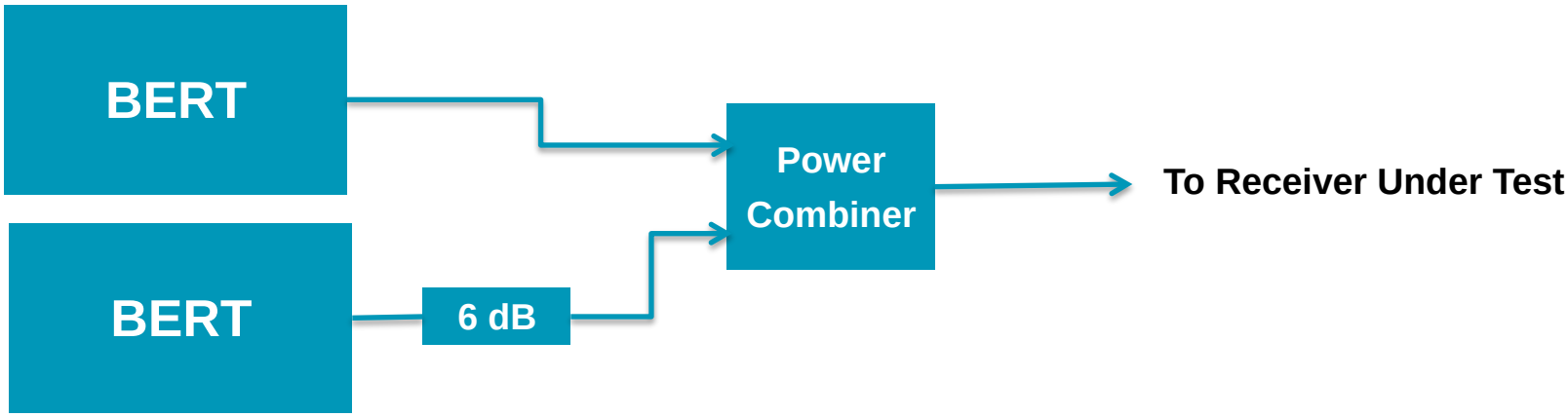
Diagram of SJ Tolerance Mask

- KP4 transmitter is tested with golden CDR having loop BW of Fabud/33985
  - KP4 receiver is tested at about 2x the mask amplitude 2e4/f
    - 1 UI @30 KHz
    - 0.2 UI @150 KHz



KP4 SJ Test Setup

- Pattern PN31
- SJ applied 1 UI @ 30 KHz and 0.2 UI @150 KHz
- Output waveform should be tested at max and min amplitude limits
- BER <1E-5

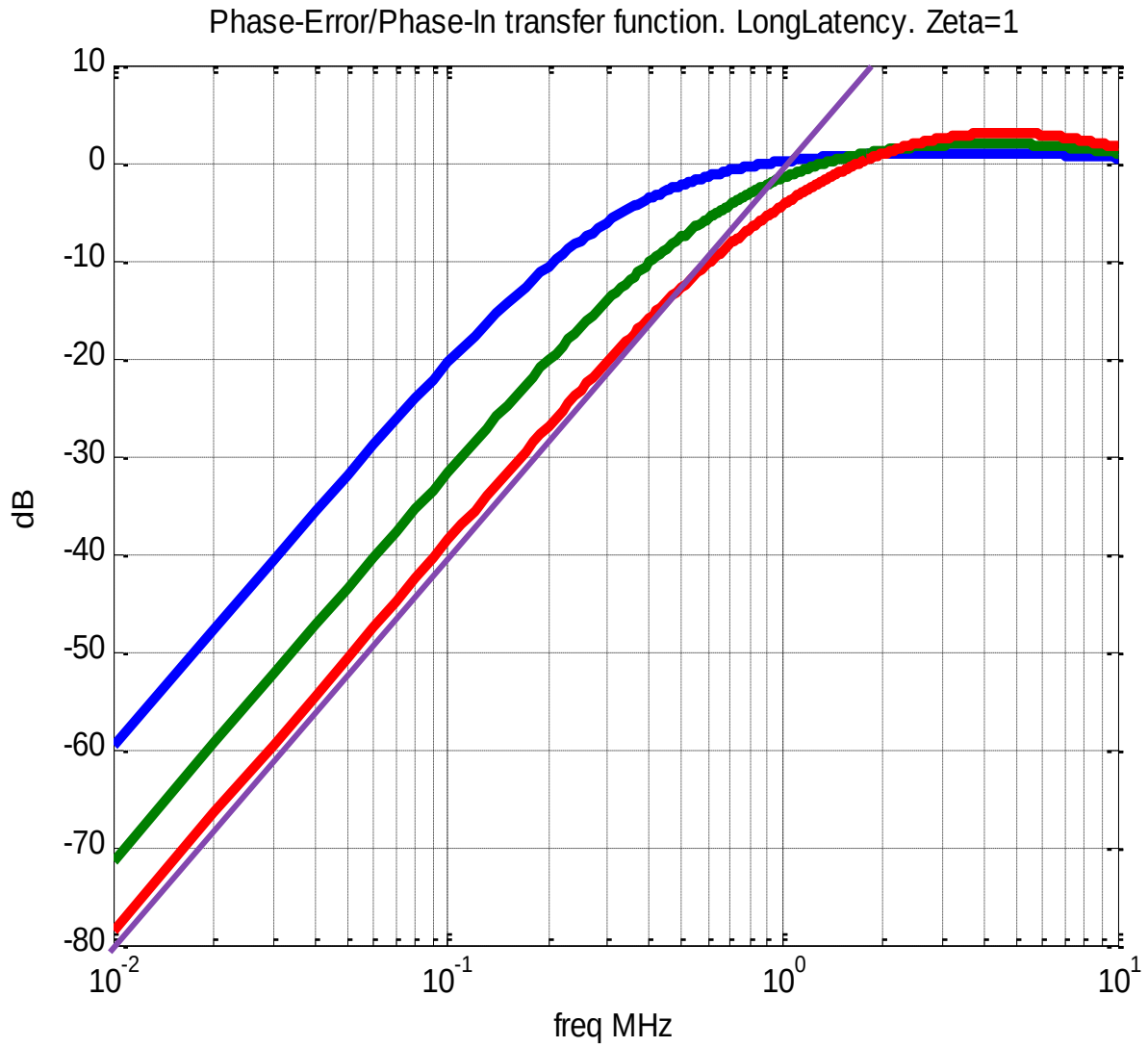


Backup Slides

CDR with Loop Latency

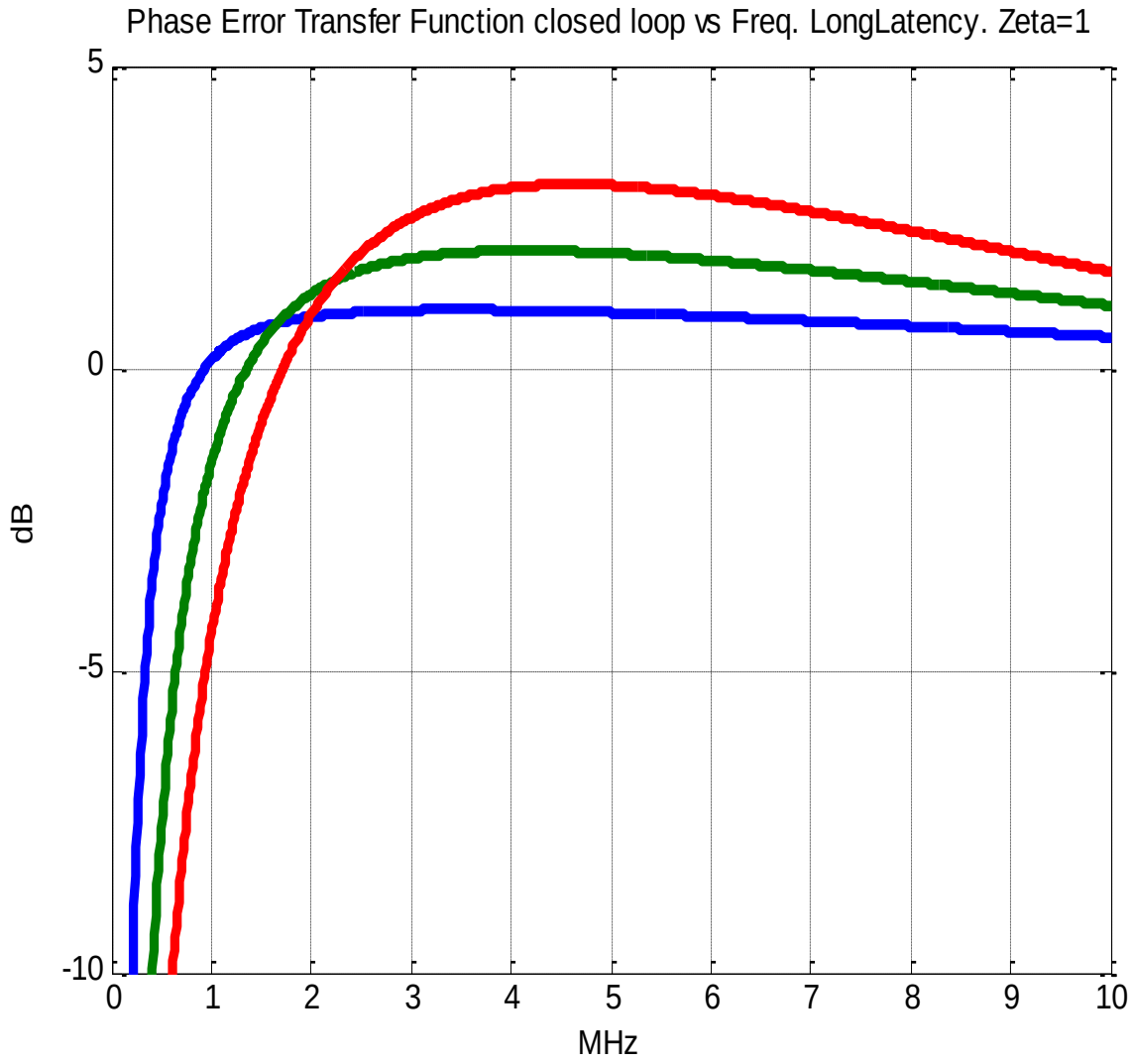
- Two basic design styles are presented
  - A well damped system with zeta = 1 which achieves ~40dB / decade roll-off
  - An over-damped system with zeta = 10 which performs close to ~20dB/ decade roll-off
- Note that the over-damped system will be less able to capture large frequency steps (as in start-up), etc.
  - But will be sufficient to track slowly changing / drifting frequency

Phase_ERROR(f)/ Phase_IN(f), Zeta=1



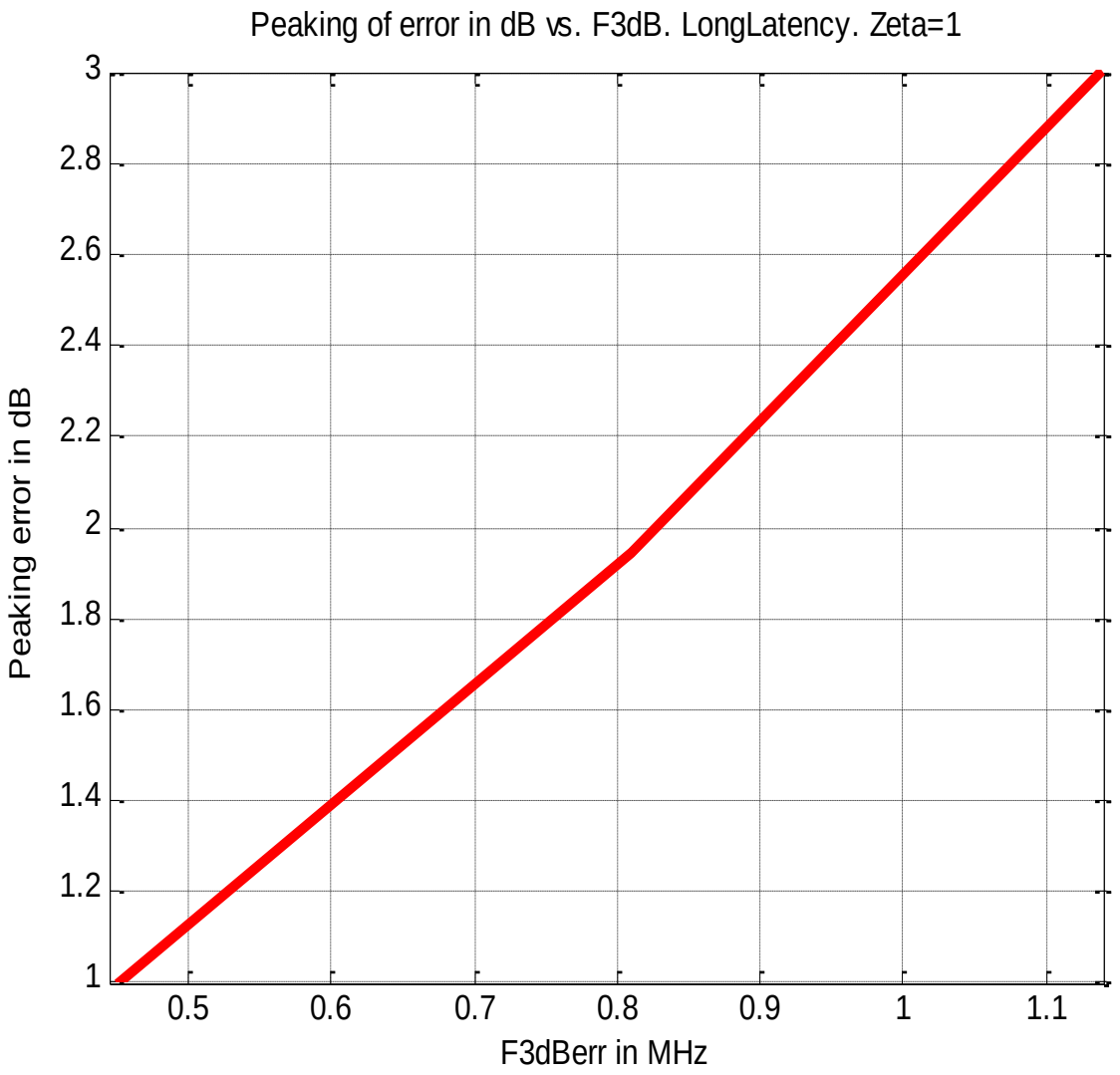
- 3 different candidates are shown
- All ‘peakt’ above their corner frequency, where they become jitter amplifiers rather than jitter suppressers
- All achieve 40dB/ decade slope away from the corner frequency
- Higher corner frequency produces higher undesired ‘peaking’

Phase_ERROR(f)/ Phase_IN(f), Zeta=1



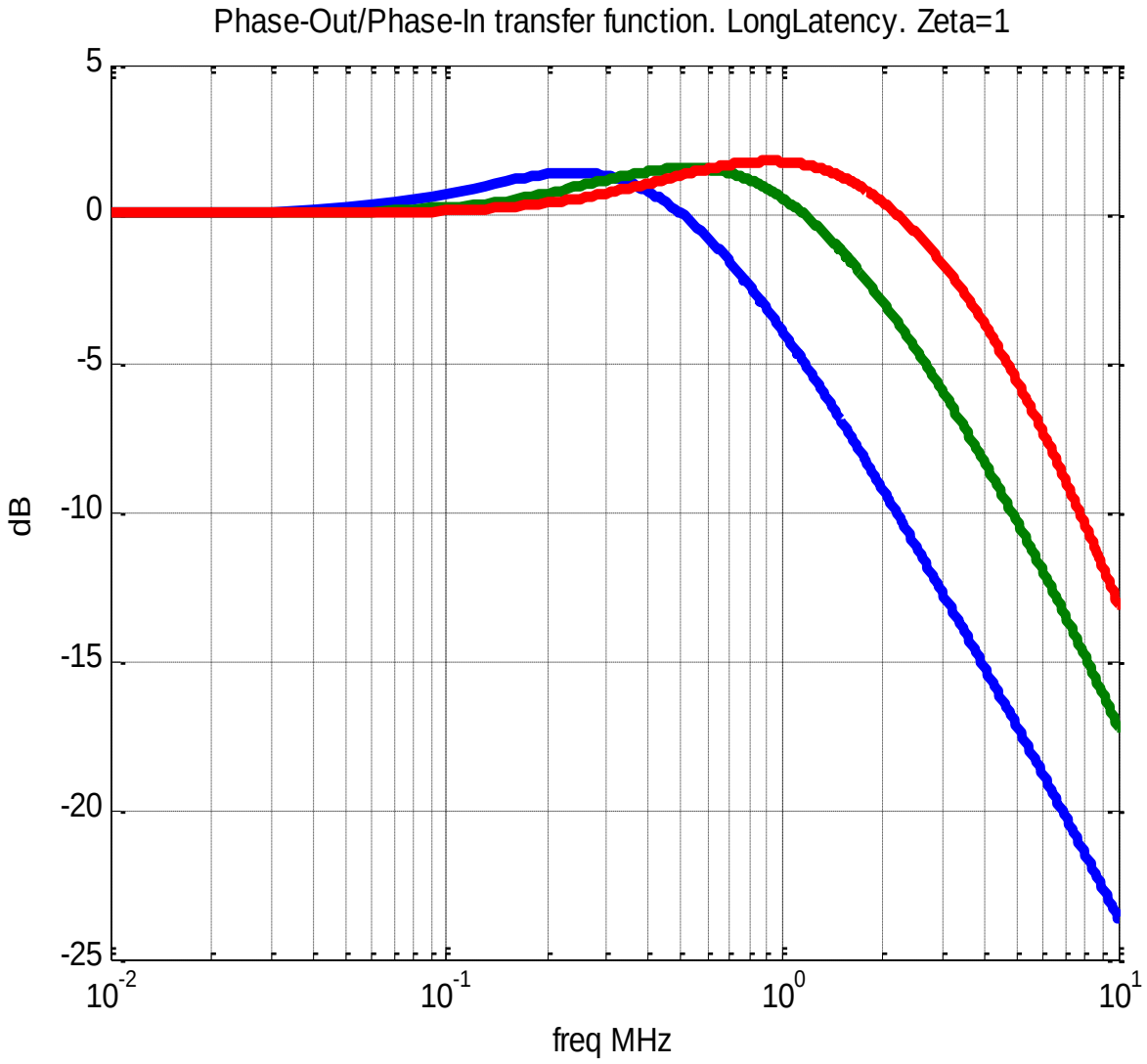
- Linear frequency scale highlights that the peaking region (of jitter amplification) is much wider than the ‘tracking region’ and increases with corner frequency

Max Jitter Peaking dB vs. 3dB Corner, Zeta=1



- Corner frequency of ~1MHz is ‘feasible’ but brings over 2.5dB max jitter amplification
- Jitter Peaking (amplification) of 1dB max limits the 3dB corner frequency to < 450KHz

Phase_OUT(f)/ Phase_IN(f), Zeta=1

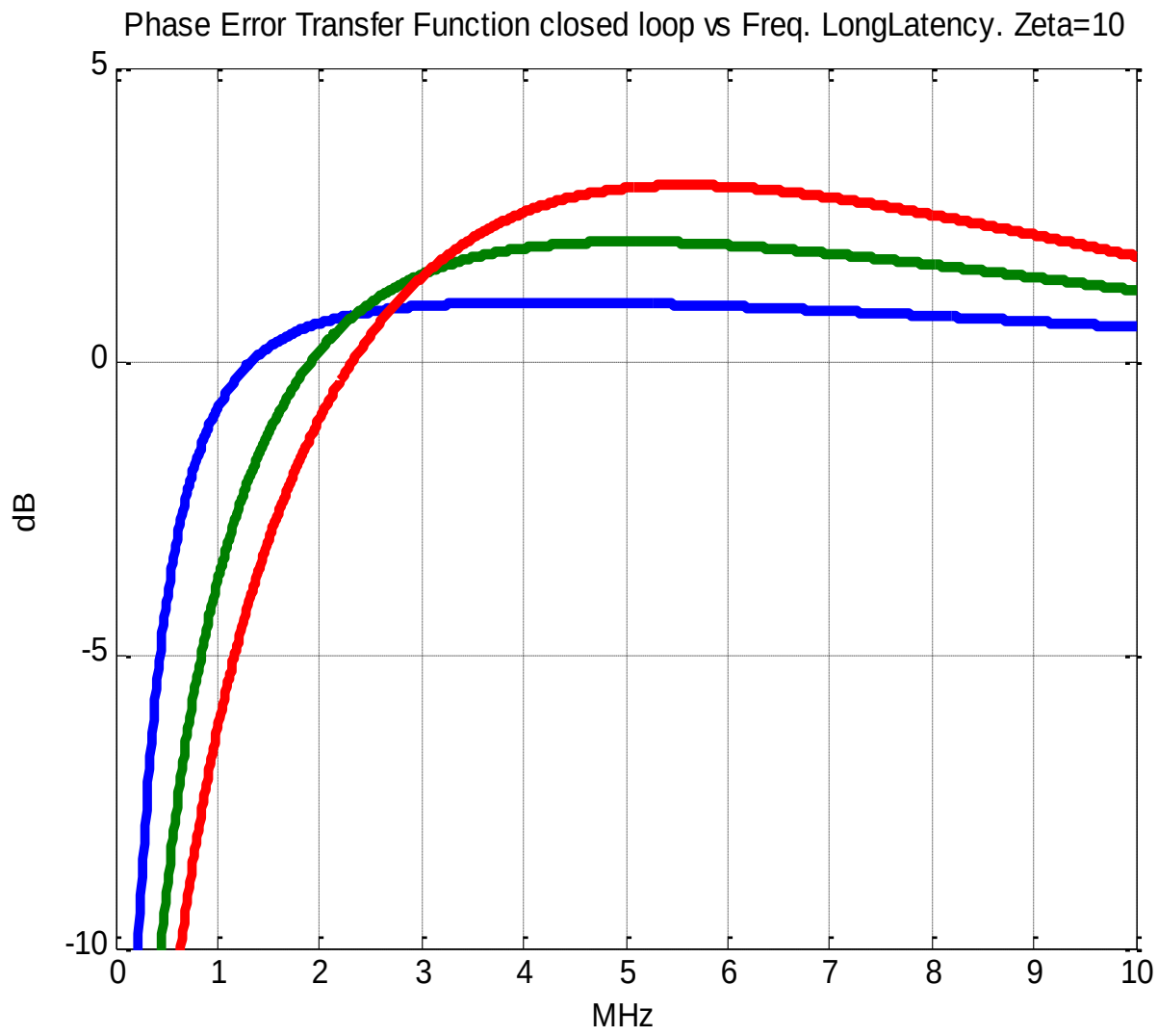


- The transfer function of CDR Phase_OUT / Phase_IN is a low pass function that is frequently shown
- The apparent 3dB corner frequency is higher and the ‘peaking’ is different
- This is not the appropriate transfer function to study Jitter suppression (or amplification)

Phase_ERROR(f)/ Phase_IN(f), Zeta=10

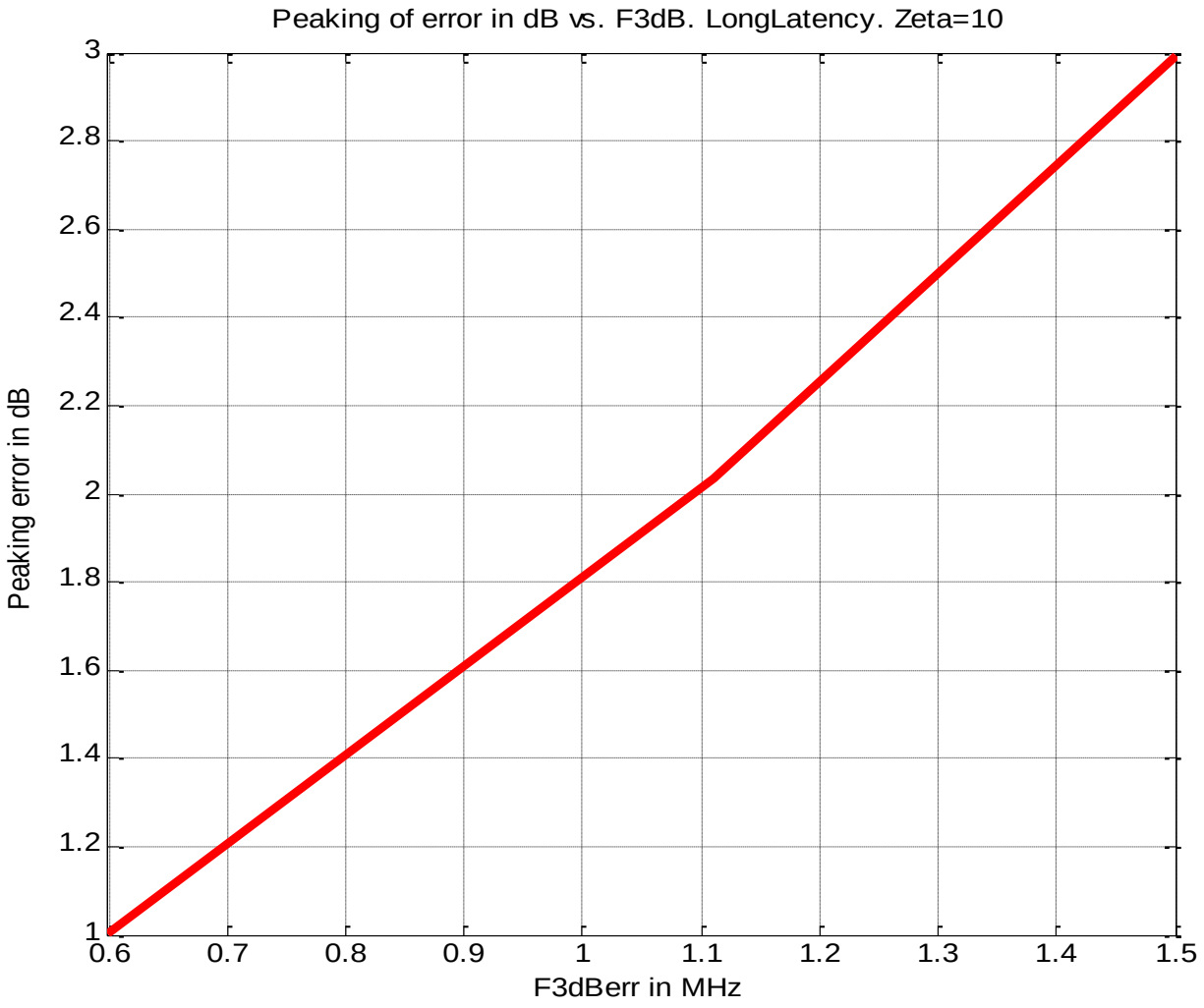
- 3 different candidates are shown
- All have ‘peaking’ above their corner frequency, where they become jitter amplifiers rather than jitter trackers (suppressers)
- The large ‘over-damping’ means the slope is only ~20dB/ decade
- Note that while the corner frequency is higher, the suppression of low

Phase_ERROR(f)/ Phase_IN(f), Zeta=10



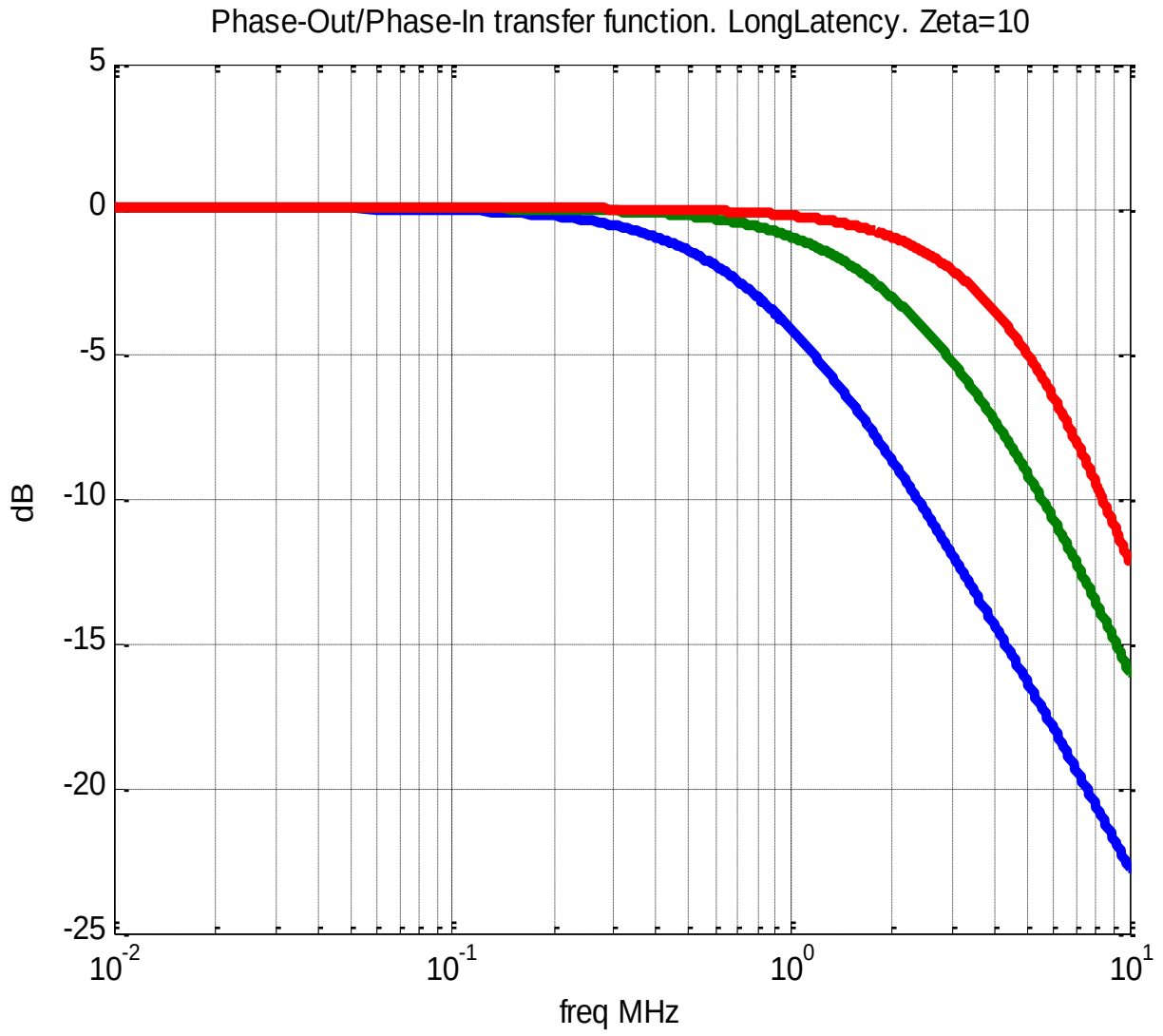
- Linear frequency scale highlights that the peaking region (jitter amplification) is much wider than the ‘tracking (suppression) region’

Max Peaking dB vs. 3dB Corner, Zeta=10



- The increased damping allows increased Corner frequency for a same maximum ‘peaking’
- A corner frequency of ~1MHz is feasible but brings 1.8 dB of jitter amplification
- Max peaking (amplification) of 1dB max limits the 3dB corner frequency to <600KHz

Phase_OUT(f)/ Phase_IN(f), Zeta=10



- The transfer function of CDR Phase_OUT / Phase_IN is a low pass function that is frequently shown
- The apparent 3dB corner frequency is higher and the ‘peaking’ is different
- In this case the ‘peaking’ is very small, even though for error transfer function we have 1,2,and 3dB peaking
- This is not the correct TF to study jitter suppression

Thank You