Supporting material for comments against Clause 91 RS-FEC

Adam Healey
LSI Corporation

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Comment #244

- FEC synchronization and alignment state diagrams deadlock when all_locked is true but fec_alignment_valid is false
- This can occur if the lane-to-lane skew exceeds the RS-FEC deskew capability
- This can occur if amps_lock<x> is set to true at the incorrect starting bit position for FEC lane x
  - A random 64-bit block matches a valid alignment marker payload (to within 3 nibbles) and…
  - The 64-bit block amp_counter bits away from the first block matches the same alignment marker payload (to within 3 nibbles)
- Despite the low-likelihood of these (or other) cases, deadlock conditions should be avoided

Modify FEC alignment state diagram, Figure 91–9

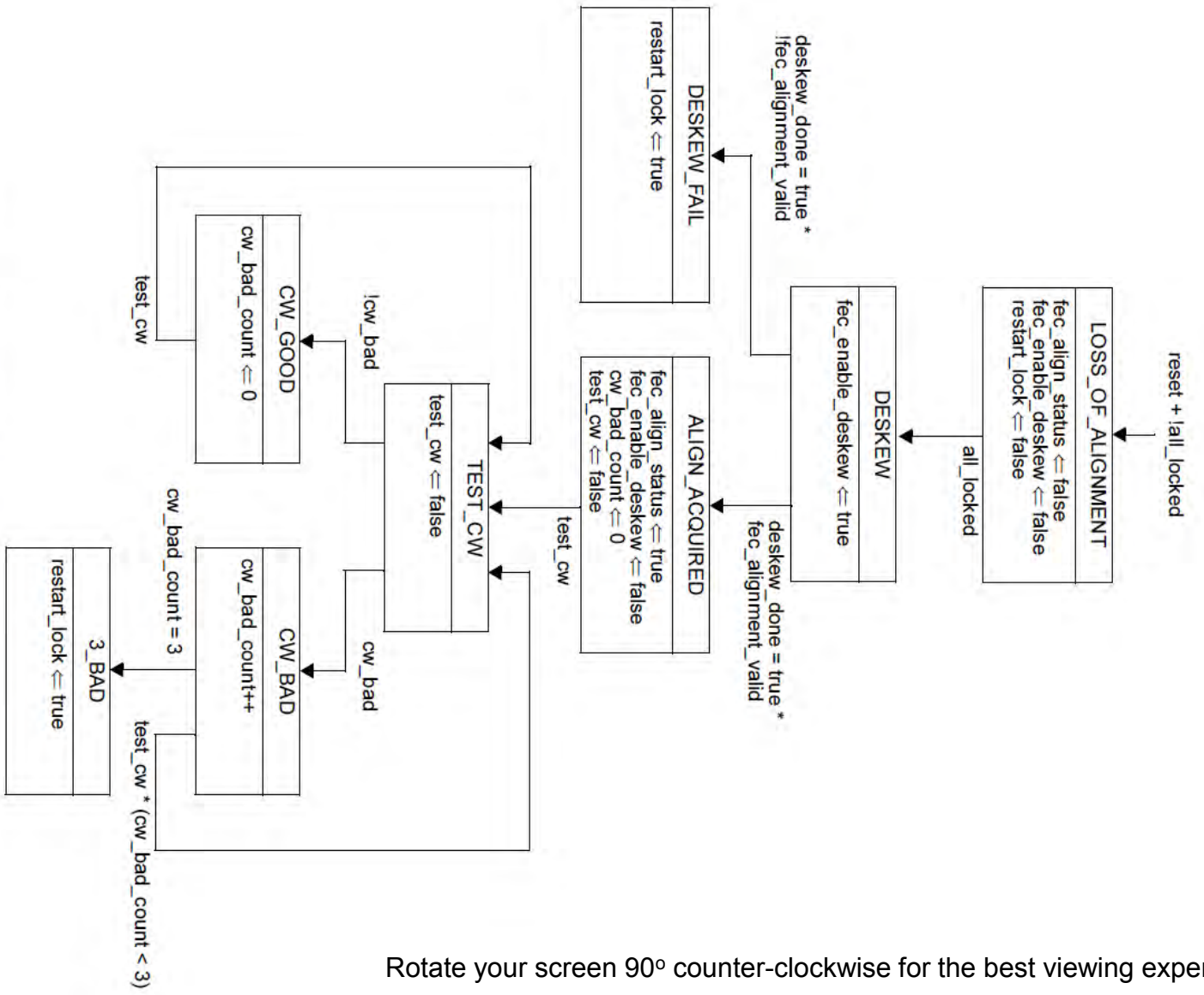

Figure 91–9—FEC alignment state diagram

Rotate your screen 90° counter-clockwise for the best viewing experience.

Add new state variable

deskew_done

A Boolean variable that is set to true when fec_enable_deskew is set to true and the deskew process is completed. Otherwise, this variable is set to false.

Comments #18, #205, #241, #110, #281, #158, #212

		FEC_bypass_indication_enable	
		0	1
FEC_bypass_correction_enable	0	A	C
	1	D	~~B~~

- Change the sense of FEC_error_indication_enable
  - FEC_bypass_indication_ability, FEC_bypass_indication_enable

- Mode A (correct and indicate uncorrected errors) is the default
- Mode D (only indicate errors) is optional for reduced data delay
- Mode B is not permitted
- Mode C (correct but do not indicate uncorrected errors) is under discussion
  - FEC_bypass_indication_ability/enable unnecessary without mode C
  - Supplemental error monitoring required to ensure acceptable MTTFPA
  - Refer to ran_3bj_01_0113, wang_3bj_01_0113, etc. for details
  - Mode C shown as conditional text (green)

91.5.3.3 Reed-Solomon decoder

For reference:

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols. The message symbols correspond to 20 transcoded blocks rx_scrambled.

When used to form a 100GBASE-CR4 or 100GBASE-KR4 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=7 symbol errors in a codeword. When used to form a 100GBASE-KP4 PHY, the RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected.

The Reed-Solomon decoder may provide the option to perform error detection without error correction to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_correction_ability variable (see 91.6.x). When the option is provided, it is enabled by the assertion of the FEC_bypass_correction_enable variable (see 91.6.1).

91.5.3.3 Reed-Solomon decoder, continued

Replace the text following the third paragraph with the following:

The Reed-Solomon decoder indicates errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors (when the bypass correction feature is enabled) or contains errors but was not corrected (when the bypass correction feature is not supported or not enabled), it shall ensure that, for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword is set to 11. This will cause the PCS to discard all frames 64 bytes and larger that are fully or partially within the codeword.

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 91.6.y). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 91.6.z).

When FEC_bypass_correction_enable is asserted, the decoder shall not bypass error indication and the value of FEC_bypass_indication_enable has no effect.

91.5.3.3 Reed-Solomon decoder, continued

Additional text for mode C:

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet will not be detected. **<Insert error monitoring proposal.>**

MDIO/RS-FEC control variable mapping, Table 91–2

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction enable	RS-FEC control register	1.200.0	FEC_bypass_correction_enable
~~FEC error indication enable~~	~~RS-FEC control register~~	~~1.200.1~~	~~FEC_error_indication_enable~~
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable

91.6.1 FEC_bypass_correction_enable

When this variable is set to one the Reed-Solomon decoder performs error detection without error correction (see 91.5.3.3). When this variable is set to zero, the decoder also performs error correction. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.92a (1.200.0).

91.6.z FEC_bypass_indication_enable

This variable is set to one to bypass the error indication function (see 91.5.3.3) when this ability is supported. When this variable is set to zero, the decoder indicates errors to the PCS sublayer. The default value of this variable is zero. This variable is mapped to the bit defined in 45.2.1.xx (1.200.1).

MDIO/RS-FEC status variable mapping, Table 91–3

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass correction ability	RS-FEC status register	1.201.~~1~~0	FEC_bypass_correction_ability
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
etc.			

91.6.y FEC_bypass_indication_ability

The Reed-Solomon decoder may have the option to bypass the error indication function (see 91.5.3.3) to reduce the delay contributed by the RS-FEC sublayer. This variable is set to one to indicate that the decoder has the ability to bypass error indication. The variable is set to zero if this ability is not supported. This variable is mapped to the bit defined in 45.2.1.xx (1.201.1).