Scrambling scheme and FEC bits performance

Pete Anslow, Ciena

IEEE P802.3bj, San Diego, July 2012

Contributors

Martin Langhammer, Altera

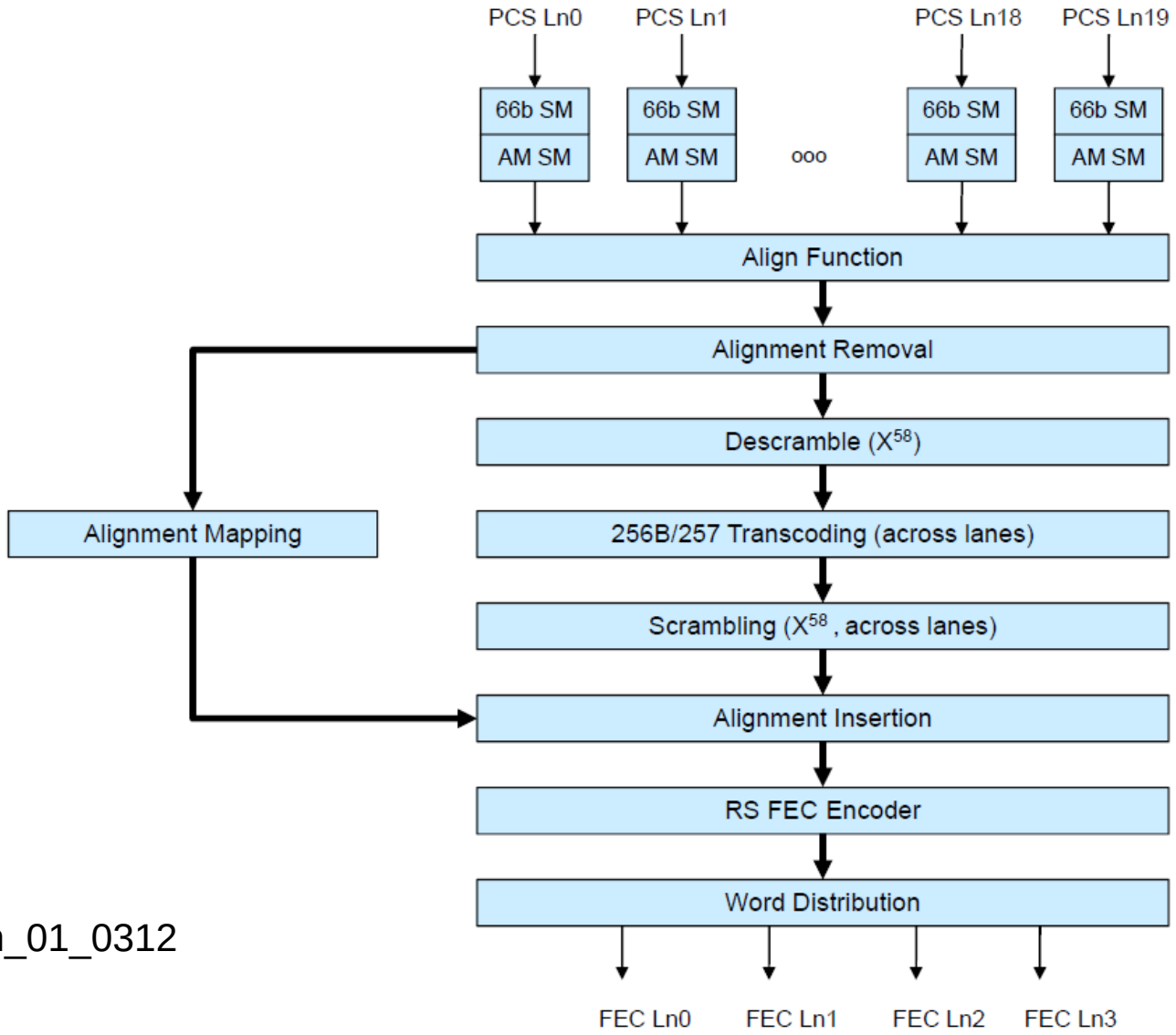
Introduction

cideciyan_02_0512.pdf from the Minneapolis meeting proposed an alternative architecture for both the NRZ and PAM4 FEC schemes where instead of de-scrambling the incoming bit stream and then re-scrambling after transcoding, the incoming bit stream is passed through with the scrambling as received.

However, in cideciyan_02_0512.pdf it is proposed to apply an additive synchronous PN-5280 scrambler after the FEC encoder. During discussion of cideciyan_02_0512 during the May meeting, it was questioned whether this was necessary.

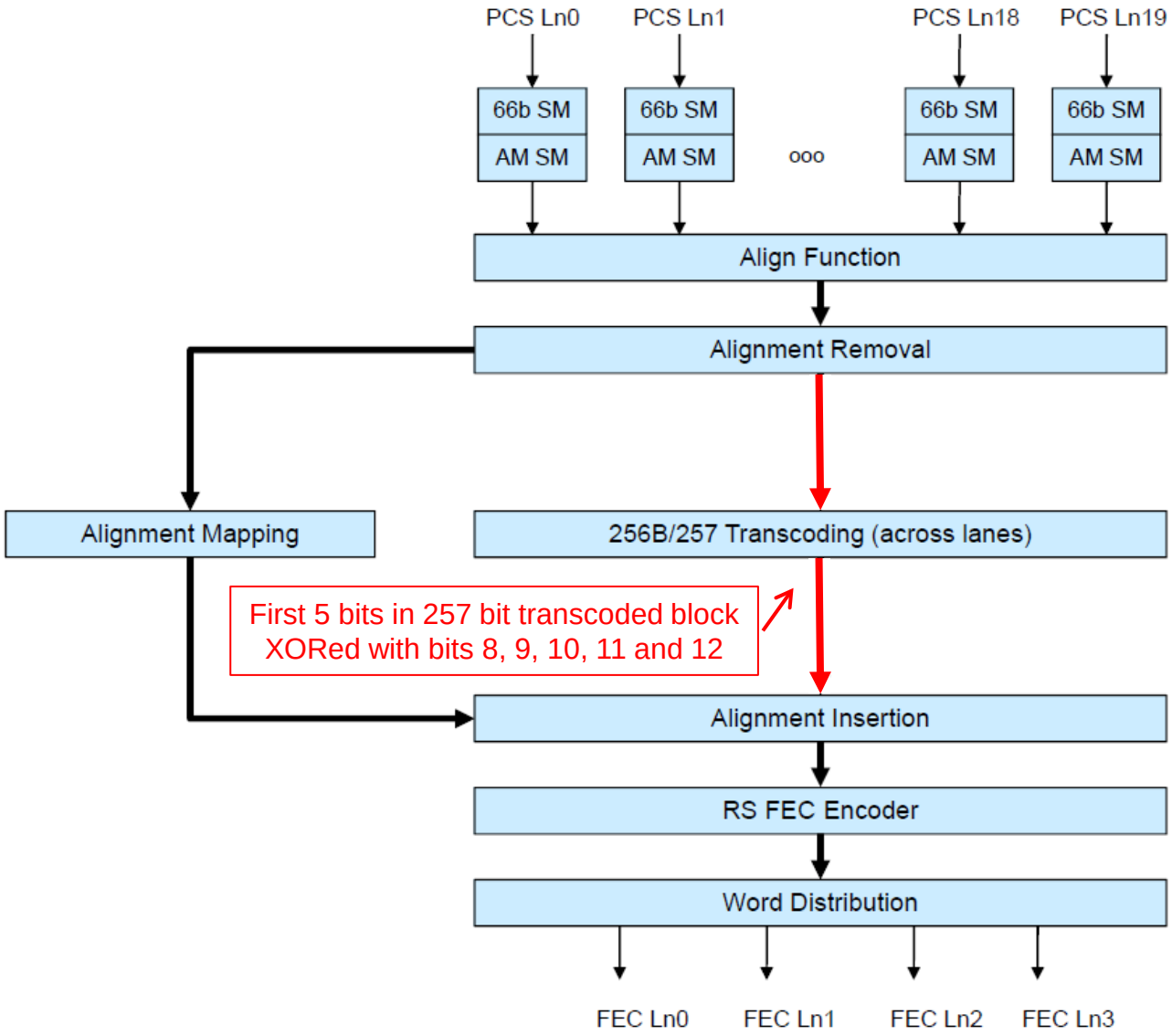
This presentation looks at the properties of the symbol stream generated by passing the input scrambling straight through and calculating the FEC parity bits to see if the additive scrambling is required.

D1.0 Tx architecture for NRZ and PAM4



Gustlin_01_0312

Simulated alternative architecture



Simulations

The differences from the simulations in anslow_01a_0512 are:

- FEC parity bits calculated by routine provided by Martin Langhammer
- AM BIP bits calculated instead of random
- AM pad bits order reversed to match D1.0 0x05, 0x1A

For D1.0 architecture simulations

- Transcoding followed by scrambling of entire 257 bit block

For alternative architecture simulations

- Scrambling followed by transcoding and first 5 bits in 257 bit transcoded block XORed with bits 8, 9, 10, 11 and 12
- BIP bits calculated from input scrambled stream

For all PAM4 simulations

- The overhead bits H(i, p, k), still random

FEC bit order

Draft D1.0 does not make it clear what bit ordering is associated with the FEC. (This will be clarified when Annex 91A is created).

For these simulations, the bit ordering shown below was used.

For the NRZ case, create a data block that is easy to define:

All zeros except that the second to last bit to be sent is a one, i.e. 5138 zeros followed by 10. Using the usual 802.3 convention of sending the lsb first, this would be passed to the FEC encoder using 513 10 bit symbols of 0x000 followed by 0x100

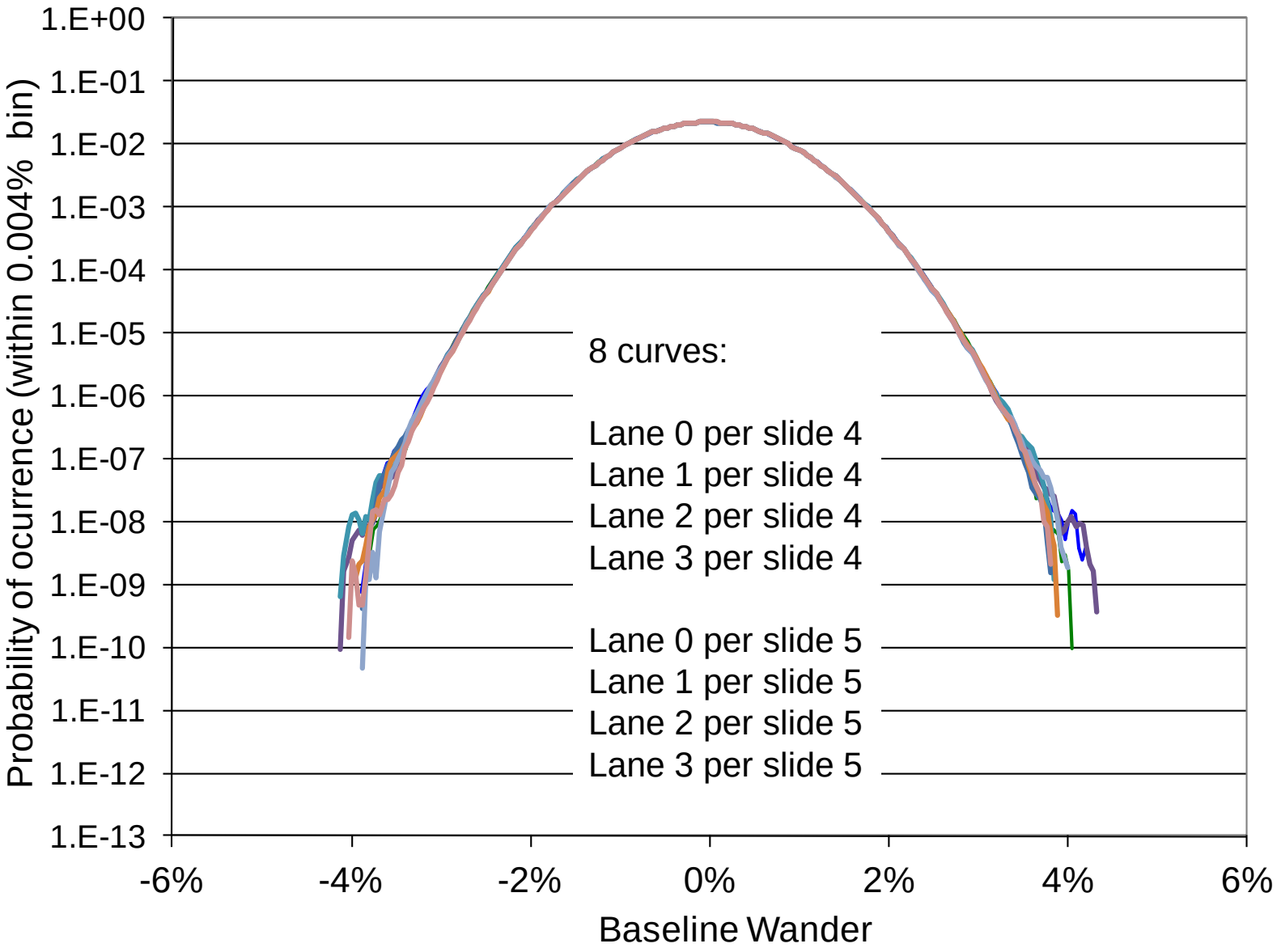
The resulting 14 10-bit parity symbols from RS(528,514,7,10) would be:

1019, 521, 222, 72, 397, 726, 992, 600, 105, 61, 850, 645, 8, 780 decimal

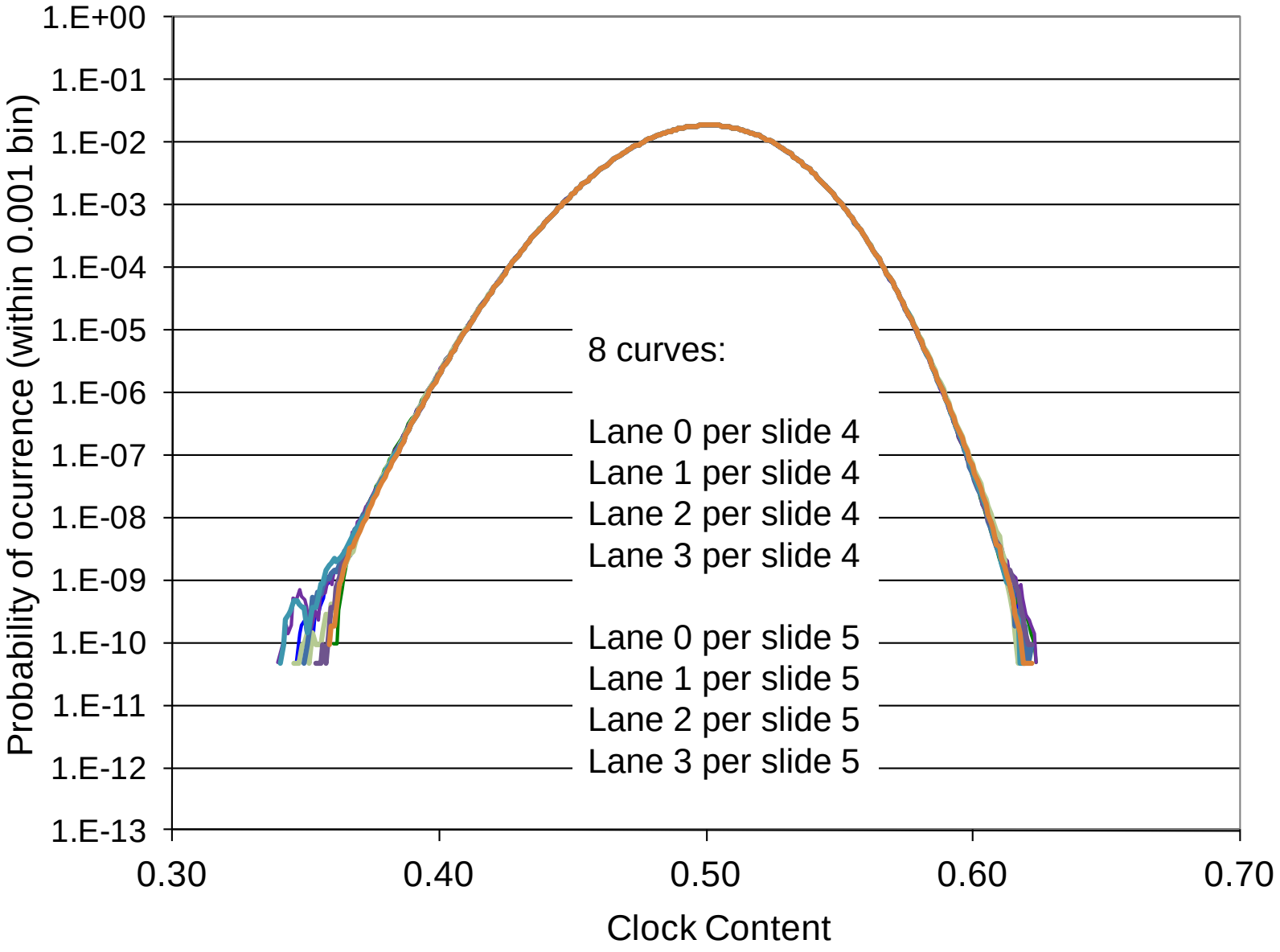
or 3FB, 209, 0DE, 048, 18D, 2D6, 3E0, 258, 069, 03D, 352, 285, 008, 30C Hex

The last of these to be sent (0x30C) would be sent as 0011000011

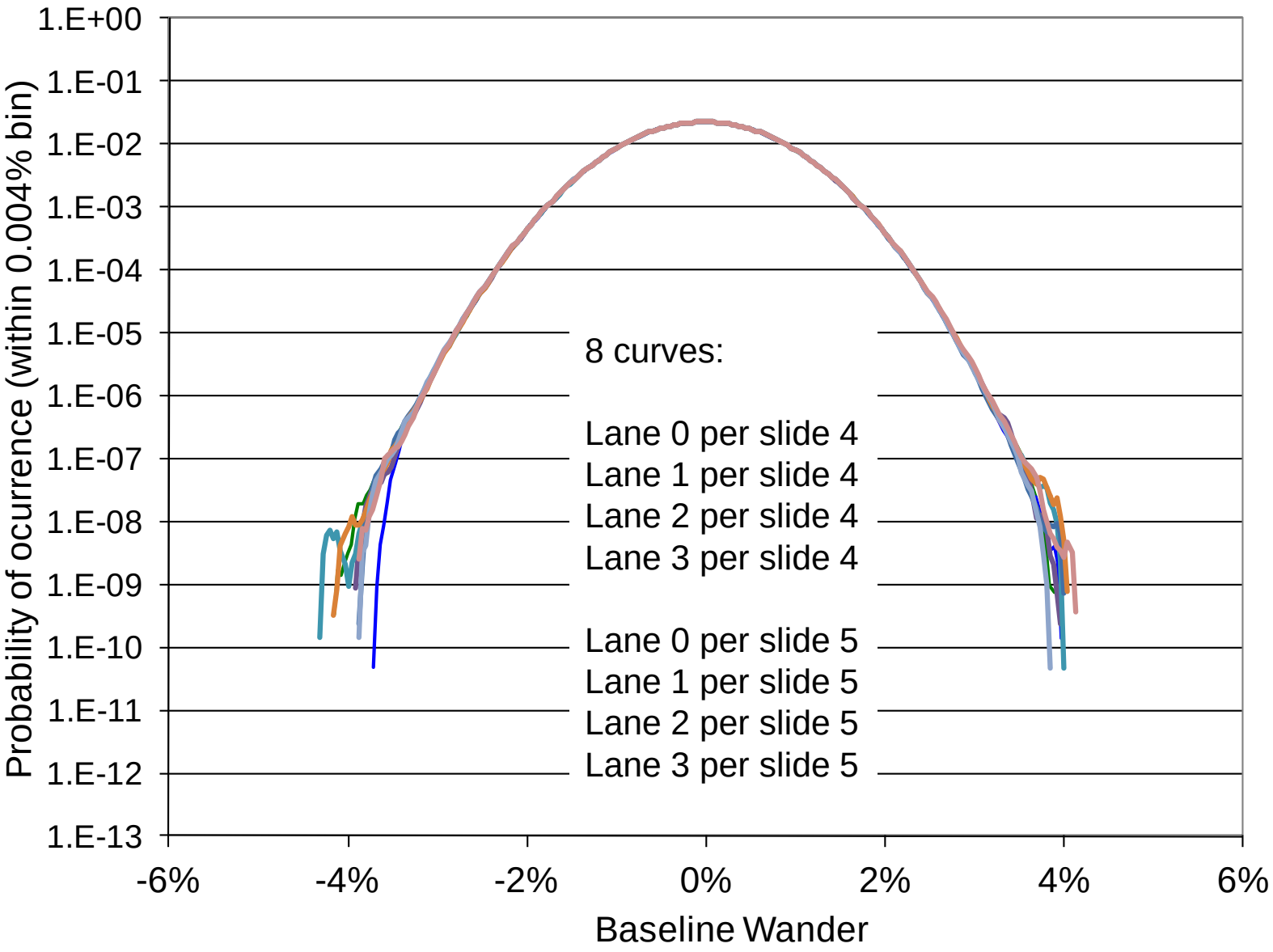
NRZ Idle baseline wander PDFs



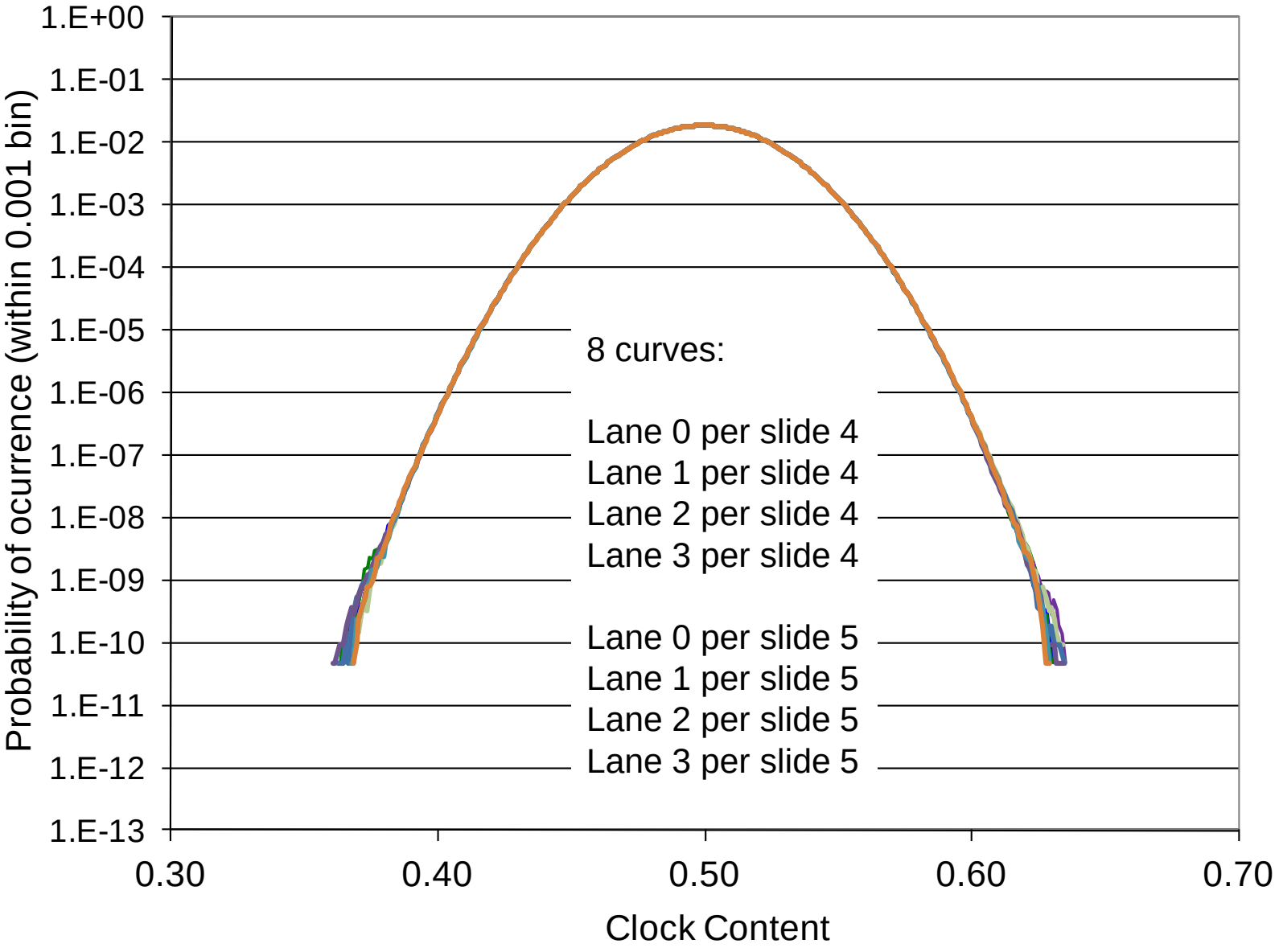
NRZ Idle clock content PDFs



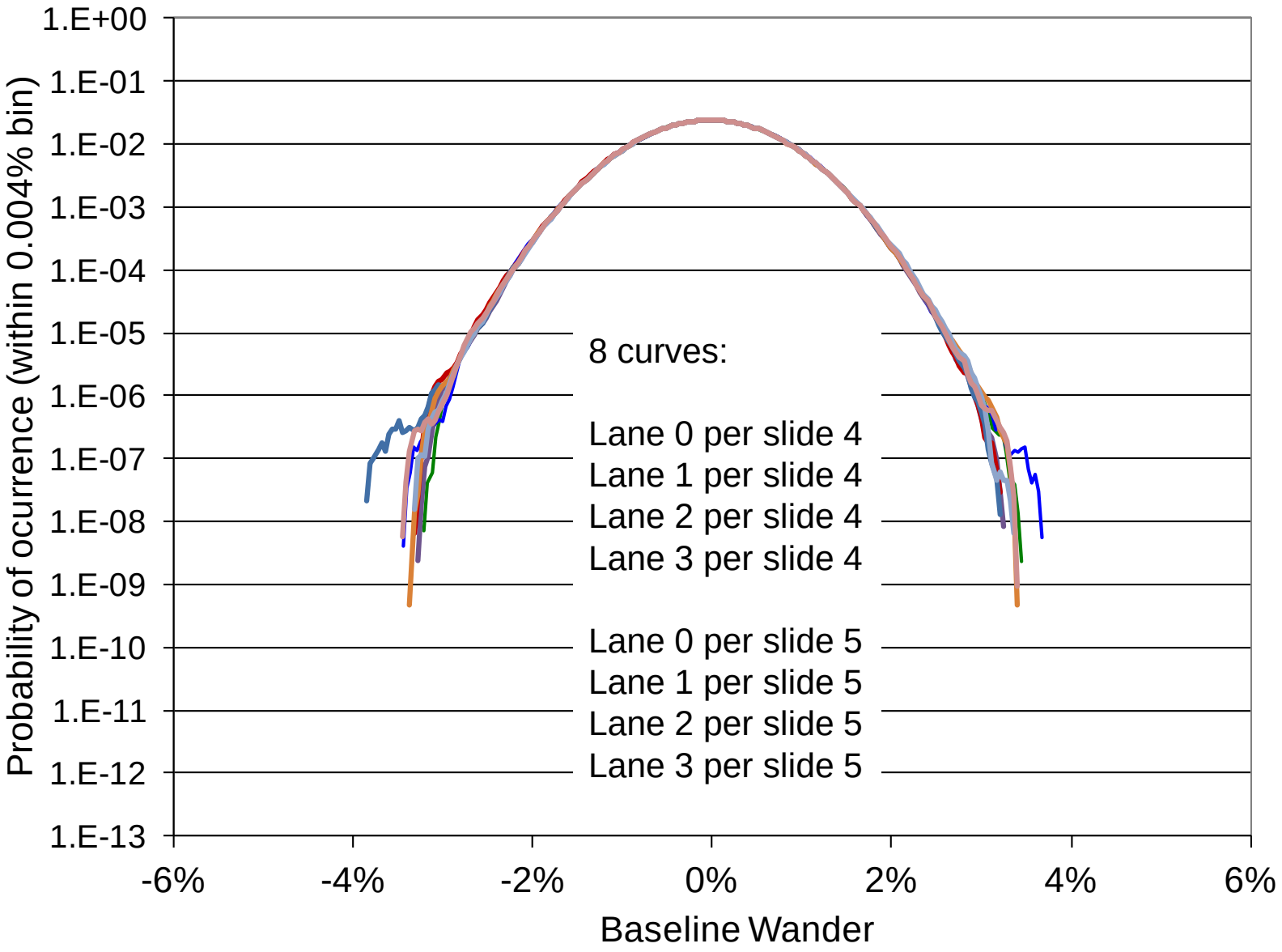
NRZ Random baseline wander PDFs



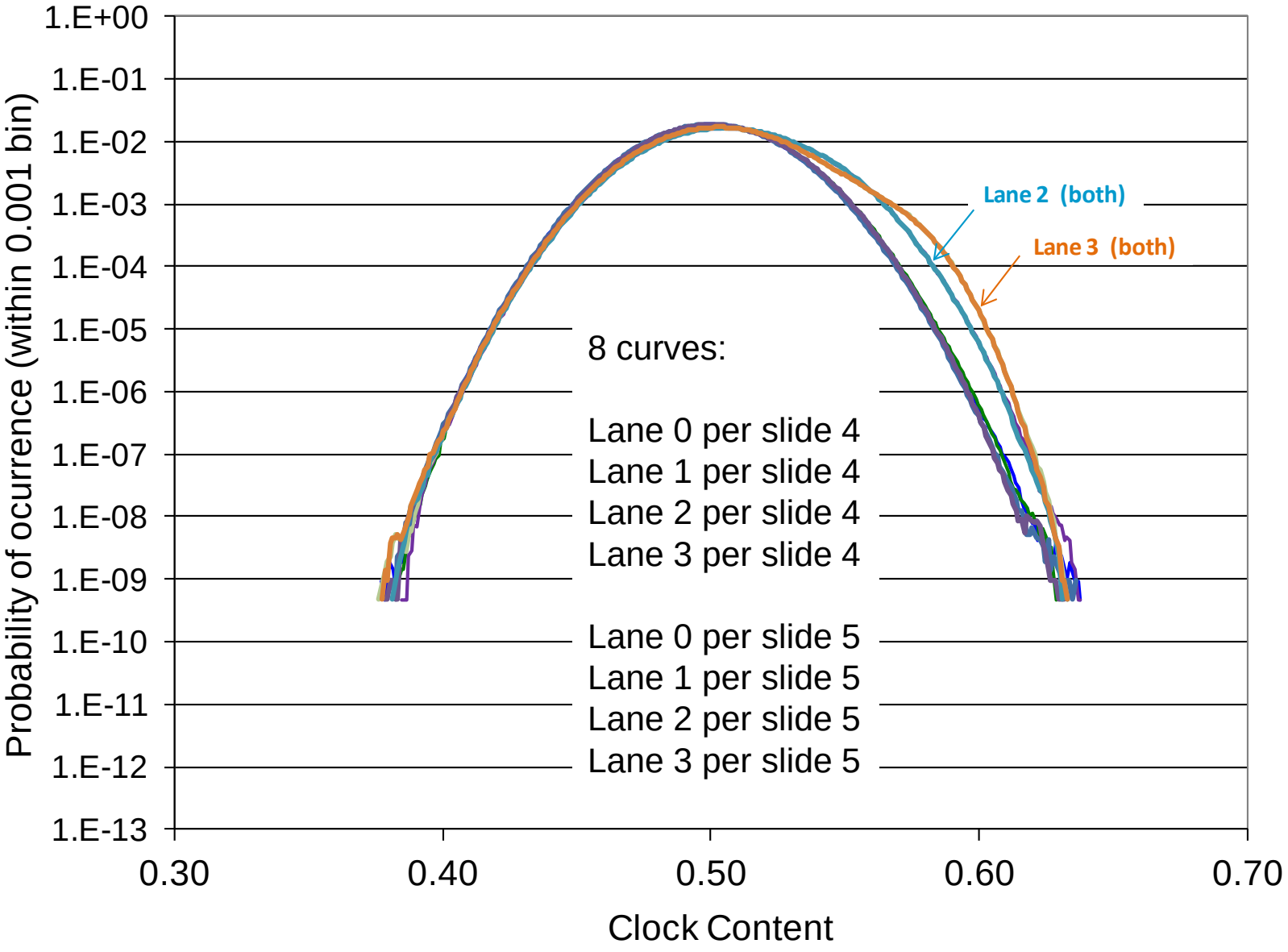
NRZ Random clock content PDFs



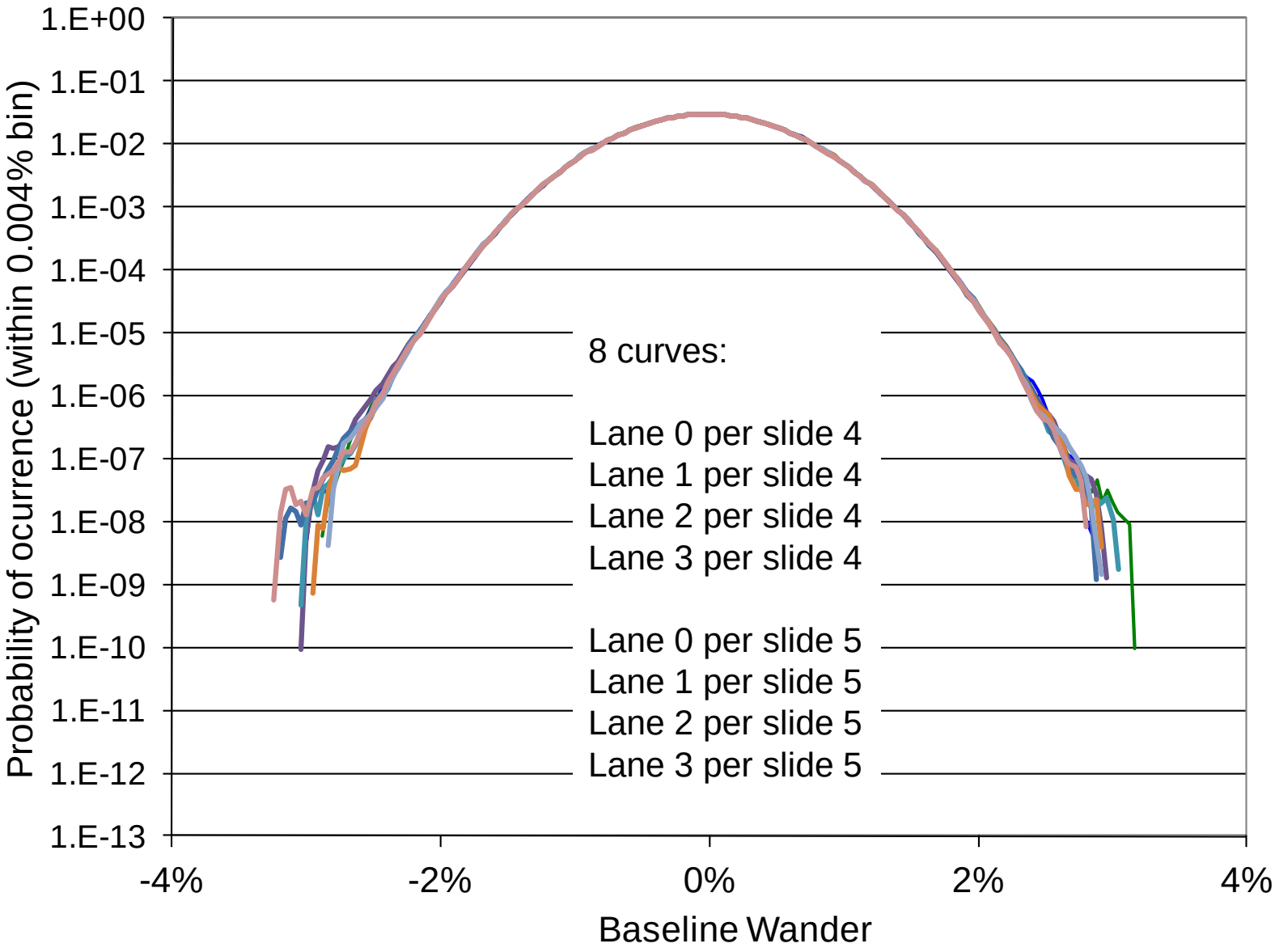
NRZ Idle baseline wander PDFs with RAMs



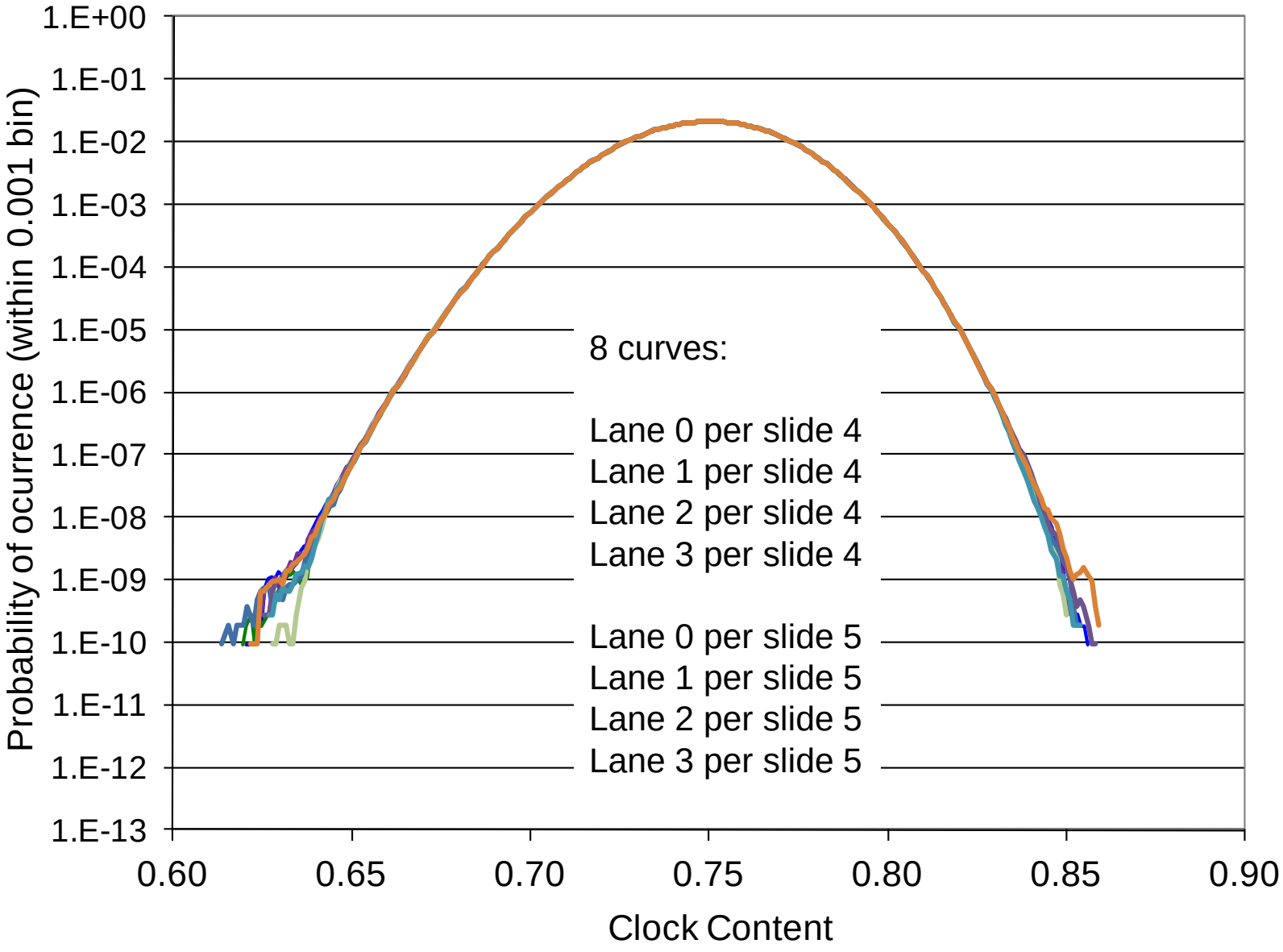
NRZ Idle clock content PDFs with RAMs



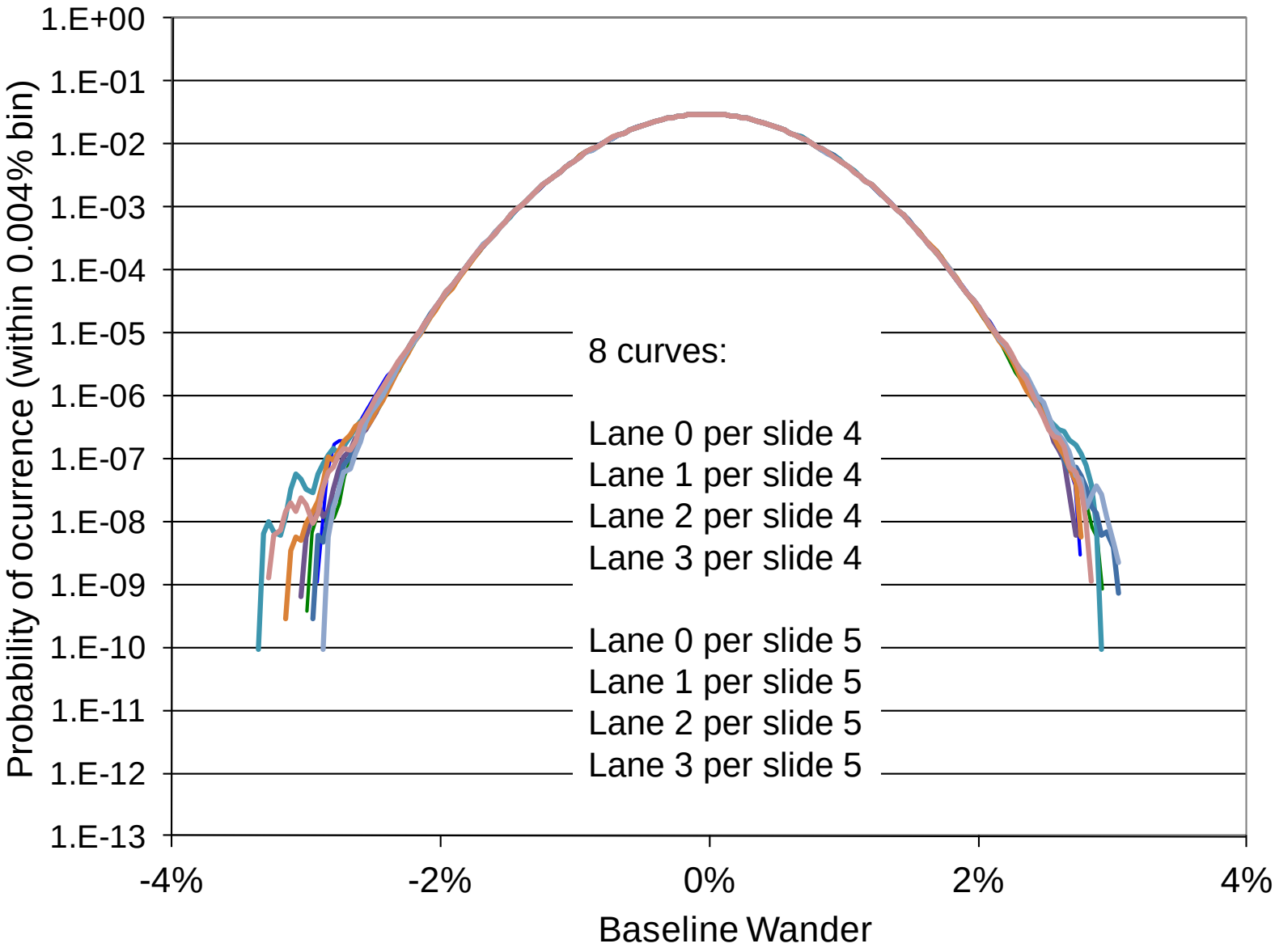
PAM4 Idle baseline wander PDFs



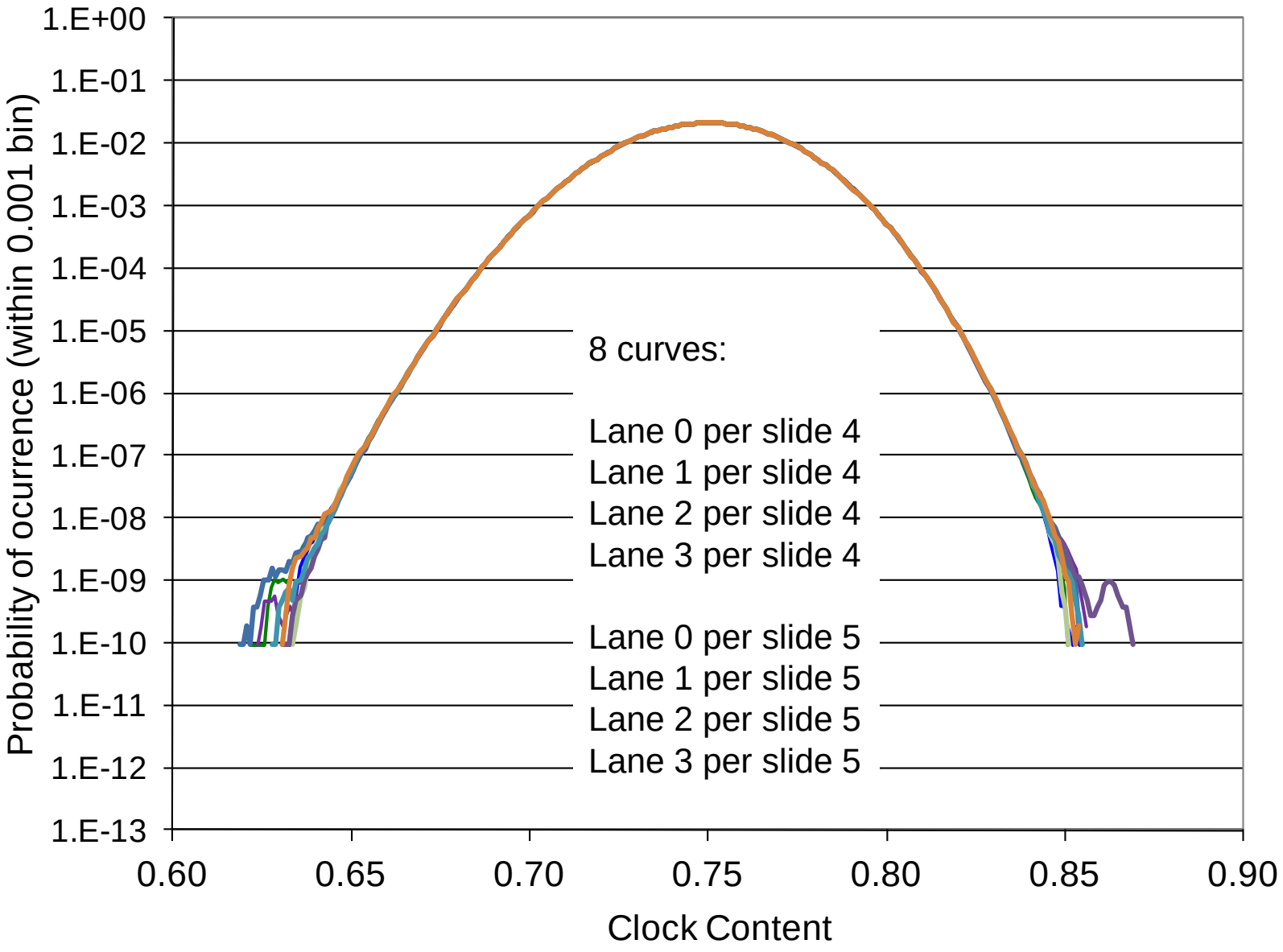
PAM4 Idle clock content PDFs



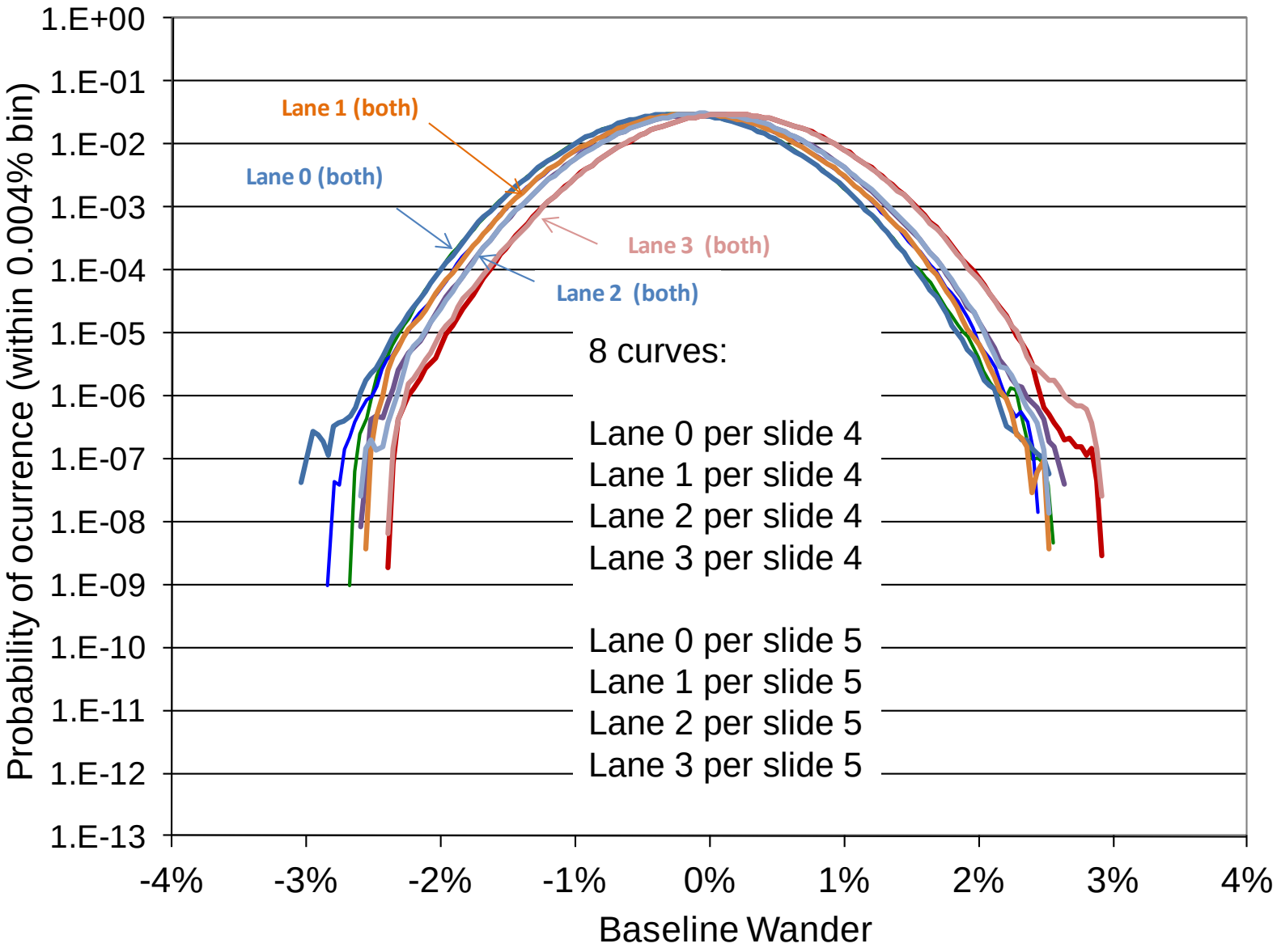
PAM4 Random baseline wander PDFs



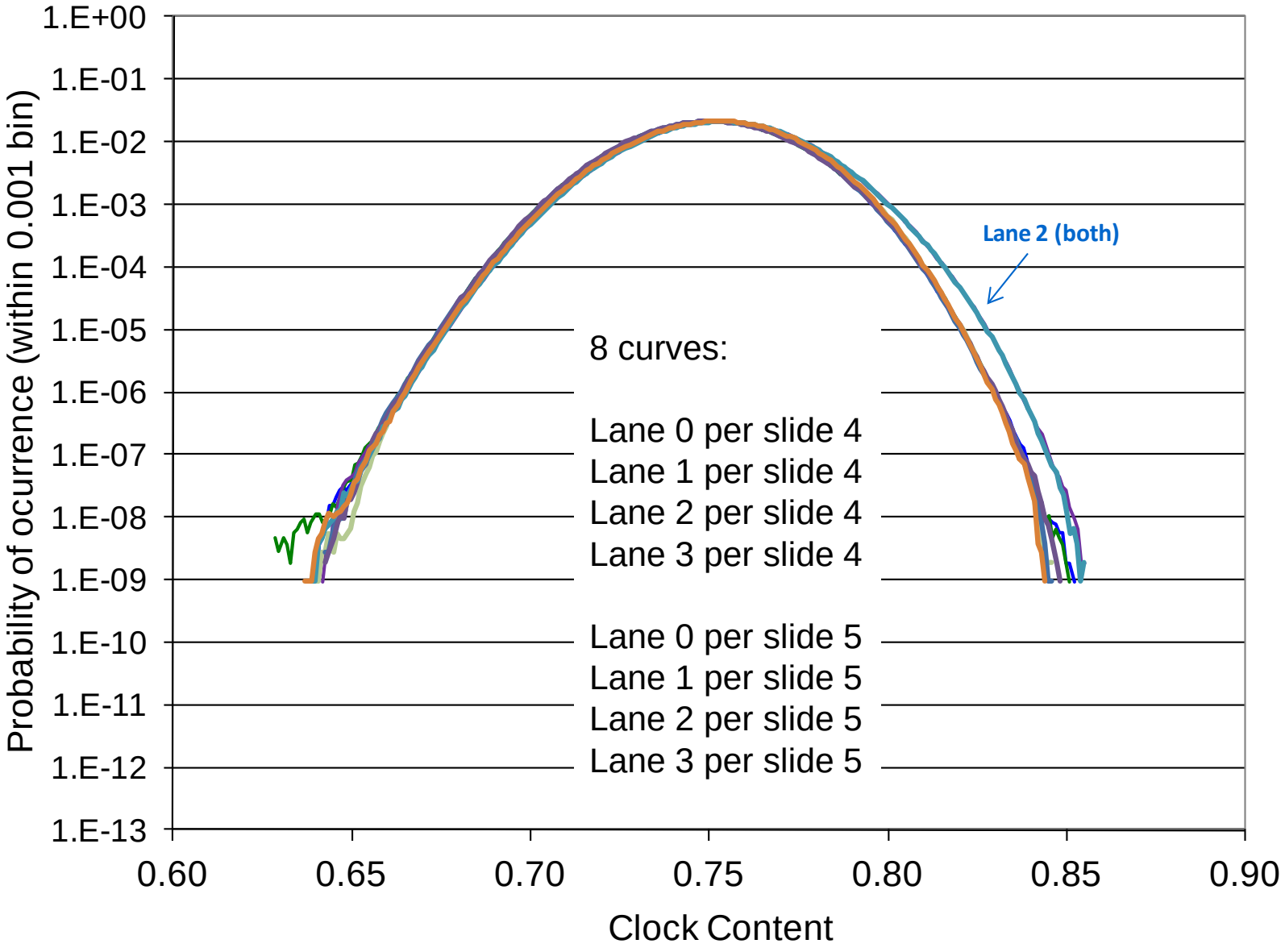
PAM4 Random clock content PDFs



PAM4 Idle baseline wander PDFs with RAMs



PAM4 Idle clock content PDFs with RAMs



Conclusion

The analysis carried out in this presentation has looked at the PDFs for baseline wander and clock content of the four lanes containing random data and scrambled idle both with and without rapid AMs for the architecture in D1.0 (slide 4) and for the alternative architecture proposed in cideciyan_02_0512.pdf but **without** an additive synchronous PN-5280 scrambler after the FEC encoder (slide 5).

There is no discernable difference in the PDFs for baseline wander and clock content between those for the D1.0 architecture and those for the alternative shown on slide 5.

The analysis also included calculating the FEC bits and BIP bits rather than setting them randomly as previously.

The conclusion from this is that if the alternative architecture proposed in cideciyan_02_0512.pdf is adopted, then there is no need for the additive PN-5280 scrambler and that for either architecture the FEC parity bits do not need to be scrambled.

Thanks!