

# Adhoc Discussion Defining Test Points in a Copper Back Plane / Mid Plane Implementation

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Summary: This presentation will describe possible test points and begin discussion of a Normative Channel Definition.

# Outline

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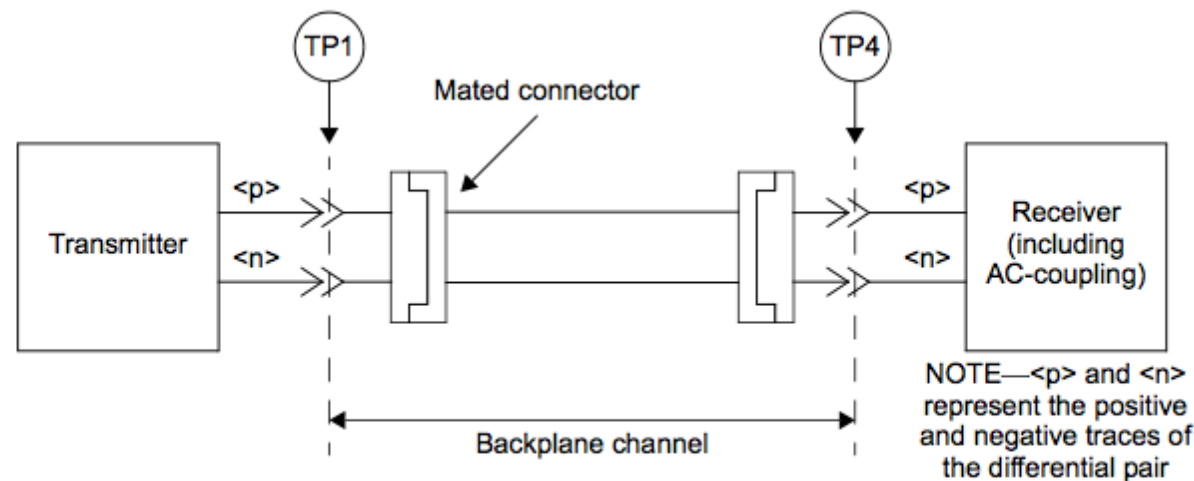
- ▶ Review test points from IEEE802.3ap
- ▶ Review proposed P802.3bj cabling test points
- ▶ Discuss the location of the cap
- ▶ Discuss the location of the test points

# Reference P802.3ap-D33.pdf Feb21, 2007

## 69B.2 Reference model

The backplane interconnect is defined between test points TP1 and TP4 as shown in Figure 69B-1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

Informative characteristics and methods of calculation for the insertion loss, insertion loss deviation, return loss, crosstalk, and the ratio of insertion loss to crosstalk between TP1 and TP4 are defined in 69B.4.3, 69B.4.4, 69B.4.5, 69B.4.6, and 69B.4.6.4 respectively. These characteristics may be applied to a specific implementation of the full path (including transmitter and receiver packaging and supporting components) for a complete assessment of system performance and the interaction of these components.



## P802.3bj test point specifications

- Adopt Figure 85-2 and Table 85-4 as baseline for 802.3bj with applicable changes for naming transmit and receive functions and figure and clause numbering.

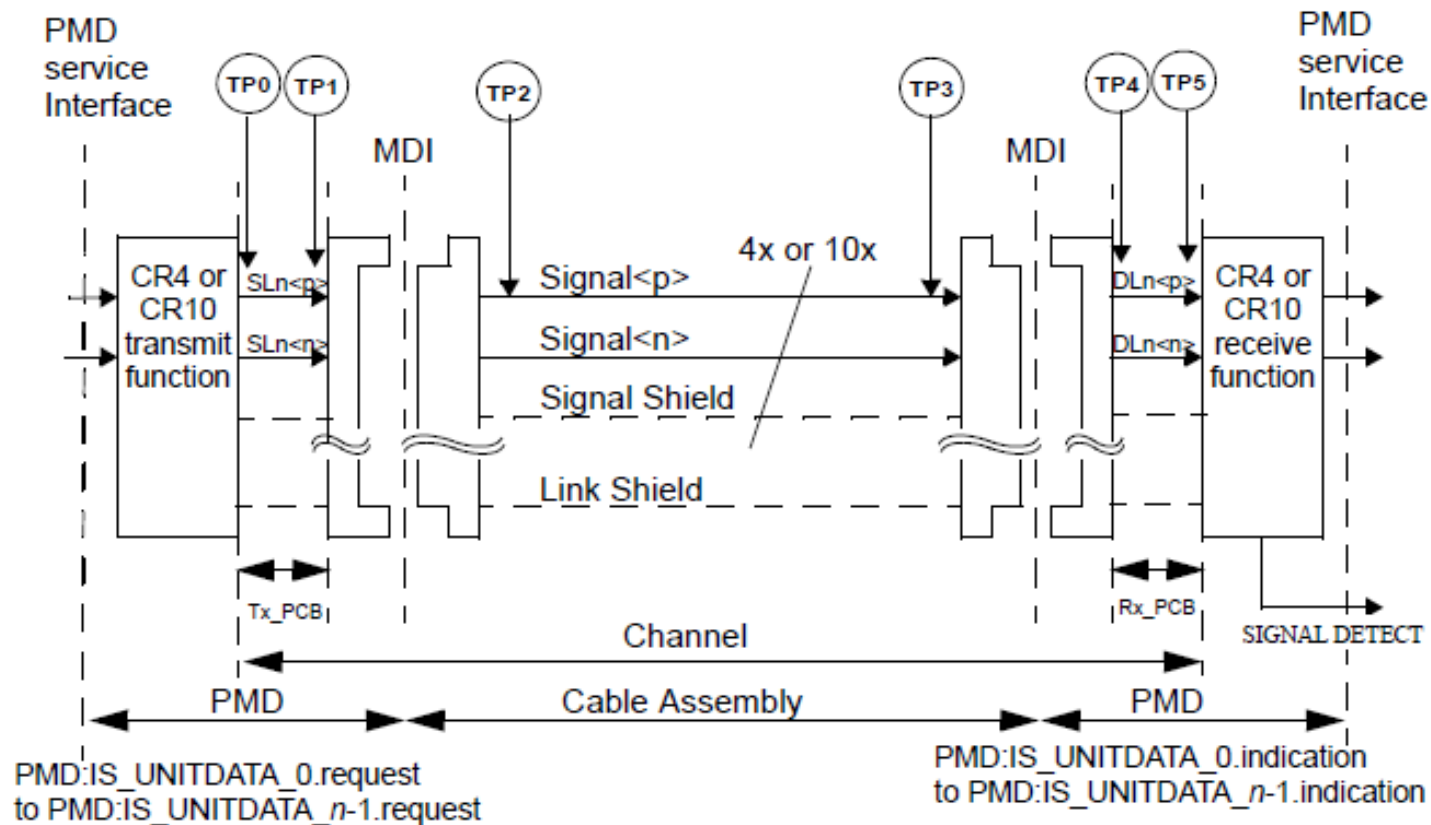
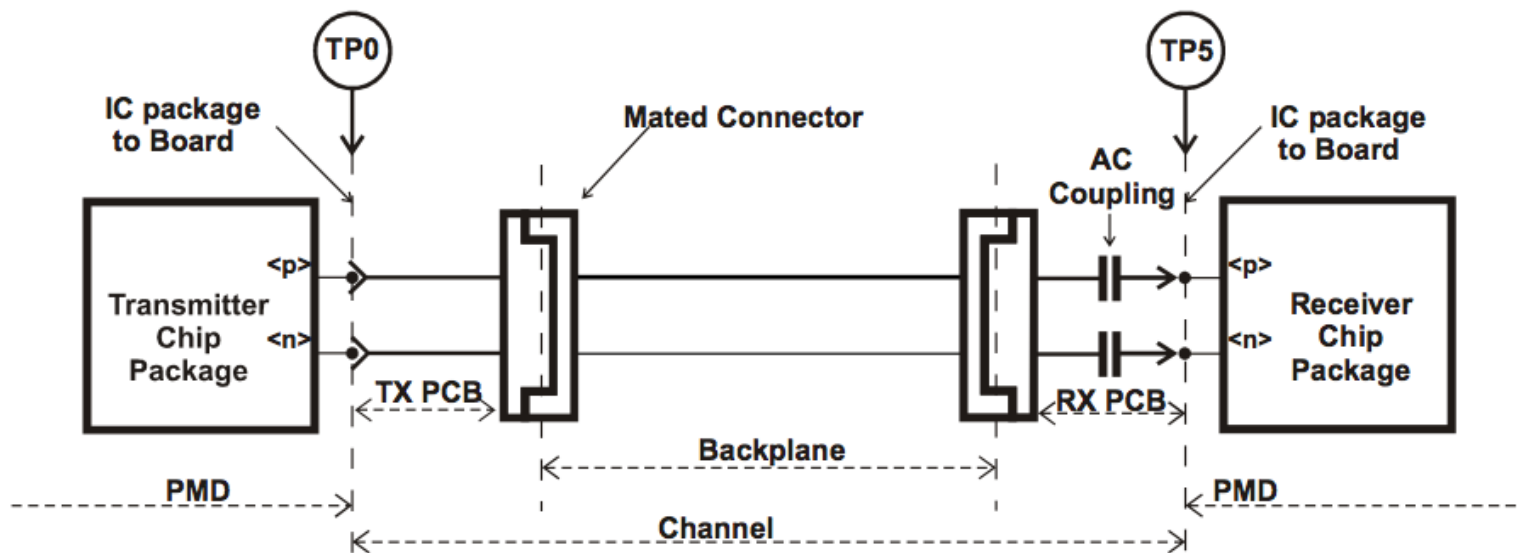


Figure 85-2—40GBASE-CR4 or 100GBASE-CR10 link (half link is illustrated)

# Back Plane Test Point Proposal from Jan 2012

## Recommended backplane test points



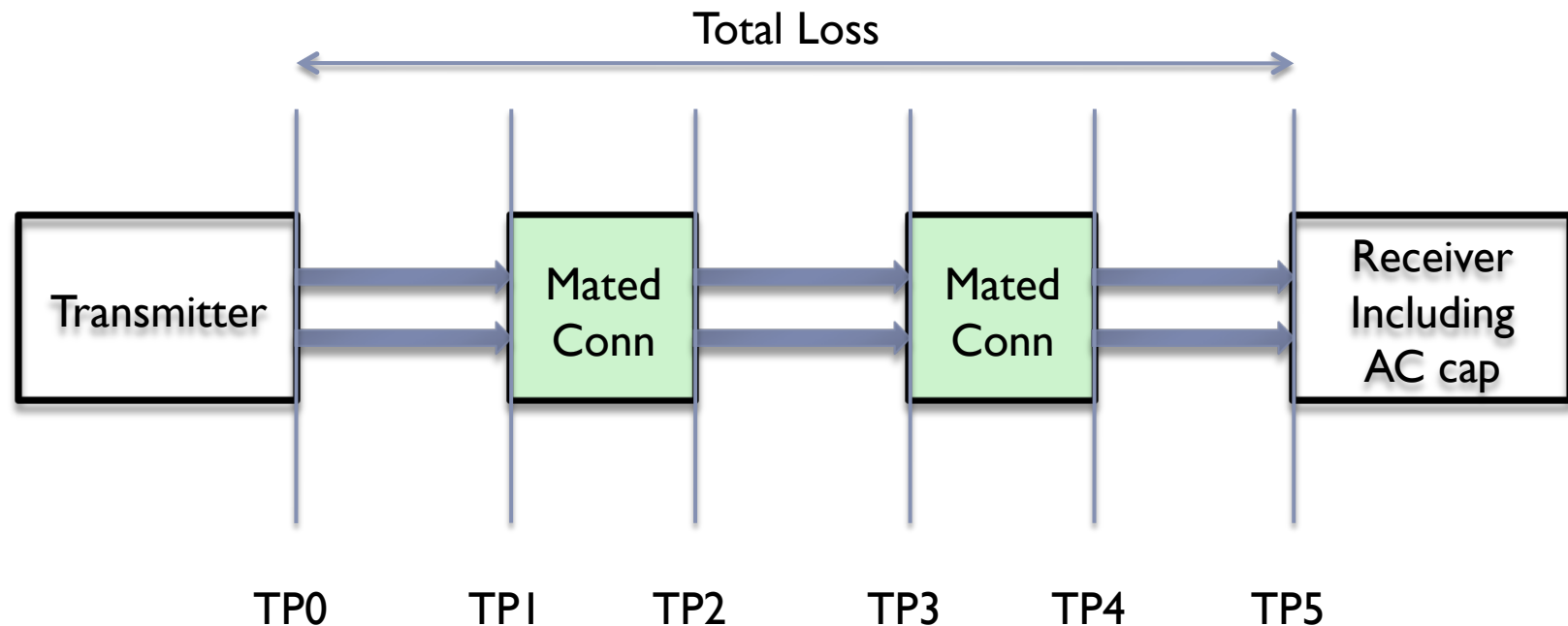
### Considerations:

- Aligned with the cable specification
- TP0 and TP5 defined; rationale on next slide

# Back Plane Test Point Proposal

Goergen\_01\_0312

- ▶ Propose using diminico\_01a\_0112.pdf as the basis for the back plane channel with the terms adjusted relevant to back plane.
- ▶ Propose the Capacitor function be owned by the receiver as in P802.3ap.



# Define the DC Blocking Capacitor Location

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- ▶ **Location**
  - ▶ In the connector – not in massive volumes until 2013
  - ▶ On the motherboard – it won't fit in many applications
  - ▶ In the chip as electronic equivalent – tighter common mode specifications
  - ▶ In the barrel – expensive and not mass producible
  - ▶ In the board – expensive and difficult to control the process
- ▶ **Channel Testing and Verification**
  - ▶ Test systems usually bypass the blocking cap
  - ▶ 3<sup>rd</sup> party blocking is typically used to isolate the scope or bert equipment
  - ▶ Not a lot of public work has been done to define the loss budgets of the cap
- ▶ All the above is mostly why we ignore the cap and assume it's part of the receiver
- ▶ If we want to recognize the cap ...
  - ▶ Define the test points accordingly
  - ▶ Provide for the additional margin in the channel (ie add 2dB onto the 35dB loss)
  - ▶ Know that there are applications that will place the cap in the receiver so we have to allocate the loss budget accordingly.



# Defining a Testable Channel

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- ▶ Establish TP0 – TP5 locations.
  - ▶ There would be more test points if the capacitor is allocated to the channel.
- ▶ Define test fixtures using TP0 – TP5 that allow measuring and isolating TP0 – TP2, TP1 – TP4, and TP3 – TP5.
- ▶ Allows for test and verification of the channel independent of the transmitter, transmitter package, receiver, and receiver package.
  - ▶ Removes the need for advanced vendor models
  - ▶ Removes the need to share channel models with vendors
  - ▶ Reduces system testing and verification