Proposal for 100G-KR4 Channel Specification

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Outline

- Motivation
- Proposal overview
- Input Definitions
- Reference Architecture Definition
- Optimization proposal
- Pass/Fail proposal

Motivation

- **Previous method of specifying channels through frequency domain magnitudes only of IL, ICR, and ILD is not well suited for the PAM-4 channel**
  - E.g., if ILD of +/-3dB is not 'equalizable', it can create a slot SNR floor of 7.6dB
  - It's not possible to know if an ILD is 'equalizable' without knowing the phase of the IL and the capabilities of the equalizers
- **Major desire is to have the Channel Specification better match whether or not a real implementation achieves acceptable performance with the channel**
  - Time domain information (or equivalently frequency domain magnitude and phase information) is needed to better predict performance
  - The strong FEC needs to be included
- **The most straightforward method is to define a 'reference architecture' consisting of TX, RX and noise impairments**
  - Easier to translate 'reference architecture' performance to a real architecture than it is to translate current frequency domain 'masks'
  - The alternative of improving the current specifications of IL, ICR, and ILD looks difficult to achieve, and difficult to determine success
    - Success is determined by correlation with a … reference architecture!
    - So need an agreed reference architecture to start. Why go further?

Input Definitions

- **The desired signal (IL) and Cross Talk ‘signals’ are all input as time domain signals**
  - M times oversampled data (e.g., M=4)
  - We can optionally provide ‘non-guaranteed’ courtesy tools to translate s-parameter descriptions into time domain
  - Note that frequency domain magnitude and phase can trivially be converted to time domain waveforms
- **{need to determine how to include effects of chip / package Z that are not normally in the measured ‘channel’} {should we define a reference package and chip input Z ?}**

Reference Architecture proposal

- TX output level (e.g., tightened range?)
- TX de-emphasis FFE (e.g., 1 pre and 1 post tap)
- TX distortion & noise emulation block (e.g., Additive noise of distribution W)
  - Separate spec for TX linearity is 'emulated' here
- PGA input thermal noise emulation (e.g., AWGN)
- PGA & CTLE (e.g., a fixed constellation, or 1 or 2 degrees of freedom)
- Analog output distortion + noise emulation (e.g., Additive noise of distribution Y)
- FFE (e.g., 32 tap)
- DFE (e.g., 1 tap FBF)

- TBD including Random jitter in the 'channel spec'

Optimization of Reference Architecture

- **The reference architecture must be 'optimized' for the channel under test**
- **We want a fast and simple optimization that is 'reasonably close' to the true optimal**
  - Needs to be fast if we need to sweep TX and CTLE parameters, etc
- **Proposal**
  - TX and CTLE can be jointly optimized by an exhaustive search of all combinations (with relatively coarse parameterization of pre, post, peaking, etc.)
  - Treat all noise distributions as if they were Normal for the purpose of optimization of FFE and DFE, which can then be simply solved with linear equations
  - Chose 'optimal' as MMSE using Normal
- **Alternate 1 proposal**
  - Choose TX FFE and CTLE to maximize Salz SNR assuming Normal. Single FFE/DFE design for that 'optima'

Evaluation of 'optimized' Reference Architecture

- **Find worst case time delays for each of the cross talk channels**
  - TBD details. One at a time search for worst case, etc.
- **For the 'optimized' parameters chosen and the worst case time delays above, calculate the before FEC Error Event Rate by calculating the 'true PDF' at the slicer**
  - Per Adee Ran paper
- **Pass / Fail EER criteria set to achieve < 1e-12 bER after FEC**
  - TBD if other 'margins' should be applied here?
  - Margin can also be achieved by setting some noise parameters larger than expected real implementations

Summary

- Time domain information on IL and all Cross Talkers is required and used to qualify channels
- A proposal to specify qualifying channels by their performance on a reference architecture is presented
- A fast computational technique that is reasonably accurate is proposed for pass/fail testing
- Once a reference architecture is agreed upon, then we're in position to evaluate other analytic methods if desired