Summary
Defining Test Points in a Copper Back Plane / Mid Plane Implementation

Joel Goergen – Cisco

April 25, 2012

Summary: This presentation will present an opinion of how to deal with the DC blocking capacitor.

Review

- Capacitor is <= 1dB at 12.89GHz
- Capacitor is <= .5dB at7GHz
- Capacitor, VIA Structure, and Lands are <= 4.5dB at 12.89GHz.
- Capacitor, VIA Structure, and Lands are <= 1.5dB at7GHz.

Recommendation

- Leave the Capacitor as was in P802.3ap, allocated to the receiver. No new test points are required for the capacitor.
- Compensate the loss budgets such that the capacitor is placed in-line the connector or on-die / on-package the receiver, providing for a less then 1dB margin allocation over the total loss budget.
- This assumes the margin allocation of up to 4.5dB at 12.89GHz is too high, and therefore, the capacitor (4via+4pad+2cap) can no longer be allocated as moveable budget in the channel.
- This allows us to assume a reasonable budgeted loss for the capacitor (1dB at Nyquist), without forcing a channel allocation or forcing an design implementation. Preserves IL, ILD, RL, and ICR methods.

Recommendation

- **Per Dudek_00_0412__ACcapPositionThoughts**
- **Locate the test points at the BGA balls (or offset by a specified test board loss.)**
- **Include the effects of the AC coupling capacitor in the channel**
- **Leave the position of the AC coupling capacitor within the channel open but recommend that it is placed at the Rx end**
- Requires test points to characterize the effects of the capacitor in the channel so it may be tested.
- Must account for additional ILD and crosstalk effects not measured currently in the channel.
- IEEE802.3 has more defined documentation then OIF. If the capacitor goes into the channel as 4via+4pad+2cap, then the loss budget should be specifically defined so the designer knows how the IL, ILD, RL, and ICR will effect the total loss budget allocated.

Reference P802.3ap-D33.pdf Feb21, 2007

69B.2 Reference model

The backplane interconnect is defined between test points TP1 and TP4 as shown in Figure 69B–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

Informative characteristics and methods of calculation for the insertion loss, insertion loss deviation, return loss, crosstalk, and the ratio of insertion loss to crosstalk between TP1 and TP4 are defined in 69B.4.3, 69B.4.4, 69B.4.5, 69B.4.6, and 69B.4.6.4 respectively. These characteristics may be applied to a specific implementation of the full path (including transmitter and receiver packaging and supporting components) for a complete assessment of system performance and the interaction of these components.

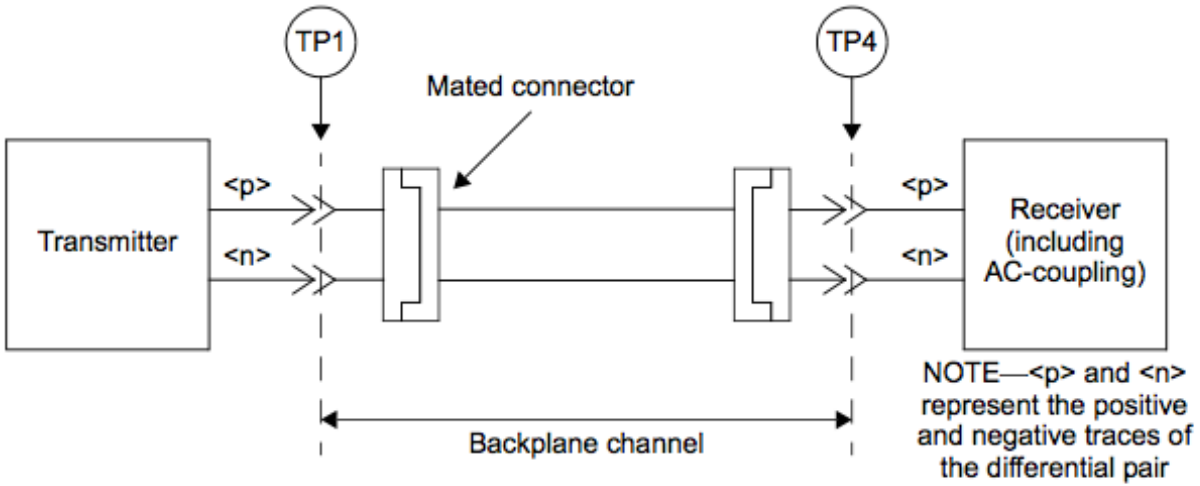

Figure 69B–1—Interconnect reference model

Back Plane Test Point Proposal Goergen_01_0312

- Propose using diminico_01a_0112.pdf as the basis for the back plane channel with the terms adjusted relevant to back plane.
- Propose the Capacitor function be owned by the receiver as in P802.3ap.