



DC-Blocking Capacitor impact @ 802.3bj lane rate

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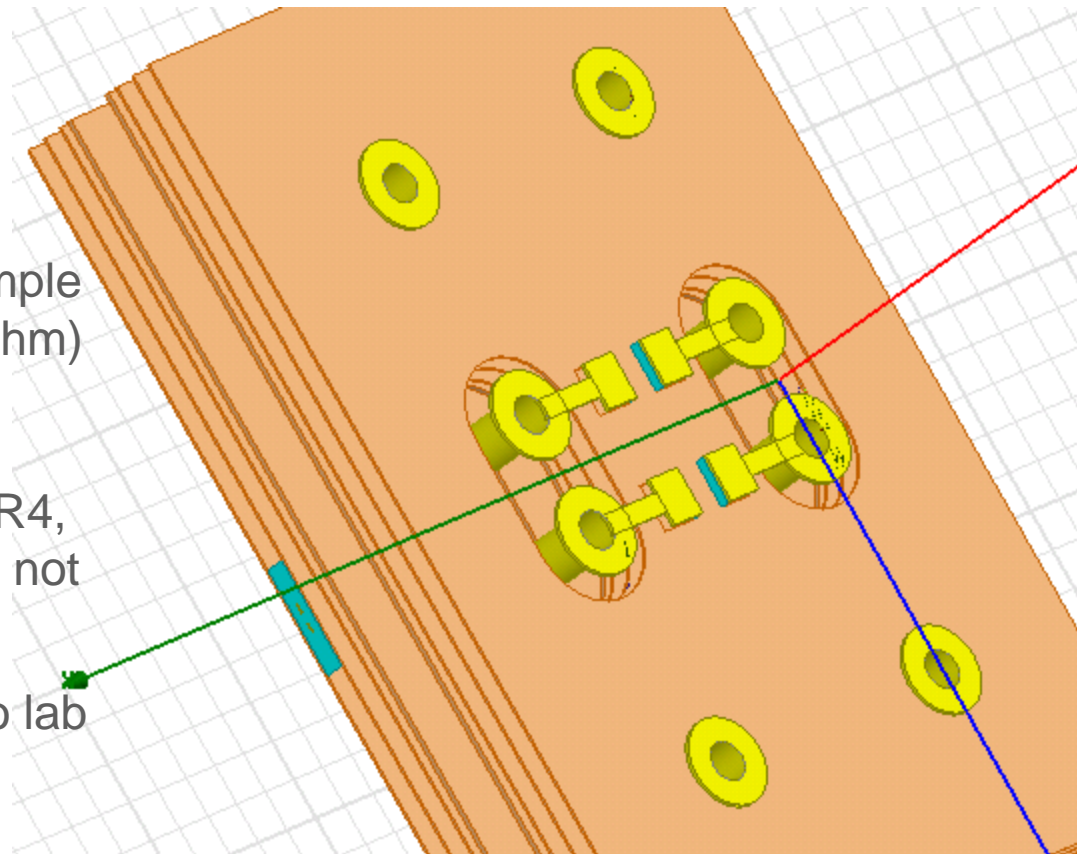
April 2012

Agenda

- DC blocking capacitor vias
- DC blocking vias impact on several interconnects
- Observations

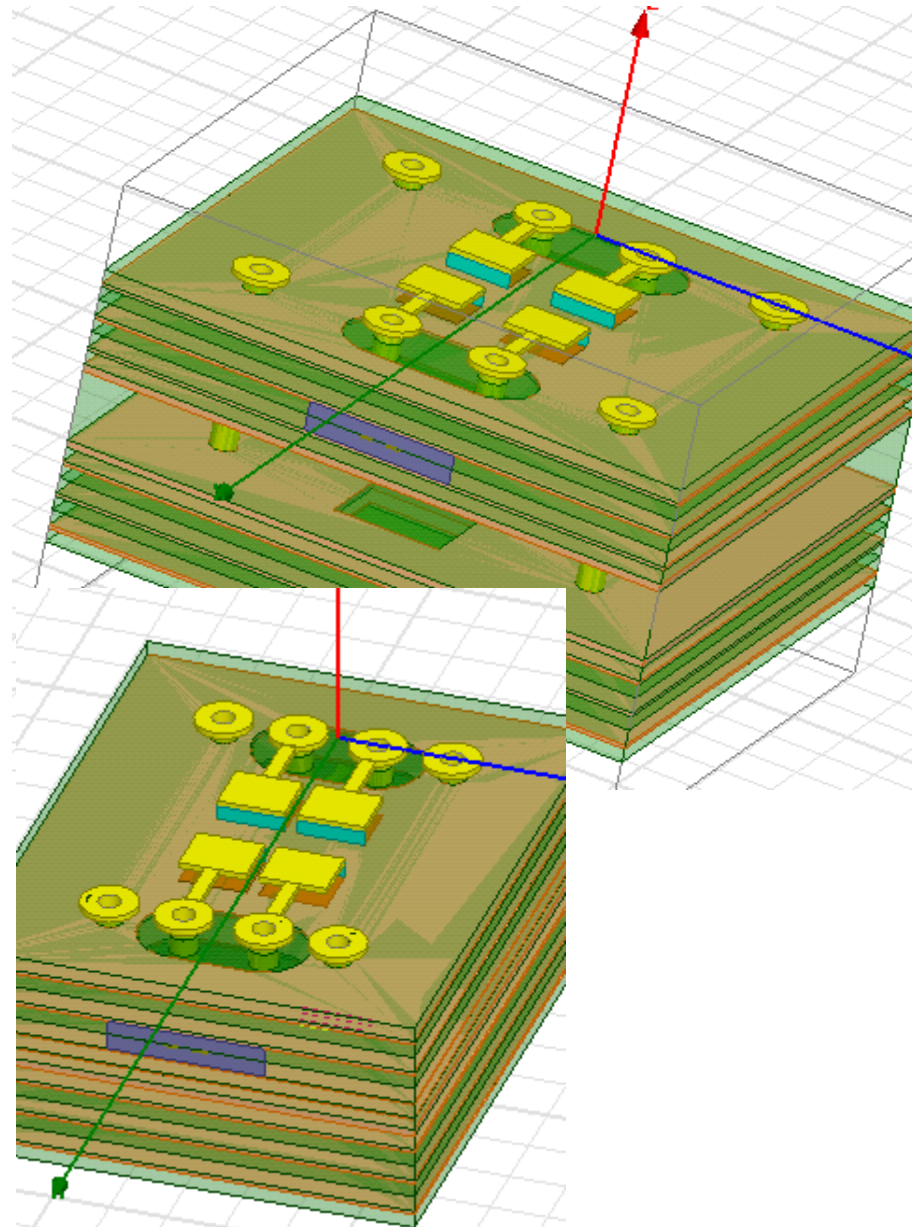
DC block construction, Assumptions and Limitations

- Vias were chosen to have a stub of 12mil-15mil
- 10mil barrel ; 20mil pad (un-used pads removed) ; 32mil anti-pad + joined differential anti-pad.
- Board thickness ~100mil
- Void underneath capacitor pads
- DC blocking capacitor was a simple LR (ESL = 0.4nH ; ESR = 0.04ohm)
- Traces de-embedded.
- Material was altered between FR4, Meg4 and Meg6 (results of FR4 not shared here)
- The model was not correlated to lab measurements.



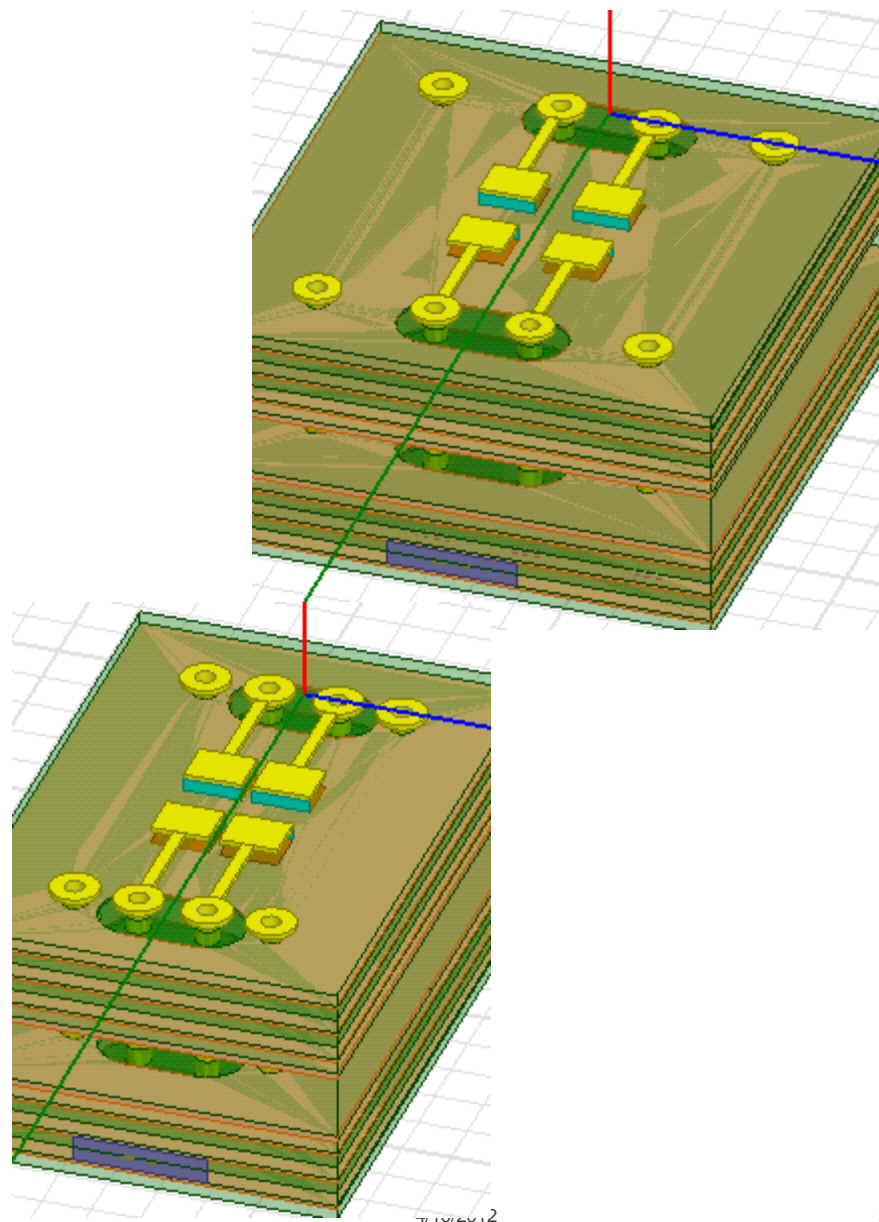
Short_Vias

- Routing on 5th, layer
- Vias length = 26mil Layer1 to 5
- Stub length = 12mil - 15mil
- Via pitch was altered to emphasis extra capacitance influence.



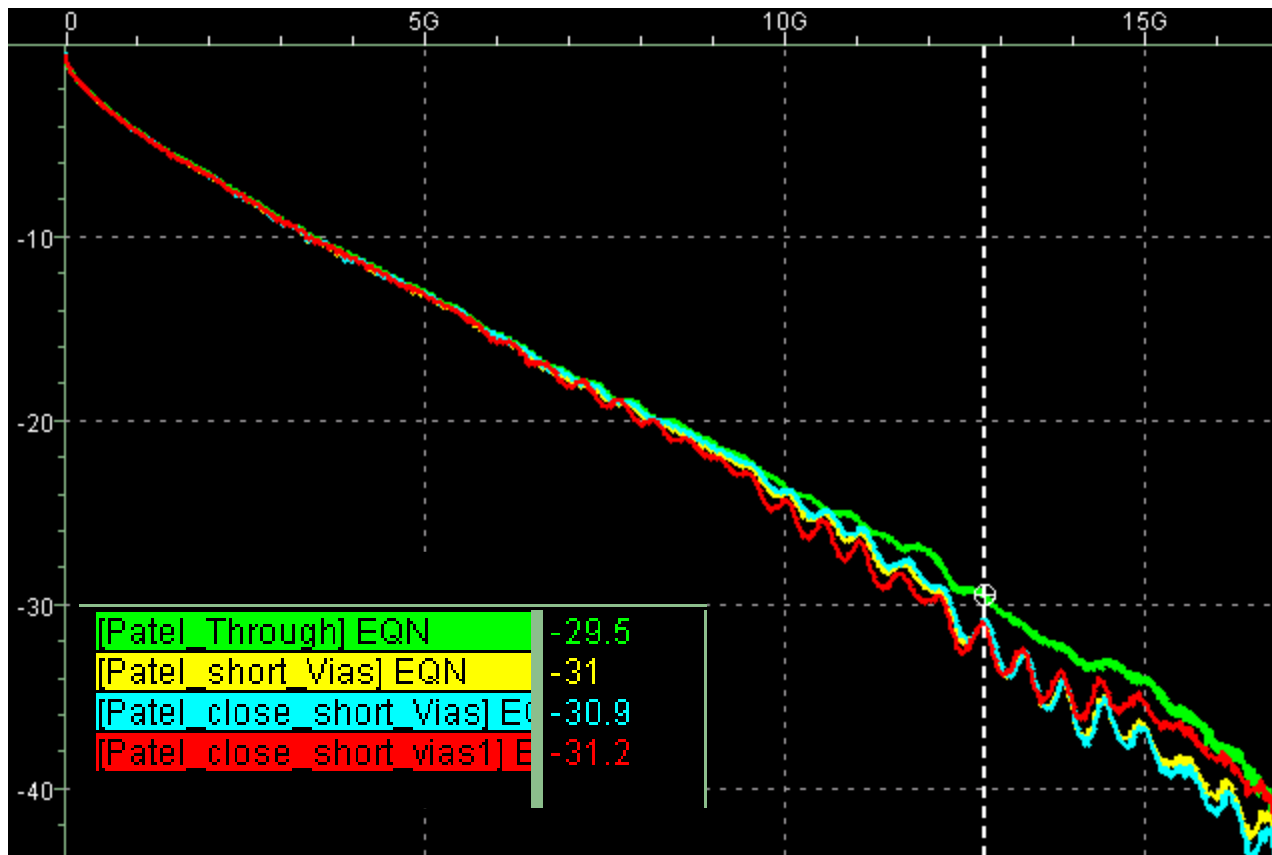
Long_Vias

- Routing on 12th, layer
- Vias length = ~90mil Layer1 to 12
- Stub length = 13mil
- Via pitch was altered to emphasis extra capacitance influence.



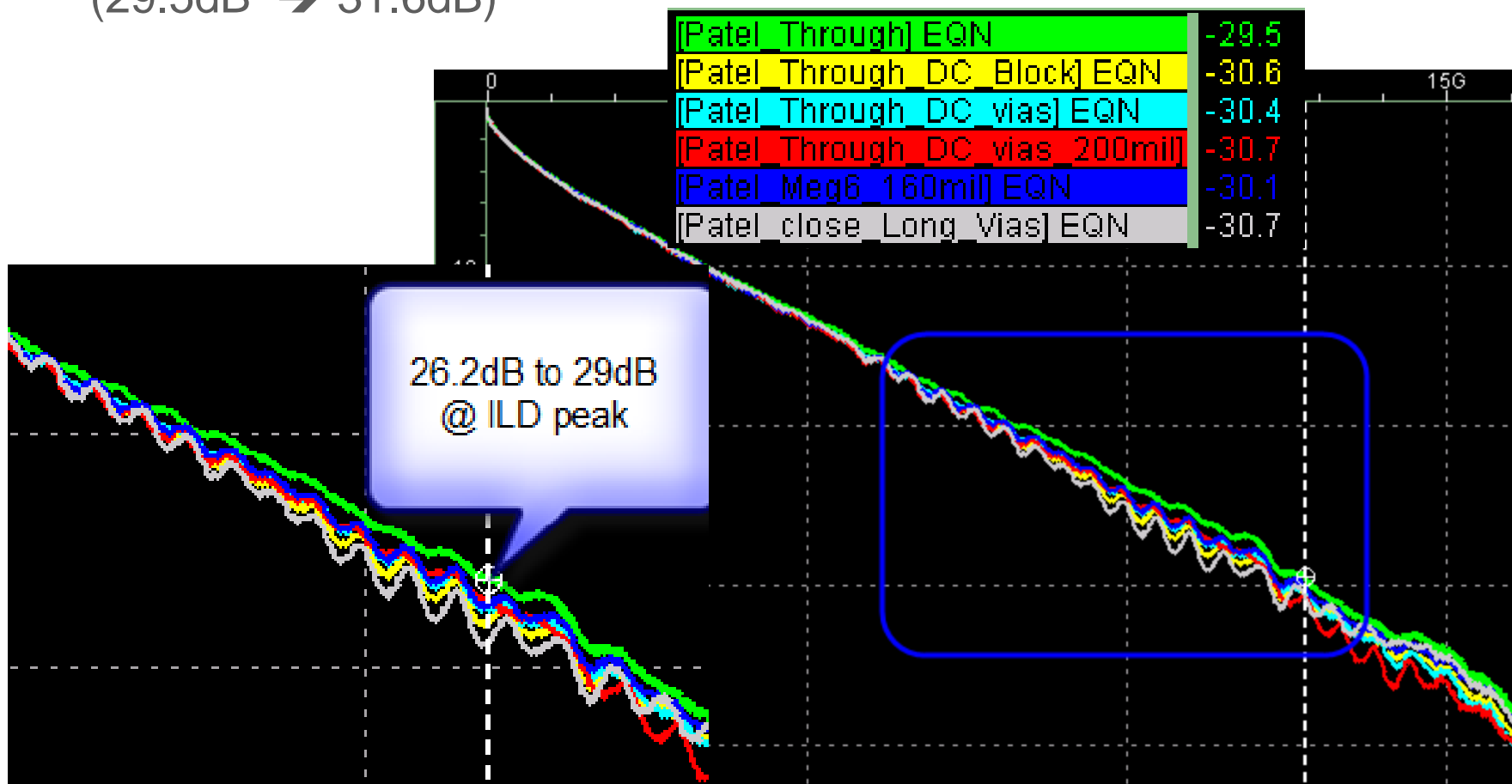
Short Via DC block Influence on “patel_03_0911THRU”

- Interconnect was used to perform analysis on patel_01a_0911.pdf
- Added ILD + 1.7dB loss @ Fb/2 (29.5dB → 31.2dB)



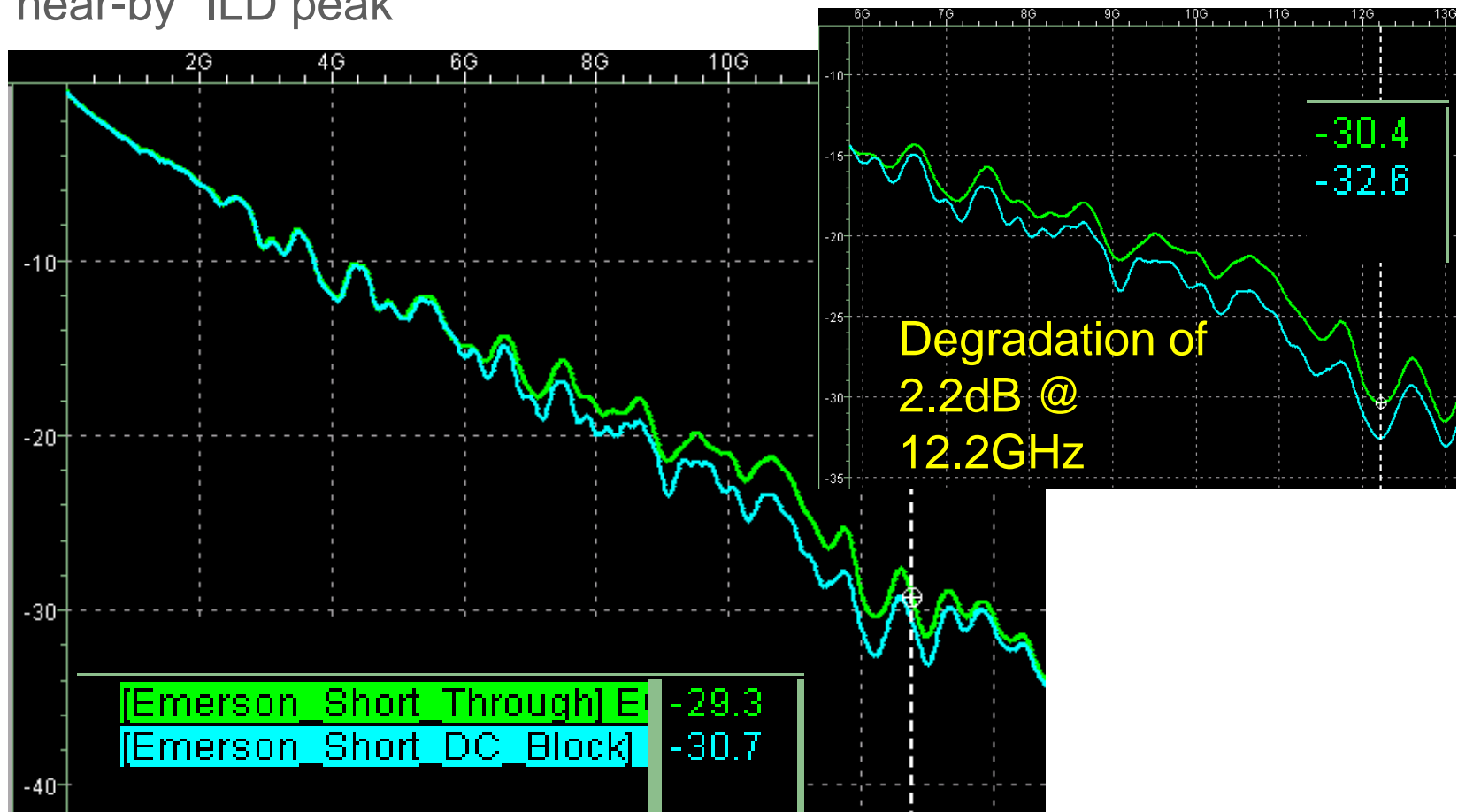
Long Via DC block Influence on “patel_03_0911THRU”

- Interconnect was used to perform analysis on patel_01a_0911.pdf
- Added ILD (degradation as high as 2.8dB) + 1.2dB loss @ Fb/2 (29.5dB → 31.6dB)



Emerson Short Channel Response

- Thru_S07-P23-02-AB_S09-P23-02-CD_NNN.s4p (as analyzed on meghelli_01_0112) – Added 1.4dB of loss @ Fb/2 and 2.2dB @ a “near-by” ILD peak

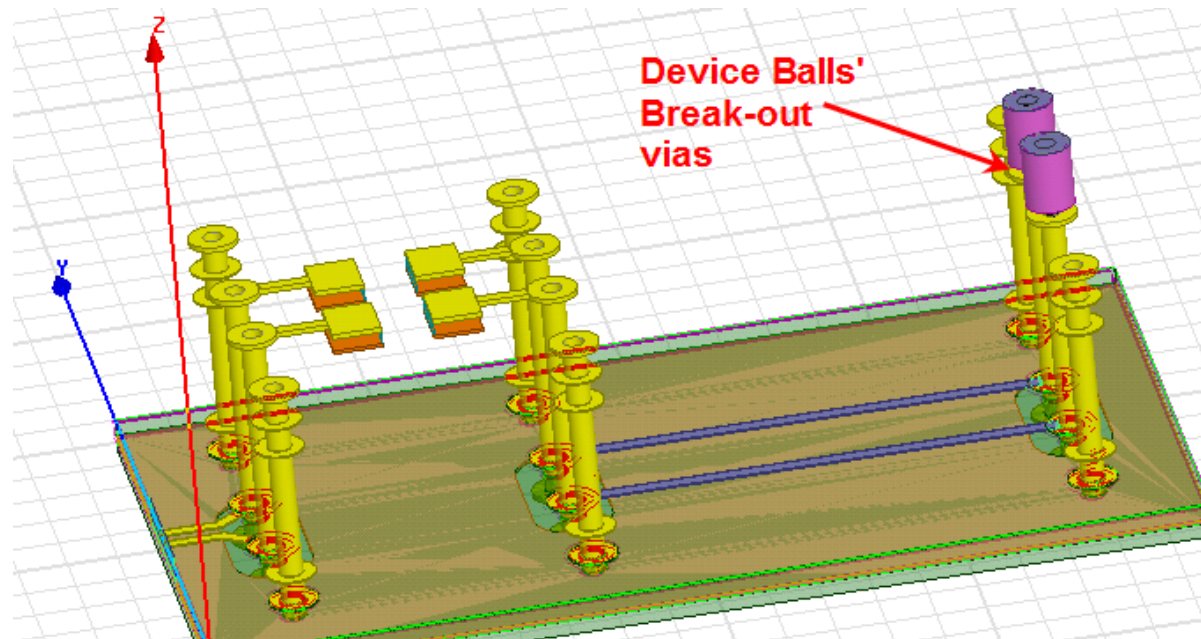


Observations

- Poorly designed DC blocking vias may cause a major interconnect degradation impact
- The DC blocking capacitor mounting construction has an impact of ~1dB -2dB @ $F_b/2$ and an higher ILD peak. Worst case may occur if $F_b/2$ happens to “fall” on the ILD peak (Murphy’s Law?).
- Major impact is due to capacitor related mounting vias, however, no major design “violation” was performed, rather the vias were not optimized.
- Lower loss material may lower the impact once vias are optimized (reflections minimized) – Did not pursue this in this presentation.
- Minor impact was observed up to ~6GHz → The former 10GBase-KR decision to allocate the Rx cap to the receiver acceptable and understandable.

Observations – Cont.

- There were vias which concluded in 0.6dB impact @ Fb/2 (inc. cap).
- Another via could have been added for device break-out.



Thank You
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Questions?

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