100GBASE-KP4 jitter and distortion specification proposal

(Regarding comment #255 on D1.1)

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Supporters

- Richard Mellitz, Intel
- Kent Lusted, Intel
- Liav Ben-Artsi, Marvell
- Rick Rabinovich, Alcatel-Lucent
- Vasudevan Parthasarathy, Broadcom
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- Mike Dudek, QLogic

Background

- Existing jitter specifications rely on zero crossing measurements
  - Two electrical levels create two possible transitions – 0→1 and 1→0
  - In an ideal transmitter, all crossings occur at the same phase
  - Low frequency jitter is filtered and (in clause 85) DDJ is excluded
    - Receiver is assumed to handle both
- This method has some drawbacks – but seems to work for NRZ.
- For 100GBASE-KP4 (PAM-4), a new method is required.

Consensus group

- 4 conference calls were conducted to discuss jitter specification ideas.
- 29 individual participants: Yasuo Hidaka, Magesh Valliappan, Kent Lusted, Richard Mellitz, Mike Li, Mohammad Kermani, Beth Kochuparambil, Scott Irwin, Hiroshi Takatori, Vittal Balasubramanian, Joel Goergen, Wheling Cheng, John Wang, Albert Vareljian, Michael Altmann, Liav Ben-Artsi, Matt Brown, Vasudevan Parthasarathy, Will Bliss, Mike Dudek, Rick Rabinovich, Pavel Zivny, Piers Dawe, Oren Ganon, Adam Healey, Arash Farhood, Charles Moore, Greg Lecheminant, Adee Ran
- Thanks for attending, sharing thoughts and reviewing ideas!

Reasoning for new proposal for PAM4

- In PAM4, there are 3 separate level at which “crossings” can be defined; therefore
  - Many transitions exist in a data signal; each transition has its own mean phase
  - DDJ analysis as done in NRZ is not practical
- **Proposed replacement – intended to be both simple and predictive:**
  1. Use simple 2-level patterns to measure PLL-related “jitter” (phase noise) separated into random and deterministic components, and even-odd jitter (EOJ); specify maximum values
  2. Use distortion analysis with a rich signal to measure jitter-induced noise; specify a minimum ratio of signal to noise and distortion (SNDR).

Proposal – part 1

- Define two new jitter test patterns (denoted as repetitive sequences, each symbol for 1 UI)
    1. JP03: 03 (periodical at 2 UI – Nyquist frequency)
    2. JP03a: 15 repetitions of “03” and then 16 repetitions of “30” (periodical at 2*(15+16)=62 UI ➔ 219 MHz)
        - In both cases, 0 denotes the −1 PAM4 symbol, and 3 denotes the +1 PAM4 symbol
- Use JP03 to measure RJ and deterministic clock jitter (DCJ)
    - Method described below (based on well-known Dual-Dirac)
    - DDJ doesn’t exist, so need not be excluded
- Use JP03a to measure EOJ
    - Enables measuring both duty cycle and rise/fall time distortion
    - Total length is 2*31UI – 31 is prime, so all internal busses are “challenged” equally (with reasonable implementations)
- Specifications shall be met with any valid equalization setting

RJ and DCJ measurement procedure #1

- Use JP03 to measure RJ and DCJ.
  - All 4 lanes active and transmit same sequence
- Capture a waveform of N UI ($N \geq 10^7$) e.g. using a real-time scope.
- Calculate the zero-crossing times $T_{ZC}(i)$, i=1..N (interpolate if necessary).
  - Align so that $T_{ZC}(1)=0$
- Calculate the average pulse width: $\Delta T_{AVG} = \frac{\sum_{i=2}^{N} T_{ZC}(i) - T_{ZC}(i-1)}{N-1}$
- Calculate the phase jitter series: $\tau(n) = T_{ZC}(n-1) - (n-2)\Delta T_{AVG}, \quad n = 2..N$
- Apply a 1st-order discrete high-pass filter $H_{CDR}(z)$ to the phase jitter series $\tau(n)$.
  - Denote the result $\tau_{HPF}(n)$

RJ and DCJ measurement procedure #2

- Sort the values of $\tau_{HPF}(n)$ in increasing order
  - Denote the result $\tau_{sorted}(n)$
- Determine the values J_5 and J_6 (in units of time) as follows (with either B=5 or B=6)
  - J_B^- is the maximum time that satisfies
    $$\tau_{sorted}(0.5\times10^{-B}\times N) \le J_B^-$$
    (typically negative)
  - J_B^+ is the minimum time that satisfies
    $$\tau_{sorted}(N - 0.5\times10^{-B}\times N) \ge J_B^+$$
    (typically positive)
  - $J_B = J_B^+ - J_B^-$
- Similar to clause 86.8.3.3 definitions

RJ and DCJ measurement procedure #3

- Calculate RJ_{RMS} and DCJ according to:

$$\begin{bmatrix} RJ_{RMS} \\ DCJ \end{bmatrix} = \begin{bmatrix} 2Q^{-1}(0.5\times10^{-6}) & 1 \\ 2Q^{-1}(0.5\times10^{-5}) & 1 \end{bmatrix}^{-1} \begin{bmatrix} J_6 \\ J_5 \end{bmatrix}$$

Where Q^{-1} is the inverse Q-function.

EOJ measurement procedure

- Use JP03a to measure EOJ
  - All 4 lanes active and transmit same sequence
- Capture 20 full cycles of JP03a
- Interpolate if necessary and calculate the average zero-crossing time for each of the 60 transitions in JP03a, relative to start of pattern
  - Average is calculated across the 20 full pattern cycles
  - Denote the average values by $T_{ZC}(i)$, i=1..60, where i=1 is the first transition following the two consecutive “3” symbols
- Calculate the widths of 40 pulses from 41 transitions excluding the “repeated symbols” vicinity:

$$\Delta T(i) = \begin{cases} T_{ZC}(i+10) - T_{ZC}(i+9), & 1 \le i \le 20 \\ T_{ZC}(i+19) - T_{ZC}(i+18) & 21 \le i \le 40 \end{cases}$$

- EOJ is half of the magnitude of the difference between the mean width of the even pulses and the mean width of the odd pulses:

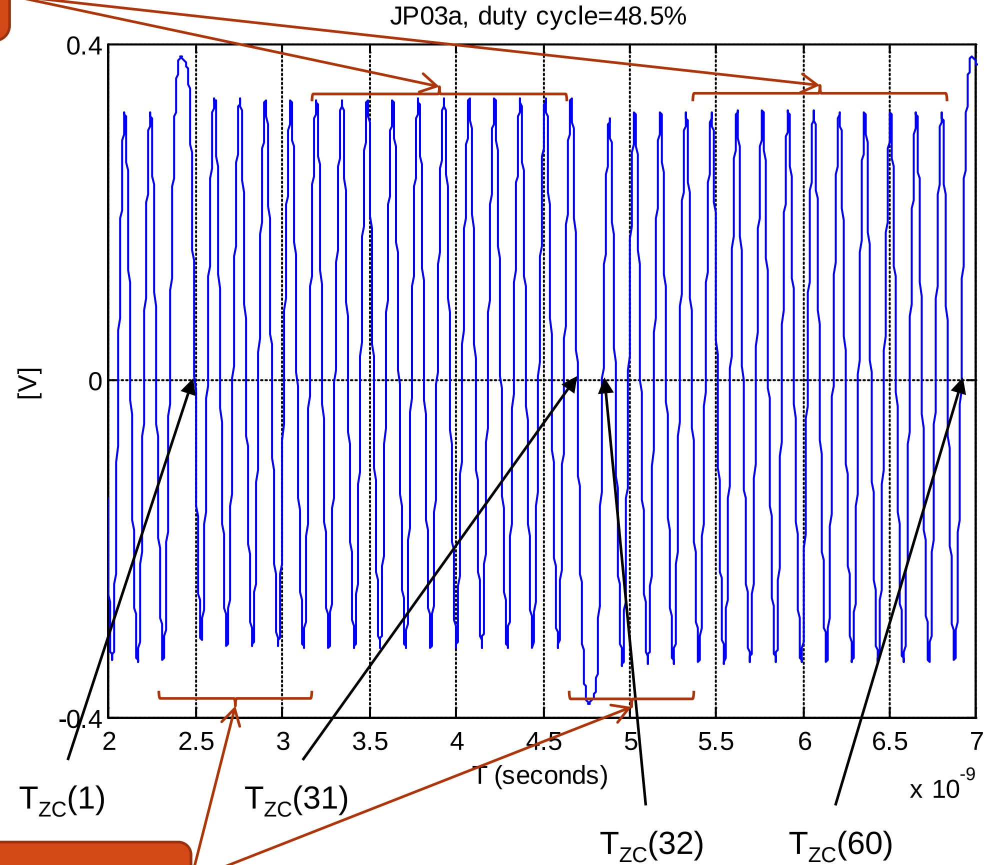
$$EOJ = \frac{\left| \sum_{i=1}^{20} \Delta T(2i) - \sum_{i=1}^{20} \Delta T(2i-1) \right|}{40}$$

Example: EOJ measurement using JP03a

Clock duty cycle error is 3% PTP

Measure widths of 10 “3” and 10 “0” pulses in each half-pattern

- This is the voltage signal resulting from simulation of JP03a driven through a risetime filter + sample package and test fixture (provided by Liav Ben-Artsi).
- The clock driving the signal has a slight duty cycle mismatch, in addition to DJ and RJ.
- From this signal, calculation of EOJ is straightforward. Results are shown in next slide.



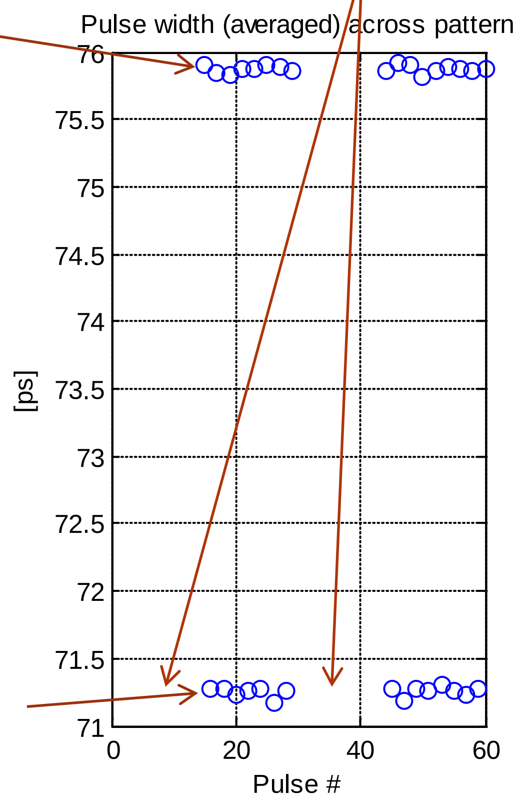
Ignore “repeated symbols” area

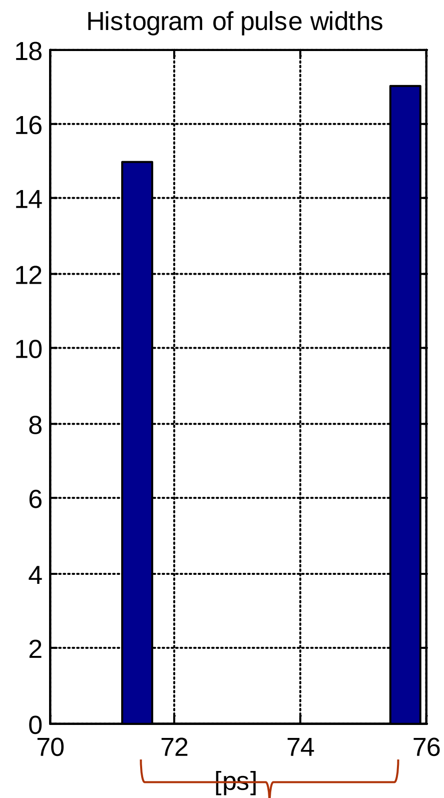
Example: EOJ measurement using JP03a

Even pulses are longer

Ignored pulses

- Measured EOJ is 2.4 ps ≈ 3.2 % UI.
- Compare to applied duty cycle of 3%.





Odd pulses are shorter

EOJ=2.4 ps

Proposal – part 1 – summary

- Changes to clause 94.3.11.9 “Transmitter output jitter”:
  - Specify RJ_{RMS}, DCJ and EOJ measurement method as defined above
    - Instead of current definitions based on BER terms (BER is not defined at the transmitter…)
    - Enables avoiding definitions like “TJ at BER”, “TJ excluding DDJ” and “TJ minus DJ”
    - No need to refer to old methods (e.g. annex 48B)
  - Specify two new test patterns and management functions: JP03 to measure RJ_{RMS} and DCJ, JP03a to measure EOJ
  - Remove references to clause 92.8.3.8 which currently uses the old method
- Examples and proposed limits in next slides…

Proposal – part 1 – suggested limits

Parameter	Notes	Value	Units
RJ_{RMS}	1	< 0.37 < 0.5%	ps UI
DCJ (including EOJ)	1	< 3.68 < 5%	ps UI
EOJ	2	< 2.21 < 3%	ps UI

1. Use JP03
2. Use JP03a

Note: These values were used to create the worst-case distortion for part 2. Final values may be different. Limits proposed as TBD.

Proposal – part 1 – Test parameters

Parameter	Notes	Value	Units
Cutoff frequency of 1st-order high-pass filter applied to zero-crossing periods in RJ and DCJ measurement	1	≤0.005	GHz

TBD

Notes:

1. The bandwidth limit denotes the “best case” conditions required to pass a test. A test can be conducted with lower filter bandwidth; in such case, meeting required limits shows positive margin, but failure to meet them does not disqualify the device under test.

Proposal – part 2

- NRZ jitter measurement includes non-linear effects that occur at the zero crossing phase
  - Linear effects cause DDJ, which should be excluded
- The proposed alternative for PAM4 is TX distortion analysis
  - Captures all non-linear effects (comprehensive)
  - Also captures TX internal crosstalk (not accounted for in other tests)
- This proposal complements COM and receiver testing:
  - Noise content of TX can be accounted for in COM
  - Real TX can be used in RX testing; if it's not "worse case", noise can be added to calibrate test conditions

Distortion analysis – general idea

- Distortion analysis shows non-linear effects as an additive noise component. In the method described in 85.8.3.3.5, this is the signal e(n) calculated from measurement y(n).
- Proposal is to limit the noise power at any phase, not just the average.
  - Channel can “mix phases”, so better be conservative.
  - This may penalize drivers with jitter and very short risetime (at TP0a); but with a reasonable test fixture it should not be a problem.
- Looking at e(n) at each phase separately can reveal noises at transitions.
  - Assuming the procedure in 85.8.3.3.5 is used for measuring equalization steps – existing data can be re-ordered and used.

Distortion measurement procedure #1

- Transmit a rich-spectrum PAM4 test pattern, different for each lane
  - E.g. Same pattern as the one defined in the training proposal – see backup
- Capture N UI (where N is an integer multiple of the test pattern's length in UI), with M samples per UI: ➔ y(k), k=0..M*N-1
- Calculate a linear channel fit of the measurement (e.g. as done in clause 85.8.3.3.5)
- Denote the linear-fit waveform as f(k) (read column-wise from the matrix product PX_1) and the error waveform as e(k), so that y(k)=f(k)+e(k), k=0..M*N-1

Distortion measurement procedure #2

- Separate f(k) and e(k) into M subsets f_p and e_p, p=0..M-1; subset p includes samples p+j*M, j=0..N-1
  - Call these subsets "phase p" of measurement and error
- For each of the M phases, calculate the RMS of the measurement and RMS of the error
- Calculate S, the minimum signal level at the "best vertical opening" phase
  - See backup for details
- Define the TX SNDR per phase p as $SNDR_{TX}(p)=S/RMS(e_p)$
- $SNDR_{TX}(p)$ should be above a specified value for any p

Example – distortion analysis with simulated jitter

Estimated signal level (S)

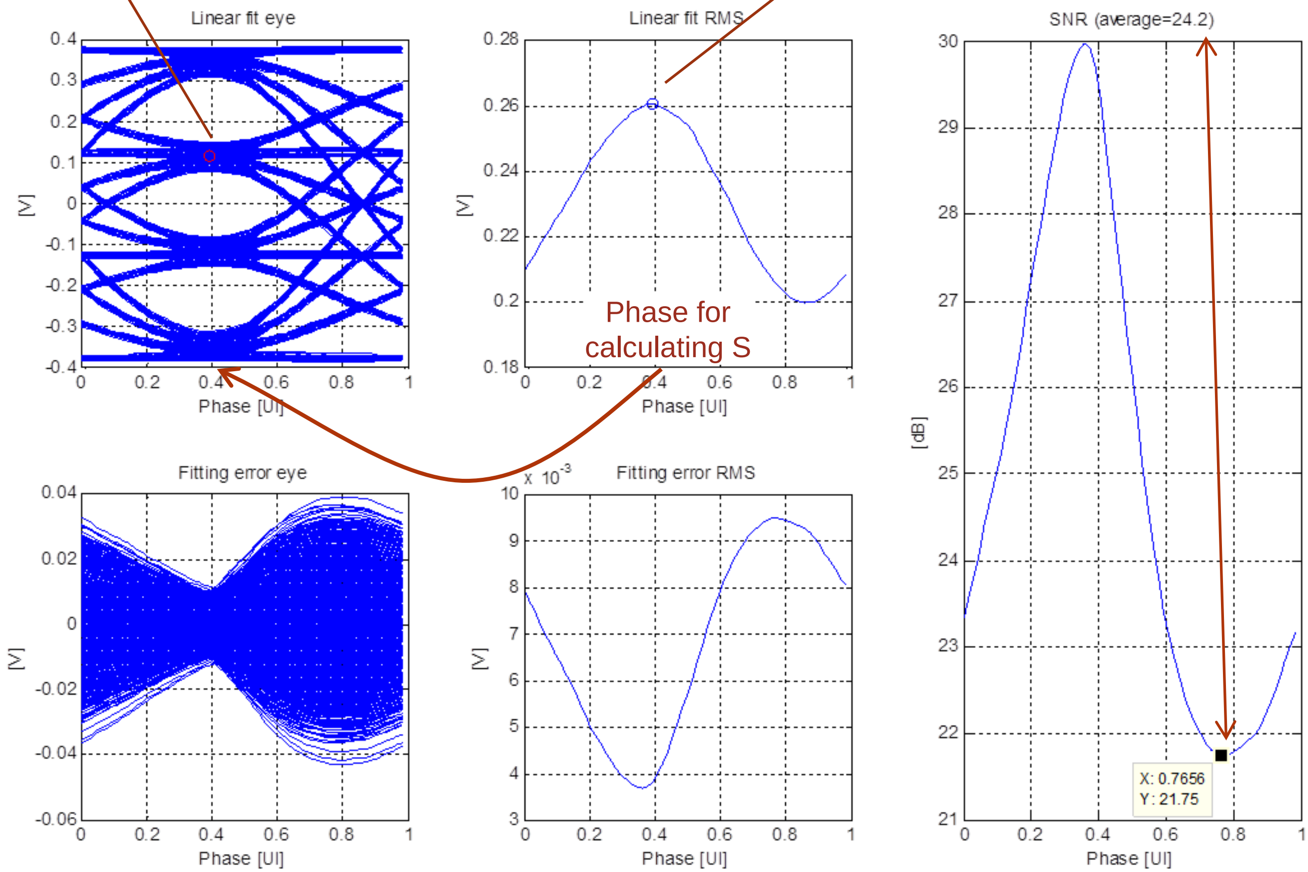
Signal RMS per phase; max RMS phase marked

Simulated TX with:

- RJ RMS=0.37 ps
- EOJ PTP=3%
- SJ PTP =1.47 ps (total DJ = 3.68 ps)

(Assumed worst case)

Risetime filter and test fixture



Linear fit and error shown as eye patterns.

Note that error is much larger at the "transition phases" than at the "sampling phases".

SNDR per phase. Note minimum is ~2.5 dB lower than "average" SNDR.

Proposal – part 2 – suggested limits

Parameter	Subclause reference	Value	Units
$SNDR_{TX}$ (at worst phase)		> 19	dB

TBD

Notes:

- Proposed SNDR limit is intended to let TX distortion consume only a small part of the noise budget, assuming FEC coding gain, but still be realizable.
  - Under the worst-case jitter assumptions (suggested values of part 1), the TX has ~3 dB margin for other possible distortion effects.
  - This value can be applied to COM channel specification, e.g. by addition of a signal-dependent noise component.

Proposal – part 2 – Test parameters

Parameter	Notes	Value	Units
Test pattern period	1	8372	UI
Acquisition period (N)	2	≥10^6	UI
Samples per UI (M)	2	≥16	
Linear fit pulse length (N_p)	3	10	UI
Linear fit pulse delay (D_p)	3	2	UI

TBD

Notes:

1. Proposed test pattern described in training proposal lusted_01_0912.
2. The measurement length specifies the “best case” conditions required to pass a test. A test can be conducted with a longer measurement; in such case, meeting required limits shows positive margin, but failure to meet them does not disqualify the device under test.
3. Refer to Table 94-5.

Backup

Details of linear fit procedure

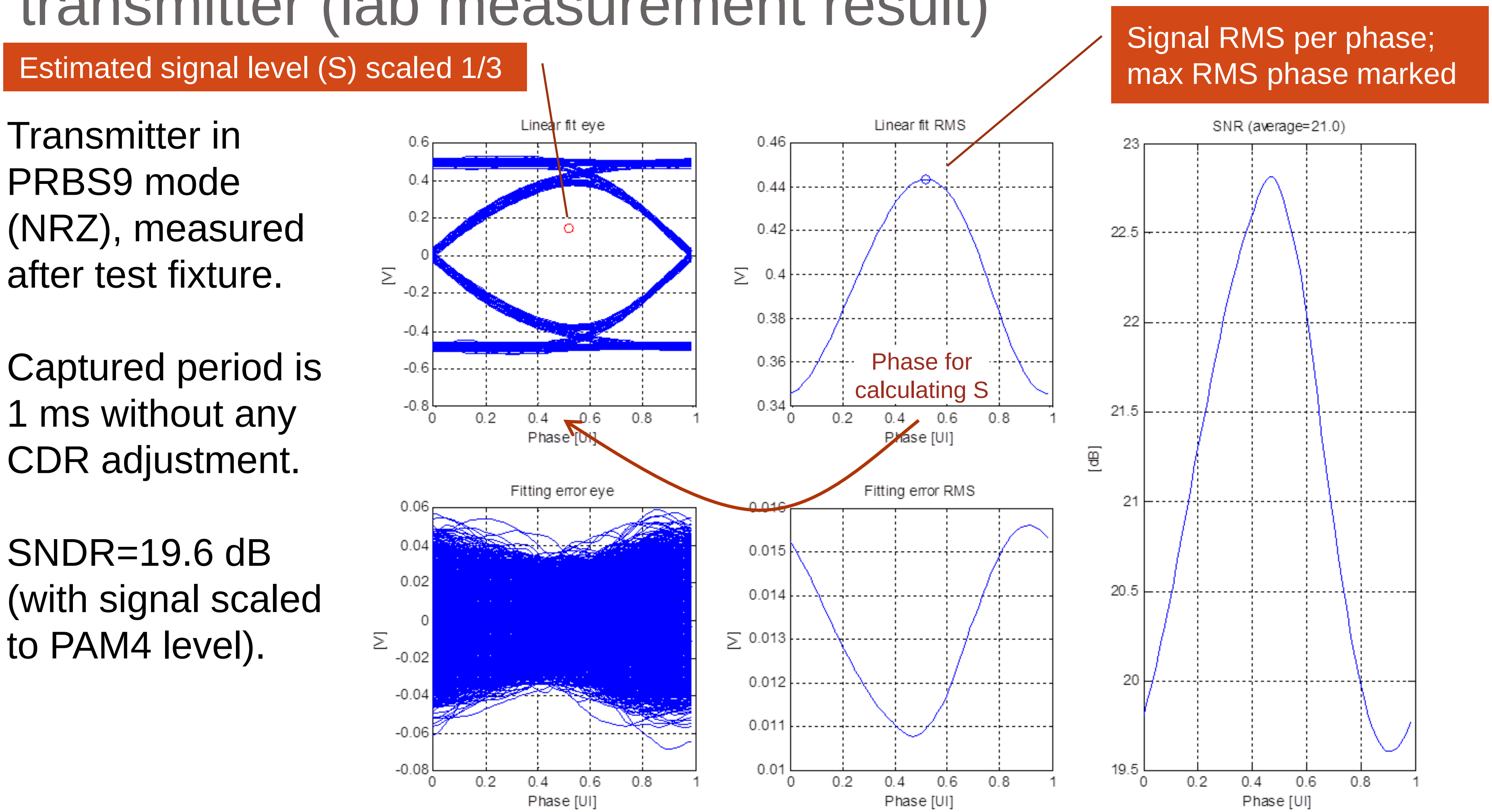
- In clause 85.8.3.3.4, averaging multiple waveform captures is recommended. This is not allowed here, since jitter effects would be diminished.
- Applying a behavioral CDR and re-sampling to get integer oversampling are allowed.
- To estimate the signal level S:
  a) Find the phase p_max in which f(k) has maximum RMS
  b) Divide the samples of f_{p_max} into groups according to the 4 voltage levels
  c) Define S_i to be the median of the samples in group i, i=0..3
  d) Define S as $\min(S_i - S_{i+1})/2$, i=0..2

Example – distortion analysis with 40GBASE-CR4 transmitter (lab measurement result)

Transmitter in PRBS9 mode (NRZ), measured after test fixture.

Captured period is 1 ms without any CDR adjustment.

SNDR=19.6 dB (with signal scaled to PAM4 level).



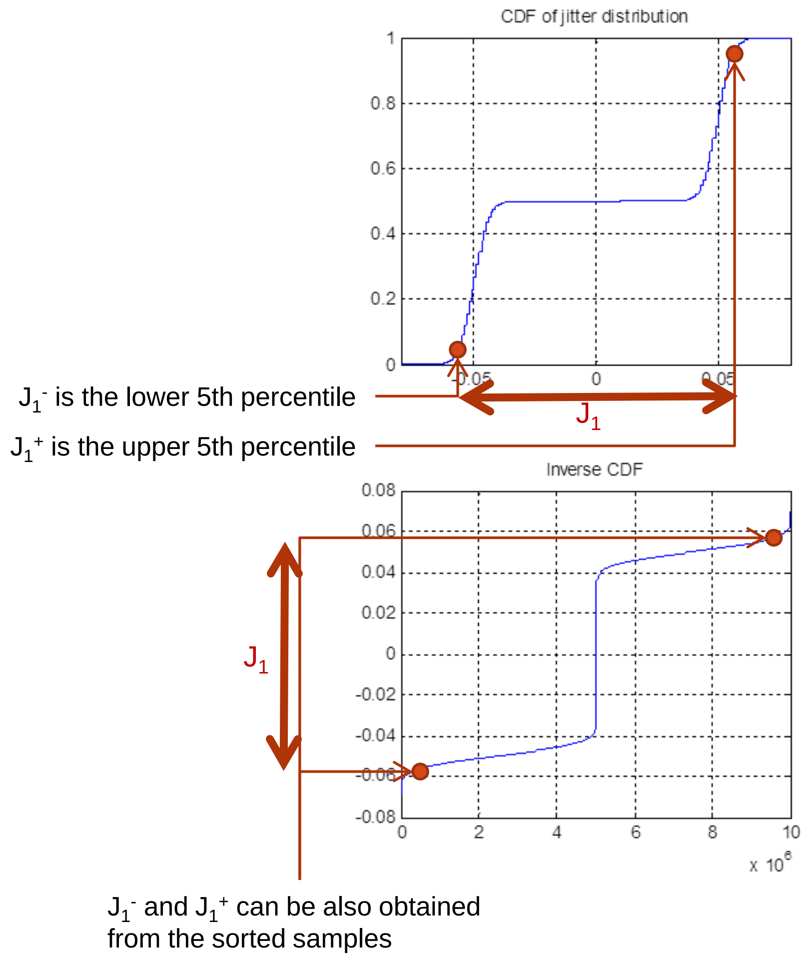
Data provided by Oren Ganon, Intel

How do the suggested limits compare to 10GBASE-KR?

- Part 1 sample specifications seem tighter than clause 72 equivalents
  - RJ limit was (effectively) 0.01 UI RMS – now 0.005 UI
  - DJ limit was 0.15 UI – now (DCJ) 0.05 UI
  - DCD limit was 0.035 UI – now (EOJ) 0.03 UI
  - And new UI is 74% of clause 72…
- Part 2 has no counterpart clause 72, but can be compared to 85.8.3.3.5
  - The required "normalized RMS error" is roughly equivalent to the minimum SNDR value (with smaller S)
  - But now it is required for any phase, not just the average
  - Averaging isn't allowed, but behavioral CDR can be applied
- **Justification**
  - Challenge is tougher – PAM4 has less margin
  - Jitter can have a big impact on RX performance; old specifications can't be assumed to "just work" (see also part 2 example)
  - New test methods can provide margin
    - No DDJ in measurement (note: no exclusion in clause 72); DCJ is not the same as DJ
  - High volume products built with current technology meet these specifications
    - See measured example in previous slide

Meaning of J_5 and J_6

- The procedure used to calculate RJ_{RMS} and $DJ_{\delta\delta}$ uses the intermediate values J_5 and J_6.
- The method is essentially an estimate of CDF values from samples, using the inverse CDF calculation as shown at the right (demonstrated for J_1).



Which test pattern to use?

- Training proposal (ref. lusted_01_0912) defines spectrally rich training patterns with low correlation between lanes
  - PRBS13 translated to PAM4 with termination and precoding
- These features are useful for linear fitting and distortion analysis
- The training pattern length N (excluding marker and control channel) is 8372 UI
  - Compare to the 511-UI long PRBS9 used in the past
  - Procedure requires inverting an N-by-N matrix
- Today's workstations have enough computing power to perform such computations within <1 minute